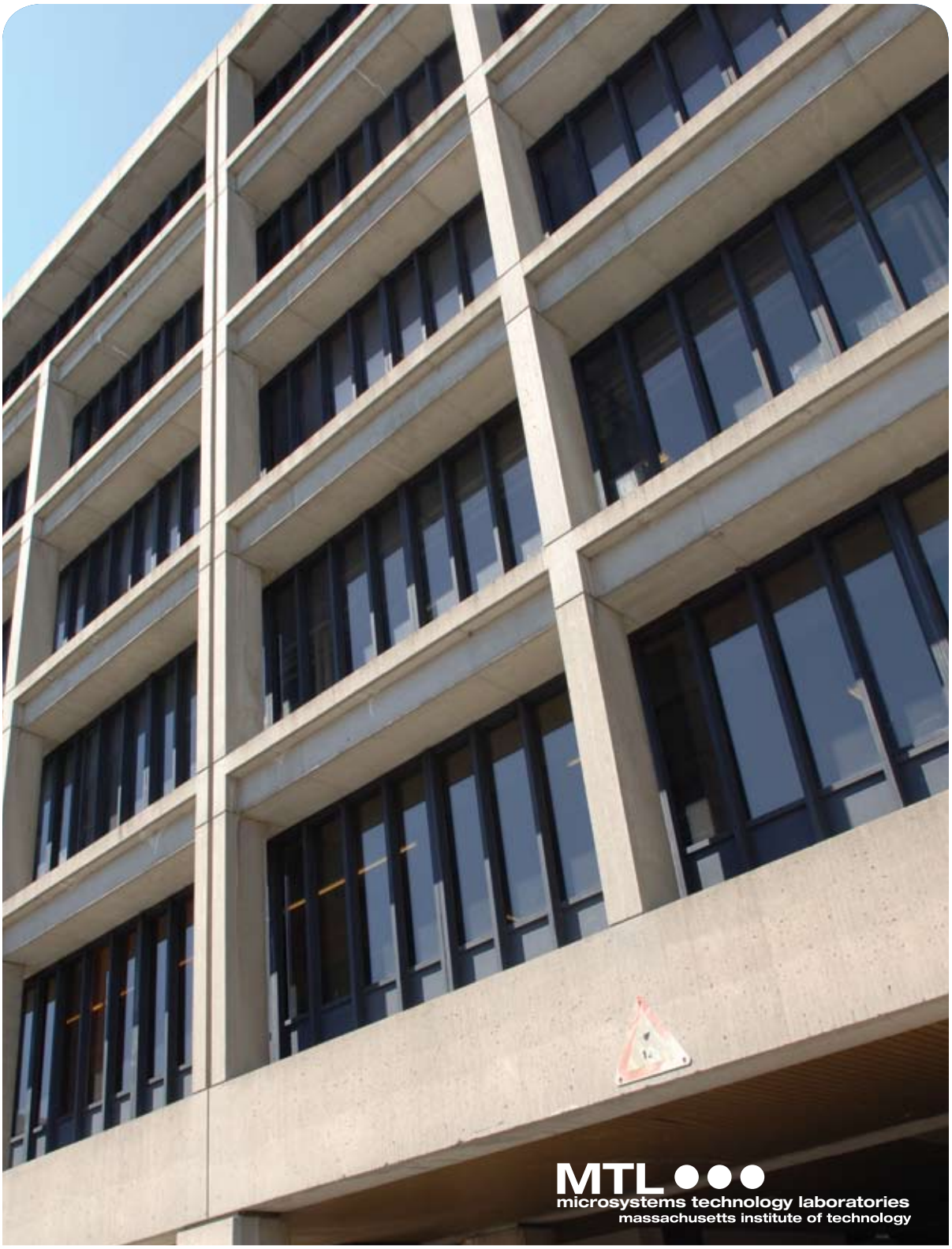

MTL

microsystems technology laboratories

massachusetts institute of technology

ANNUAL RESEARCH REPORT

2004 - 2005

MTL Annual Research Report 2004-2005

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INTRODUCTION

Welcome to the 2005 MTL Annual Report. This report contains research abstracts from faculty and senior research staff whom are associated with the MTL. The work spans a broad range of topics from Circuits and Integrated Systems to Molecular and Nanotechnology. These investigators come from more than 30 different departments, labs, and centers across the Institute.

This year, the Annual Report format and appearance has been changed to provide a more effective means of communicating the various activities in and around MTL. In particular, we have adhered to a strict one-page format for the Annual Report abstracts which are intended to give the reader a high level view of the project, and provide information on where to find more detailed information. This report is also available on the MTL web site at http://mtlweb.mit.edu, which includes links to more detailed content.

The MTL Mission states that we are an Interdepartmental Laboratory that encompasses research and education with an intellectual core of i) Semiconductor Process and Device Technology, and ii) Integrated Circuits and Systems Design. MTL fosters new initiatives in Microsystems at the Institute. MTL provides Microsystems infrastructure to the Institute.

Organizationally, MTL supports this mission by focusing on two major goals; maintaining and supporting a core research community which is aligned with our research mission, and managing a set of shared experimental facilities which support of the core research community as well as the broader campus community. In addition, MTL maintains a strong relationship to industry through a portfolio of relationship options.

The core research community is comprised of approximately 20 faculty and senior research staff that do research in areas of integrated circuits and systems, nanoelectronics, photonics, MEMS, and molecular and nanotechnology. These faculty are closely aligned to the industries which commercialize this research. The community is maintained through a collection of activities including seminars, committees and an annual research conference attended by approximately 150 persons.

The shared experimental facilities are comprised of three different clean-rooms which support micro and nano fabrication technologies from advanced silicon processing, to a diverse range of materials. These three facilities are centrally managed by a professional staff of 16 engineers and technicians. In addition to the fabrication facilities, the MTL also maintains computer infrastructure for CAD as well as testing equipment. More details on the facilities are provided later in this report as well as on the MTL web site.

MTL has a portfolio of industrial engagements from major alliances to individual research grants. The flagship relationship is the Microsystems Industrial Group (MIG) which is a consortium relationship which provides members with priority access to the students and research output of the lab. In addition, four industrial research centers with more focused interests are associated with the MTL; Center for Integrated Circuits and Systems (CICS), Intelligent Transportation Research Center (ITRC), MEMS@MIT, and the Center for Integrated Photonic Systems (CIPS).

Martin A. Schmidt, MTL Director.

ACKNOWLEDGEMENTS

All of us at MIT are grateful to the following organizations for their generosity and participation in the Microsystems Industrial Group (MIG). Their membership makes possible the continuing operations of the Microsystems Technology Laboratories:

Advanced Micro Devices
Analog Devices
Applied Materials
Hewlett-Packard
IBM Corporation
Intel Corporation
National Semiconductor
Novellus Systems, Incorporated
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We would also like to acknowledge past support of the Microsystems Technology Laboratories by the following organizations:

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Polaroid Corporation
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Raytheon Corporation
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We also wish to acknowledge the support of those organizations who have generously contributed equipment for use at the Microsystems Technology Laboratories:

Agere Systems
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  Intelligent Transportation Research Center
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  Laboratory of 3D Optical System
  Lincoln Laboratory
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  Microchemical Systems Technology Center
  MicroPhotonics Center Consortium
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National Renewable Energy Laboratory
National Science Foundation
  Chemical and Transport Systems
  Engineering Research Center for Environmentally Benign Semiconductor Manufacturing (NSF/SRC)
  Fellowship
  Grant Opportunities for Academic Liaison with Industry
  Materials Research Science and Engineering Centers
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  Nanoscale Interdisciplinary Research Team
  NSE and CAREER program
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XOPT, Inc.

RESEARCH THEMES

The research in MTL spans an extraordinarily broad set of activities. If one were to identify a unifying theme associated with these projects, it would be the system-level interest in micro and nano technology. The MTL represents a community which brings experimentalist skilled in materials and technology at the micro and nano-levels together with circuits/systems researchers to realize visions for new systems which are enabled by the integration of these disciplines.

In the past year, the circuits and systems group engaged in research in the areas of RF design, including receivers, modulators and power devices. Wireless systems remained a major focus area in both the high performance and ultra-low power domains. The high performance wireless research was primarily directed towards gigabit LAN, whereas the low power systems were in support of wireless sensor networks primarily. This coupled to an extensive range of research on low-power design in general. Analog to digital conversion and mixed signal circuit design continue to be a major focus area. Intelligent transportation systems, and vision systems in support of these were studied. As part of a larger overall effort on interconnect issues, there was considerable work on circuit/systems issues in interconnect and the investigation of 3D systems. Analysis tools for design of circuits and test devices to understand manufacturing issues provided core underpinning research for the entire circuits and systems area.

A wide range of emerging technologies were explored and are reported in detail in our Annual Report. 'Substrate engineering,'

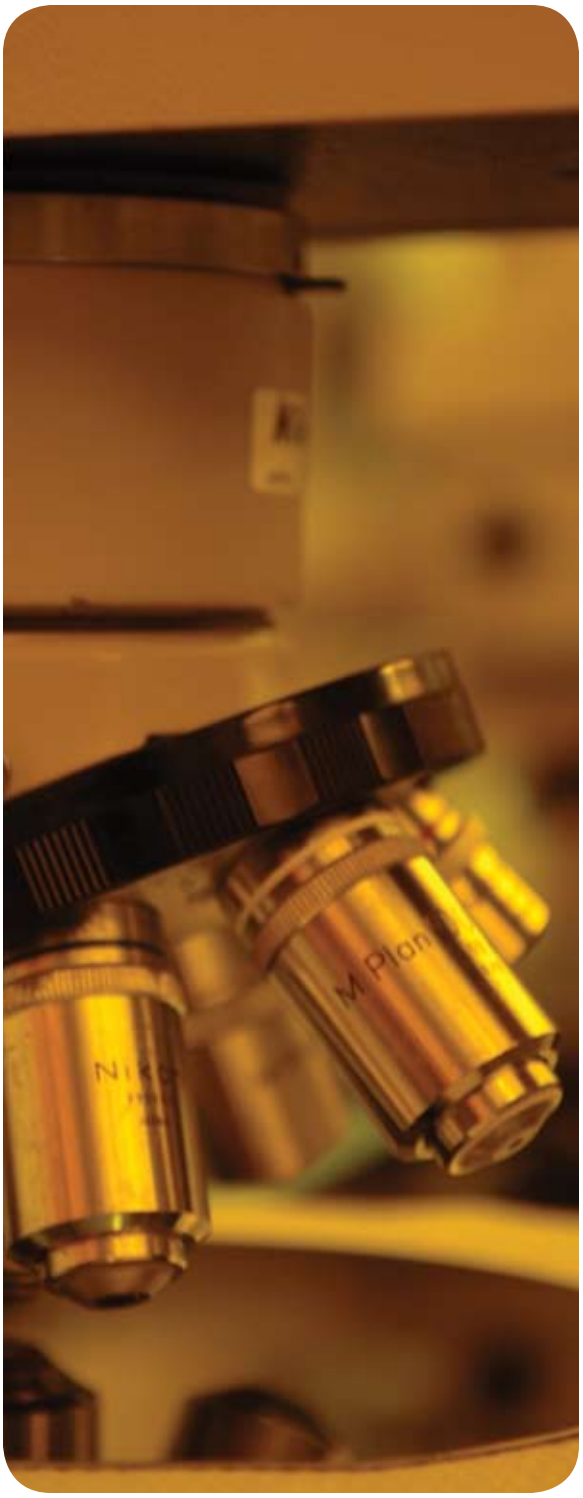
or the development of optimized silicon-based hetero-structures, was a substantial activity, as was the exploration of novel means to achieve device isolation in integrated systems. Compound semiconductor systems such as InP/GaAs were explored for high performance RF devices. Field emission structures were studied for a variety of applications in devices and displays to name a few. In the areas of advanced fabrication technologies and materials, we saw exciting work on magnetics, metal interconnect materials, and environmentally-benign processes. Lastly, we saw substantial and growing focus on new non-silicon devices in organic and inorganic materials systems.

Photonic devices were studied for a wide range of applications. Quantum dots, photonic crystals and display materials and devices were explored, as well as J-aggregates. Lasers in compound semiconductor materials and heterogeneous integration methods for merging such devices with silicon platforms were pursued. Integrated silicon photonics and silicon-compatible optical interconnect methods were developed. MEMS structures were merged with optics to achieve new functionality in optical systems.

In the area of MEMS, the primary focus areas are; bio/chemical devices and systems, power devices, and a variety of enabling technologies. A large number of microfluidic devices are being developed for manipulation of cells, DNA, proteins, and other molecules. Microreactors are being designed which enable the synthesis of chemicals at a small scale, as well as microbioreactors which can be used in areas such as fermentation studies. Microchemical analysis systems such as portable gas analyzers are also studied. In the area of portable power generation, we are exploring both fuel-burning and energy harvesting approaches. The primary focus of

the energy harvesting approaches is to utilize piezoelectric materials for vibration harvesting. In the area of fuel-burning systems, we are exploring microturbines as well as fuel cells and thermophotovoltaics. Beyond these systems focused projects, there are a wide ranging set of projects looking into the applications of MEMS technologies for mechanical devices such as switches, tweezers, and nano-assembly. Lastly, there are some core technology development efforts to understand better, model, and characterize MEMS materials and structures.

Molecular and nanoscale devices are a new and emerging area of work in the lab. Nanoscale assembly methods inspired by origami are studied, as well as nanoscale field ionizers. Nano-dimensioned fluidic channels enable manipulation of chemicals and molecules that are nanoscale. Organic and quantum dot structures are explored for many electronic and photonic purposes. Carbon nanotubes have emerged as potentially exciting structures to explore for many different applications. The work in this area includes not only studying the material, but developing means for fabrication and manipulation of the nanotubes. Magnetic nanoparticles hold great promise in advanced devices and are extensively explored. Self-assembly methods appear as promising methods for creating ordered nanostructures and these methods are being studied in detail. Quantum-effect devices are explored for a variety of applications including quantum computing.



MTL FACULTY RESEARCH AREAS AND SPECIAL INTERESTS

A.I. Akinwande
Display devices: Flexible large area electronics, organic and inorganic thin film transistors, field emission displays; High Aspect Ratio Gated Microstructure Arrays: field emission devices, electrospray thrusters and gas analyzers.

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Molecular electronics, integration of biological materials and conventional electronics, electrical and exciton transport in organic materials, energy transfer, metal-organic contacts, nanomechanical organic transistors.

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3D optical systems. Spatial 3D and spectral imaging with a single camera and without scanning. MEMS for integrated optics. Nanostructured Origami(TM) 3D fabrication and assembly process for nanomanufacturing.

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Characterization and modeling of variation in semiconductor and MEMS manufacturing, with an emphasis on chemical mechanical polishing (CMP), plasma etch, and advanced interconnect processes. Understanding the impact of process and device variation on circuit performance, and design for manufacturability.

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Physical properties of organic and organic/inorganic nanocrystal composite thin films and structures, and development of novel optoelectronic nanostructured devices.

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Design of digital integrated circuits and systems with an emphasis on the energy-efficient implementation of microsensor networks and ultra-wideband systems. Circuits techniques for deep sub-micron technologies and 3D integration.

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Heat transfer and energy conversion at micro- and nanometer scales, including microelectronics, photonics, thermoelectrics, thermionics, and thermophotovoltaics; solid-state micro- energy conversion devices and materials, radiation transport and electromagnetic metamaterials; micro and nanofabrication.

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M.J. Cima
Formation of methods for complex macro and micro devices, using three-dimensional printing. Development of chemically derived epitaxial oxide films for HTSC coated conductors. Implantable MEMS devices for drug delivery and biomedical applications. Devices and processes for high throughput combinatorial screening of complex materials formulations.

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M.L. Culpepper

Macro-, micro-, and nano-scale machines for precision positioning, assembly, and manipulation. Basic and applied research on physical principles, modeling approaches, synthesis/simulation tools, and manufacturing practices. Design and integration of mechanical systems with multi-scale (macro, micro, nano) components. Hands-on education applied to the mechanical design of macro-, micro-, and nano-scale devices.

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Model order reduction, parasitic extraction, electromagnetic interference, mixed-signal and analog RF circuit modeling and synthesis, power electronics, MEMs design and modeling.

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Microelectronics device technologies for gigahertz and gigabit-per-second communication systems: physics, modeling, technology and design. Technology and pedagogy of online laboratories for engineering education.

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Nanofluidic / Microfluidic technologies for advanced biomolecule analysis and sample preparation: novel nanofluidic phenomena, nanofluidic biomolecule separation and pre-concentration, molecular transport in nano-confined space.

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Novel processes, materials, and device concepts for silicon technology. Device physics and epitaxial growth of silicon-based heterostructures and nanostructures. Strained Si MOSFETs, heterojunction bipolar transistors, CMOS front-end processing, and silicon-germanium photodetectors.

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Design, fabrication, testing, and integration of microsystems for chemical and biological discovery, synthesis, and processing. Microsystems for energy applications, including microcombustors, micro-reformers, thermophotovoltaic, and solid oxide fuel cells. Chemical kinetics and transport phenomena related to processing of materials for biomedical, electronic, and optical applications.

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MTL FACULTY RESEARCH AREAS AND SPECIAL INTERESTS continued

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Synthesis and characterization of carbon nanotubes. Applications of nanotube electrical devices.

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H.-S. Lee
Analog and mixed-signal integrated circuits in CMOS Technologies. Subsystems and circuits including analog-to-digital and digital-to-analog converters, operational amplifiers, and signal processing circuits. Applications include communication systems, portable electronics, and multimedia.

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Circuit and architecture design for high speed mixed-signal circuits such as phase-locked loops and A/D converters: circuit topologies, architectural approaches, design methodologies, modeling, and simulation techniques. Communication system simulation software and tutorials for engineering education.

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Microelectronics and technologies for three-dimensional integrated circuits: design, modeling, and technology development. Carbon nanotubes technology development for microelectronic applications

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Fabrication, properties, and applications of magnetic films and nanostructures. Self assembly.

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Advanced lithography, including X-ray, electron-beam, ion-beam, and optical. Nanotechnology and nanofabrication. Precision engineering and nano-accuracy dimensional metrology. Advanced interference lithography technology for super-accurate patterning of general grating and grid patterns. Micro and nanometer fabrication technology applied to advanced astronomical and laboratory instrumentation. Silicon micromachined structures applied to high-precision optical assembly. X-ray optics and instrumentation.

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MicroElectroMechanical Systems (MEMS) Microfabrication technologies for integrated circuits, sensors, and actuators; design of micromechanical sensor and actuator systems; mechanical properties of microelectronic materials, with emphasis on silicon wafer bonding technology; integrated microsensors; and microfluidic devices. Novel applications of MEMS and nanotechnologies to a variety of fields, including miniature gas turbines, miniature chemical reactors, microswitches, biological applications and sensors monolithically integrated with electronics.

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Micro-scale gas bearing dynamics, aero-acoustics, internal flows in turbomachinery, compressor aerodynamics and stability, and dynamic system modeling of aircraft gas turbine engines.

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Modeling of noise and dynamics in circuits and systems. Application of convex optimization to digital communications, analog and VLSI circuits. Communications and signal processing architectures. High-speed electrical and optical links, on-chip signaling, clock generation and distribution. High-speed digital and mixed-signal IC design.

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MTL FACULTY RESEARCH AREAS AND SPECIAL INTERESTS continued

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MEMS Power Devices and Energy Harvesting; Nanocomposites; Advanced Composite Materials and Systems; Structural Health Monitoring (SHM); Fracture, Fatigue, and Damage Mechanics; Durability Modeling/Testing; Finite-Element Modeling; Structural Response and Testing; Buckling Mechanics; Project Design and Management; Business Strategy and Growth; Cost Modeling.

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J. White

Using engineering design applications to drive research in simulation and optimization algorithms and software. Focus on fundamentals of nonlinear and parameterized model-order reduction, matrix-implicit methods, and fast techniques for solving integral equations. Applications under investigation include design tools for integrated circuit interconnect, IC inspection, bio-micromachined devices, aircraft, nanophotonics, biomolecule design, and systems biology.

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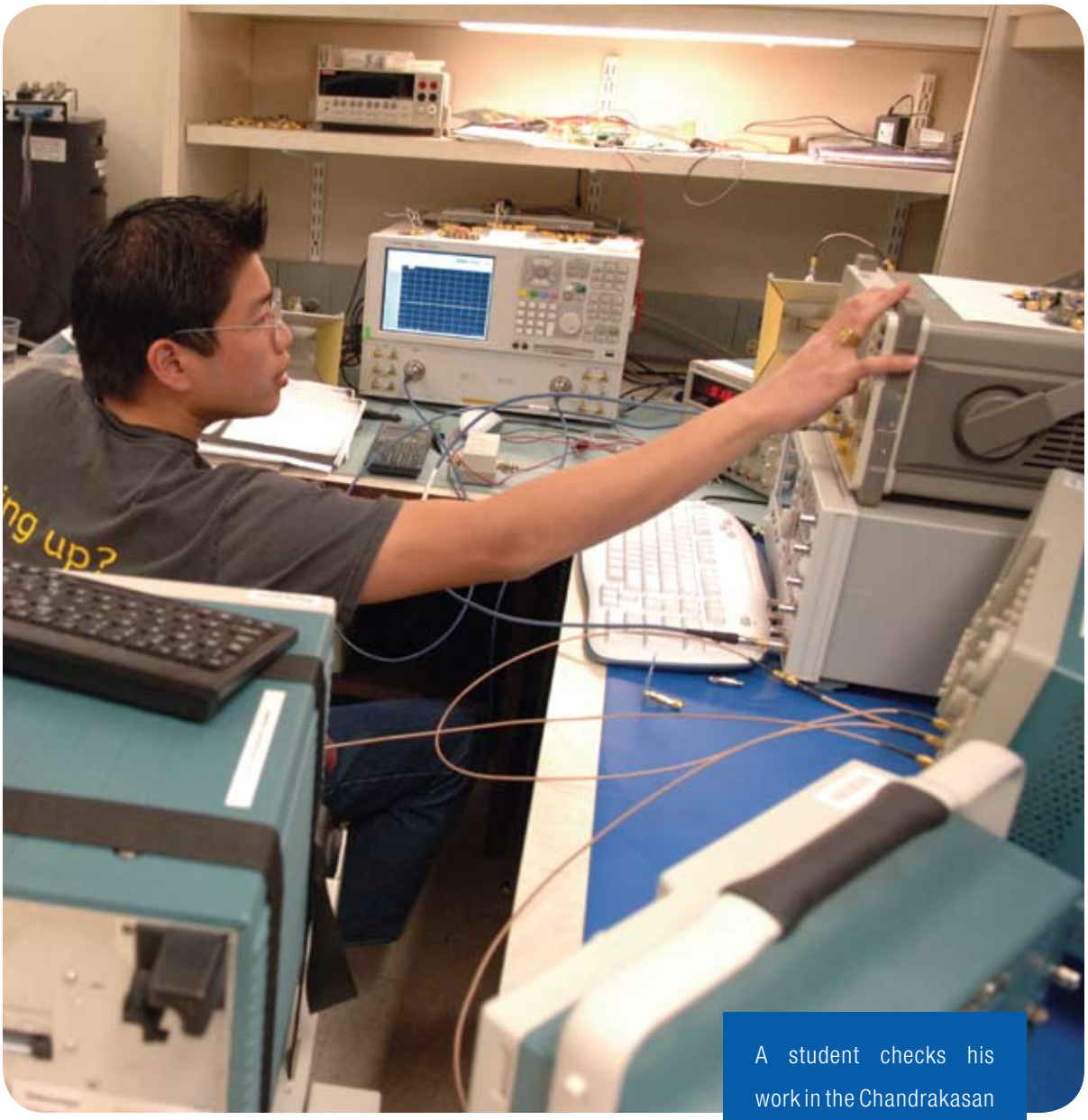

A student checks his work in the Chandrakasan group lab.

CIRCUITS AND SYSTEMS

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A 77 GHz Front-End Receiver for Antenna Arrays

J.D. Powell, C.G. Sodini
Sponsorship: NSF Fellowship, MIT Lincoln Laboratory

SiGe bipolar technologies have proven to be viable candidates for integrated circuits operating at very high frequencies, due to consistently increasing cutoff frequencies of the transistors. While millimeter wave (MMW) integrated circuits have traditionally been implemented in GaAs or InP, the advancement of silicon technologies has recently enabled silicon-based ICs with promising and cost-effective performance in the MMW regime. The most advanced SiGe bipolar transistors now exhibit cutoff frequencies (f_T, f_{MAX}) exceeding 200 GHz, enabling MMW ICs with high levels of integration even between the antenna and front-end radio. Several applications exist for circuits operating in the MMW regime at and above 60 GHz, such as: concealed weapons detection, automotive radar, and high data rate communication systems. Concealed weapons detection is a specific application that improves with increasing frequency due to the distinct difference in radiation between human beings and metals at millimeter wavelengths, which increases the probability of detection. Automotive radar benefits as well from the higher frequency of operation, in that, the spatial resolution is greatly improved over applications at lower frequencies. Another highly useful advantage that comes with radio communication in the MMW regime is the antenna profile. An antenna operating near the silicon interface at 60 GHz on a dielectric such as FR4 requires a length of approximately 1mm. Therefore, an array of 32 x 32 antennas can be fabricated with a small profile of approximately 3 inches^2.

In this research, a 77 GHz front-end receiver will be designed in the IBM 8HP SiGe process for automotive radar applications. The antenna array that will connect directly to the silicon interface will also be designed. Several major circuit design challenges will be encountered at every stage in the front-end receiver, namely: in obtaining a sufficient tuning range in the VCO, achieving sufficient gain in the LNA, and minimizing loading and parasitic capacitance, as it has significant impact on the frequency response of the circuit blocks. The BJT parasitic capacitance also significantly impacts the tuning range of the VCO, since it tends to dominate the varactor capacitance at an oscillation frequency of 77 GHz. This parasitic capacitance will be exploited in the VCO design in order to obtain a superior tuning range. A simple block diagram of the system with the outlining box showing the front end of the receiver is shown in Figure 1 for one of the 1024 antennas that will make up the receiver array. This front-end is part of a typical super-heterodyne receiver with a LO signal of 75 GHz from a fully differential VCO designed for at least a 10% tuning range.

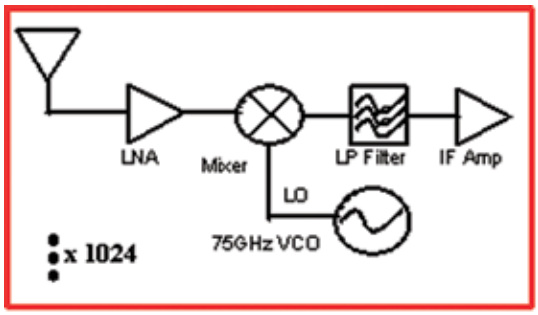

Figure 1: 77 GHz Front-End Receiver Block Diagram

A ΔΣ Direct Digital-RF Modulator

A. Jerng, C.G. Sodini

Sponsorship: Texas Instruments, MIT Center for Integrated Circuits and Systems

This research focuses on the implementation of a direct digital-RF transmitter for use in the Wireless Gigabit Local Area Network (WiGLAN) system that is capable of providing a throughput of 1 Gb/s in the 5.15 – 5.35 GHz U-NII bands. This architecture takes advantage of digital process scaling trends by replacing high dynamic range analog circuits with digital circuits.

In the conventional IQ transmitter depicted in Figure 1, the I and Q signal paths from the DAC to the output of the analog mixer must maintain noise and distortion to levels satisfying the required dynamic range of the system. As the baseband signal bandwidth increases, the analog anti-aliasing filter consumes more power for the same dynamic range. DAC accuracy becomes degraded by dynamic errors at high frequencies rather than static DC errors. Furthermore, as transistors continue to scale and supply voltages continue to decrease, it becomes more challenging to design high dynamic range analog circuits over a wide bandwidth.

Direct digital modulation of an RF carrier can eliminate the DAC, anti-aliasing filter, and analog mixer, resulting in power and area savings. Luschas [1] introduced the RF DAC, which combines a conventional DAC and mixer into one stage. The RF DAC uses one of the high-frequency Nyquist images of the DAC as an RF output. We further develop this concept by modulating an RF carrier using digitally controlled RF phase shifters. In this way, the output power is concentrated at the RF carrier frequency, rather than at DC and at Nyquist image frequencies. Oversampling ΔΣ concepts are applied to convert digital baseband data into a bitstream of +/- 1's, corresponding to phase shifts of 0° and 180°. A 2-level RF phase selector can then be implemented using differential signaling and simple CMOS switches. By applying quadrature RF and baseband components to the phase selectors, we create a quadrature digital modulator capable of arbitrary I-Q modulation, as shown in Figure 2. As the noise shaping transfer function (NTF) of the baseband ΔΣ modulators push their quantization noise outside the signal bandwidth, a bandpass filter at the output can remove the up-converted quantization noise, acting as an RF reconstruction filter.

The new transmitter architecture requires circuit design in both the digital and RF domains. The main challenges include designing a high-speed digital ΔΣ modulator and realizing a high-Q on-chip passive bandpass filter.

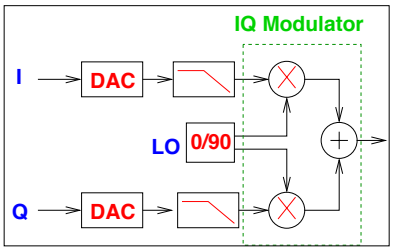

Figure 1: Conventional Transmitter.

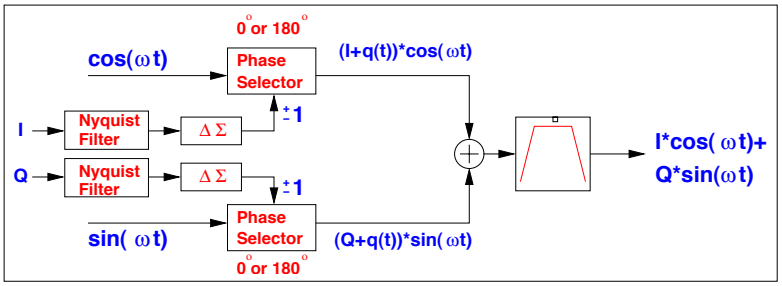

Figure 2: Diagram for an IQ ΔΣ Digital-RF Modulator Block.

REFERENCES:

[1] Luschas, S., R. Schreier, H.S. Lee, "Radio Frequency Digital-to-Analog Converter," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 9, pp. 1462-1467, September, 2004.

Outphase Power Amplifiers for OFDM Systems

A. Pham, C.G. Sodini
Sponsorship: MARCO C2S2

A fundamental trade-off exists between efficiency and linearity among power amplifiers (PAs). Conducting classes such as class-A and -AB offer great linearity, but are very inefficient. On the other hand, switching classes such as class-E and -F have excellent efficiency, but perform poorly in linearity. The outphase amplifying technique allows high-efficiency, non-linear PAs to be used in amplitude-modulated systems that usually require linearity.

Originally proposed by Chireix in 1935, the outphase technique uses a simple trigonometric identity, equation (1), to convert an amplitude-modulated signal into two constant-amplitude, phase-modulated signals, as shown in equation (2). The two constant-amplitude signals can then be amplified using two highly efficient, non-linear PAs. Finally, the outputs are combined to restore the original amplitude-modulated signal. A block diagram is shown in Figure 1.

The outphase technique's practical merit depends largely on the implementation of the amplitude-to-phase conversion box. By implementing this function in the digital domain, we can take advantages of the cheap and vast capability of digital technology. However, the amplitude-to-phase conversion, in general, expands the bandwidth of the original signal. Therefore, the further back we push the conversion from the PAs, the more circuits are affected by bandwidth expansion. In addition, any mismatch in the two outphase paths will cause the combined signal to deviate from the original one and result in transmission errors.

This work studies in detail the advantages and challenges of employing the outphase technique for an OFDM system of multiple QAM sub-channels. The amplitude-to-phase conversion is implemented in the digital domain without extra bandwidth constraints on the transmitter analog circuits. A test chip to demonstrate the concepts also includes an on-chip integrated power combiner at 5.8GHz. In addition, system simulations are conducted to find the distribution of OFDM constellations and the link between mismatch and bit-error-rate.

$$2\cos(b)\sin(a) = \sin(a+b) + \sin(a-b) \quad (1)$$

$$a(t)\sin(\omega t + \theta) = \sin(\omega t + \theta + \phi) + \sin(\omega t + \theta - \phi)$$
$$\phi(t) = \cos\left(\frac{a(t)}{2}\right) \quad (2)$$

Equation List

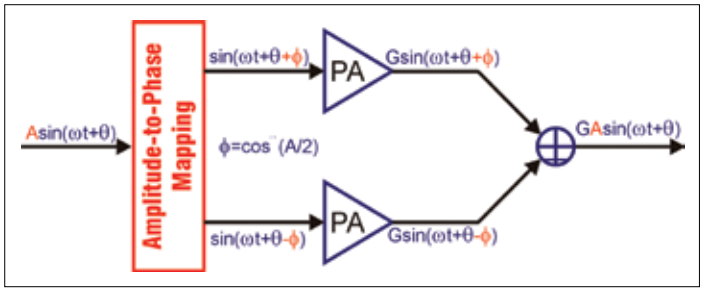

Figure 1: Outphase Amplifying Block Diagram.

Parallel Integrated Receiver Front-Ends for a 5.25 GHz Wireless Gigabit LAN

L. Khuon, C.G. Sodini
Sponsorship: MARCO C2S2, MIT Center for Integrated Circuits and Systems

Wireless systems with arrays of multiple antennas at the transmitter and receiver promise a greatly increased capacity without increasing the required bandwidth. Going from a "single transmit- single receive" antenna (1x1) system to a "four transmit- four receive" antenna (4x4) system potentially quadruples the achievable data rate; however, each antenna requires a separate analog front-end. Putting each front-end on a separate chip is costly as the number of antennas continues to increase. Integration of the parallel RF chains onto a single chip is a cost-effective solution when both total area and DC power consumption for the multiple front-ends do not increase in proportion to the number of antennas.

Using an individual front-end per antenna seems to suggest that the area and DC power consumption increase proportionally with the number of antennas. For example, a receiver with four antennas would consume four times the area and DC power of a one-antenna receiver; however, large SNR gains, available through spatial diversity with multiple antenna systems, can be used in a variety of tradeoffs to minimize area and DC power consumption. One tradeoff applies SNR gain to lower the necessary transmission power. Another uses the SNR gain to relax the noise requirement of the receiver. The relaxed noise requirement allows physically smaller inductor-less circuits to be used [1], while it minimizes DC power consumption by operating circuits at a lower bias current.

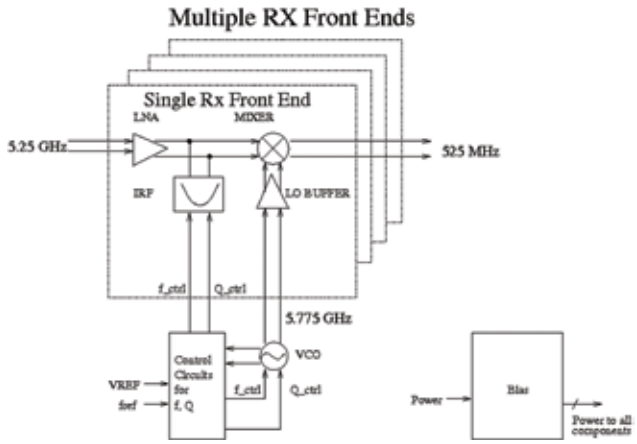

Figure 1: WiGLAN receiver front-ends. Each front-end includes an LNA, image reject filter, mixer, and local oscillator buffer but shares the local oscillator, bias circuits, and filter tuning circuits.

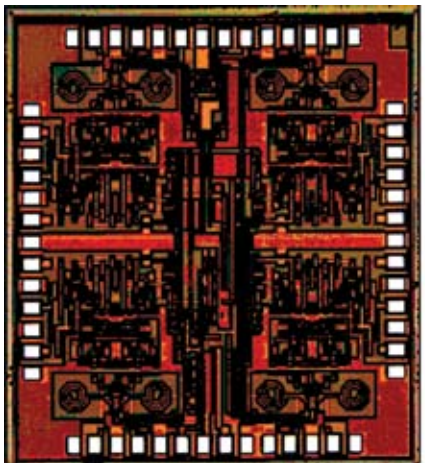

Figure 2: Die photo of a multiple front-ends chip fabricated on IBM 0.18μm SiGe BiCMOS 7WL. The chip consists of four receiver front-ends, a first stage LO buffer, and current mirrors.

REFERENCES:

[1] Khuon, L.., E. Huang, C.G. Sodini, and G. Wornell, "Integrated Transceiver Arrays for Multiple Antenna Systems," in *Proceedings of IEEE Vehicular Technology Conference (VTC) , Spring*, Stockholm, Sweden, May 2005.

Realization of the Baseband DSP Core for the Wireless Gigabit LAN

J.K. Tan, C.G. Sodini
Sponsorship: NSF

In the development of wireless standards, the use of the Orthogonal Frequency Division Multiplexing (OFDM) is becoming increasingly pervasive. The Wireless Gigabit LAN (WiGLAN) aims to achieve a high data rate of 1 Gbps through the utilization of OFDM technology in combination with a wide bandwidth of 150 MHz. The high data rate motivates the need to realize the DSP Core in hardware and test its functionality in real-time.

The hardware platform is a Field Programmable Gate Array (FPGA) because it offers programmability and the capability to tradeoff hardware resources for speed. However, even with an FPGA, the implementation of the DSP Core is challenging, because of limited hardware resources and tight real-time requirements. Due to these constraints, the algorithms used in the DSP Core have to be programmed for minimal complexity; algorithms with high complexity take more hardware resources and lengthen the execution time. After the DSP Core has been realized in hardware, 2 PCs are connected to the DSP Core via PCI to perform high-speed transmission.

The goal is to demonstrate a prototype of the WiGLAN's communication system in which the realized DSP Core will be integrated with the RF Front-End. This test prototype is the primary vehicle for the performance evaluation of the system. The many uses of this prototype include: determining the role of DSP algorithms in mitigating RF imperfections and characterizing the 5-GHz indoor wireless channel.

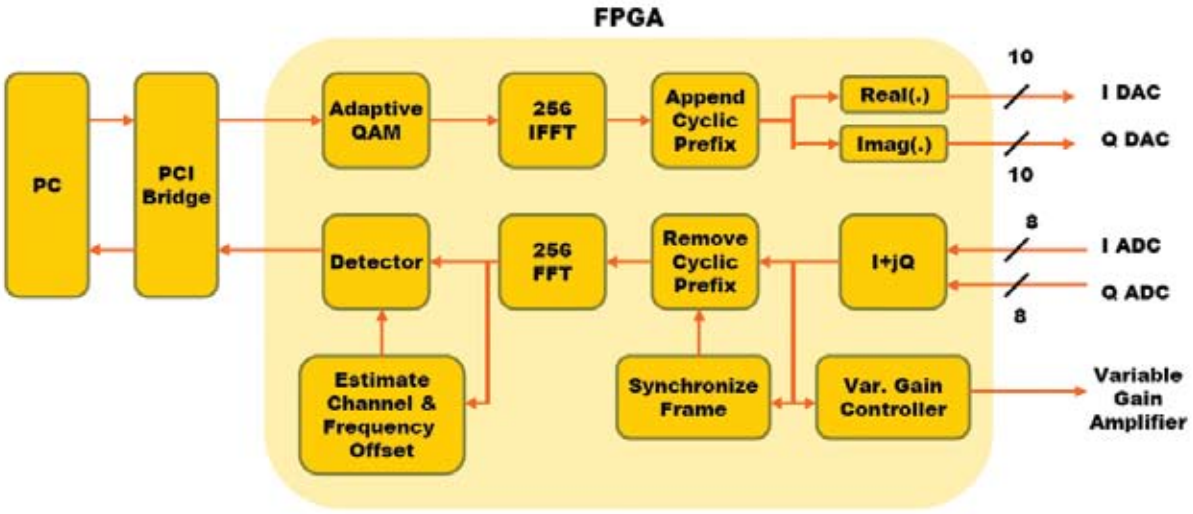

Figure 1: Block diagram for the baseband transceiver to be interfaced with the RF Front-End.

An Implementation of a 5.25GHz-Transceiver for the Wireless Gigabit LAN

N. Matalon, K.M. Nguyen, C.G. Sodini
Sponsorship: NSF

Though the transmission data rate of wireless LAN systems has increased significantly over the past few years with standards today allowing for up to 54 Mbit/s, higher rates are still sought after for a variety of applications. The focus of the Wireless Gigabit LAN (WiGLAN) project is the design of a system capable of transmitting data up to 1Gbit/s. This transmission can be achieved with an OFDM architecture using 150MHz of bandwidth, adaptive modulation per bin, and multiple antennas. This work focuses on the discrete design of the RF front-end used to transmit and receive OFDM symbols already created.

The challenge involves successfully transmitting information through a wireless indoor channel while minimizing noise, non-linearity effects, and other system non-idealities. Furthermore, the system should accommodate signal bandwidths up to 150MHz, and operate in the 5.25 GHz band. Low noise figure is desired for increased receiver sensitivity, and linearity must be carefully monitored due to the multi-carrier nature of the system. Other issues addressed include: 5 GHz impedance matching, preserving gain flatness, synthesizing low spur and low phase noise carriers, and ensuring proper high-speed data conversion.

The design is implemented on a printed circuit board and uses the most advanced RF and mixed-signal commercial components. These include: 5 GHz LNAs, filters and mixers; high bandwidth I/Q modulators and demodulators, low-noise variable-gain amplifiers, and high speed (> 250MSPS) 8-10 bit data converters. The synthesis of data converter clocks is also required. Though issues such as power consumption and board area are important and hence, motivate the design of completely integrated systems, this design places a secondary emphasis on these issues and focuses on the implementation of a functioning prototype that will enable the characterization of the wireless channel.

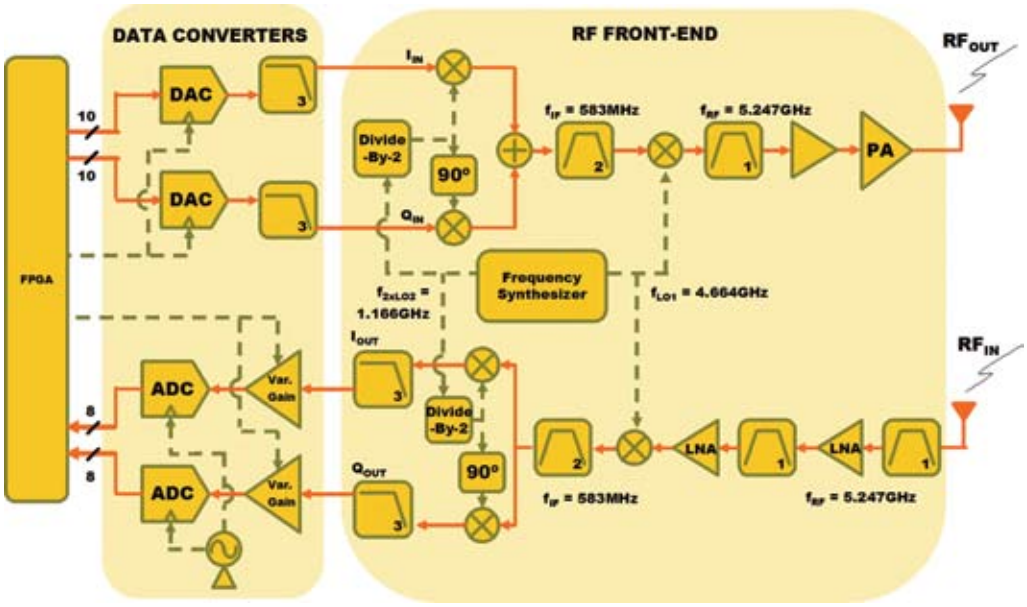

Figure 1: Schematic of a single WiGLAN Transceiver node. Two printed circuit boards are used for the data converters and RF front-end.

Optimization of System and Circuit Parameters in Wideband OFDM Systems

F. Edalat, C.G. Sodini
Sponsorship: NSF, Texas Instruments

In the Wireless Giga-bit Local Area Network (WiGLAN) research effort, the goal is to achieve Giga-bit data rates by methods fundamentally different from the proposed IEEE 802.11n, next-generation WLAN. In other words, instead of using multiple antennas as multiplexing to increase the capacity, WiGLAN uses a much wider bandwidth (150 MHz compared to 20 MHz) and adaptive modulation per bin of a multi-carrier system. However, both systems employ Orthogonal Frequency Division Multiplexing (OFDM) to combat inter-symbol interference from multipath fading of the indoor channel and to eliminate equalization. We have simulated the WiGLAN system using CppSim, which is a time-step behavioral simulation tool that uses C++ as the language code for higher flexibility and faster simulation time [1]. The wideband characteristic of WiGLAN, while enabling high throughput, imposes several challenges. The system simulation is used as one of the initial steps to identify such challenges and to examine the effects of circuit and system parameter choices on the high data rate wideband OFDM signal. With the aid of system simulation, optimum system solutions and circuit design techniques will be investigated. For instance, we are investigating various adaptive modulation techniques to choose the most appropriate one for such systems and use simulation to test our proposed adaptive modulation algorithms

In such multi-carrier systems with a frequency-selective channel, higher capacity can be obtained by adapting modulation of each subcarrier to the channel response over its band (Figure 1). The modulation per bin is selected (Figure 2), based on the estimated Signal-to-Noise ratio (SNR) per bin at the input of detector at the receiver and the target Bit-Error-Rate (BER) of the overall system performance. However, due to high overhead delays for transmitting the information required to perform such modulation selection among four types for each bin, we are investigating other variants of adaptive modulation that will be more practical to implement.

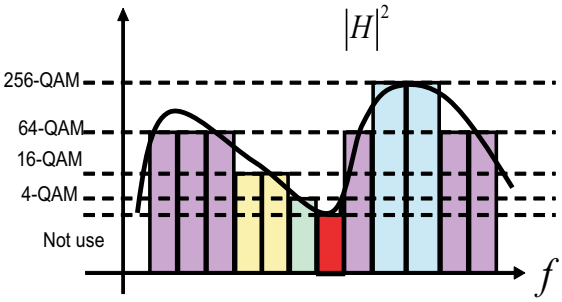

Figure 1: Adaptive modulation per bin in WiGLAN based on the channel response over each bin. The modulation scheme is chosen from 4-, 16-, 64-, and 256-rectangular QAM modulations.

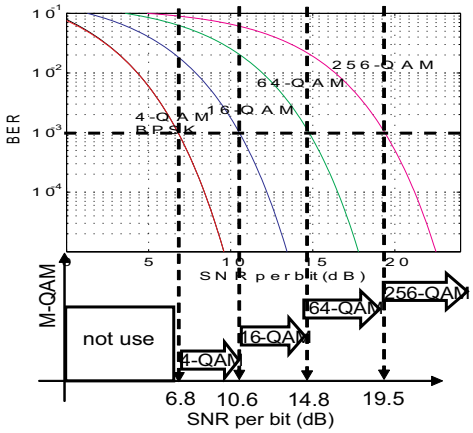

Figure 2: How adaptive modulation algorithm dictates the modulation scheme for each bin in WiGLAN.

REFERENCES:

[1] Perrott, M., CppSim Behavioral Simulator: [Online document], Available HTTP: http://www-mtl.mit.edu/researchgroups/perrottgroup/tools.html.

Low-Power, High-Speed Analog-To-Digital Converters for Ultra-Wideband Application

A. Chow, H.-S Lee

Sponsorship: MARCO C2S2, MIT Center for Integrated Circuits and Systems

With the emergence of the Ultra-Wideband (UWB) wireless communication and the general versatility of digital signal processing, wireless systems have demanded higher speed ADC's. This thesis investigates topologies to reach these higher speeds. In particular, this work will design a 20-giga-sample per second with six effective bits in a 0.18-CMOS technology. The requirement for power efficiency further constrains the design. A time-interleaved architecture is explored as a means to optimize the power dissipation for a given speed (Figure 1). Preliminary design calculations indicate that the optimal total power occurs with massive time interleaving, on the order of several hundred channels. The two main design considerations for such a large parallel system are matching between the channels, and the generation and distribution of the several hundred clock phases. This work looks at various means of performing digital background calibration to account for the mismatches between the ADC's. Several methods for generating and distributing a large number of clock phases are investigated, including the use of transmission lines. Although this ADC will be applied to the UWB applications, the conclusions and results from this work can apply to general high-speed ADC design or general time-interleaved systems.

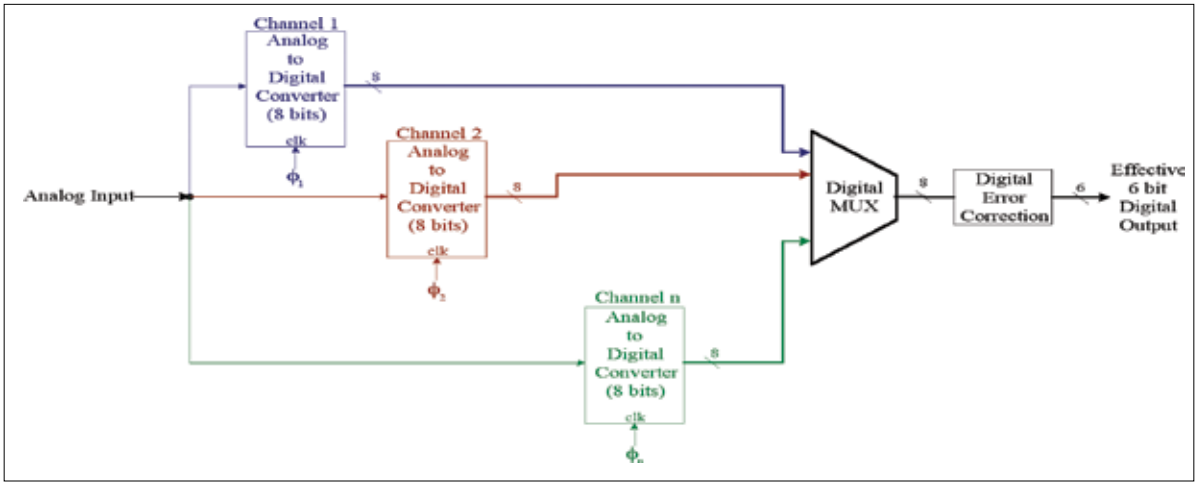

Figure 1: Time interleaved ADC topology. Each individual ADC is clocked with a different phase, which time division multiplexes the input signal. Therefore, it allows the overall time-interleaved ADC to operate n times faster than each individual ADC.

A Pulsed-Based, Ultra-Wideband Transmitter

D.D. Wentzloff, A.P. Chandrakasan
Sponsorship: HP-MIT Alliance, NSF

This research focused on an ultra-wideband (UWB) transmitter fabricated in a 0.18-µm SiGe BiCMOS process that uses a tanh-shaping technique to generate approximate Gaussian pulses in the 3.1-10.6-GHz band. The MIT UWB architecture uses pulse-based, binary phase-shift keyed (BPSK) communication in which information is encoded as a pulse with either positive or negative polarity [1]. This transmitter generates a baseband pulse train and up-converts it to one of 14 non-overlapping channels in the 3.1-10.6-GHz UWB band. A separate receiver down-converts and digitizes the pulses. During acquisition, the digital back-end learns the pulse shape, and under the assumption that BPSK pulses are matched, the back-end uses the learned pulse and its inverse when performing correlation. For this reason, amplitude and timing matching between positive and negative pulses generated by the transmitter are critical to the quality of service. The goal of this work was to design a low-power UWB transmitter that emits well-matched, BPSK Gaussian shaped pulses due to their desirable frequency response. By exploiting the exponential behavior of a BJT, the Gaussian pulse can be accurately approximated with an elegant analog circuit that simultaneously performs up-conversion mixing [2]. The transmitter uses a differential pair with a triangle signal input to generate and shape a pulse of one polarity. For the proper triangle input signal, the output current will have a shape that approximates that of a Gaussian pulse. If the bias current of the differential pair is modulated with a tunable local oscillator (LO), the pulse can be simultaneously up-converted to the UWB band. The BPSK modulation is performed by using two pulse generators in parallel, where the LO in each is 180 degrees out of phase. A block diagram of the complete transmitter appears in Figure 1. The transmitter was fabricated in a 0.18-µm SiGe BiCMOS process, and near-Gaussian pulse generation in the UWB band has been demonstrated. A die photo is shown in Figure 2. The total DC power consumption of the PA, mixer, and LO buffering was 31.3 mW.

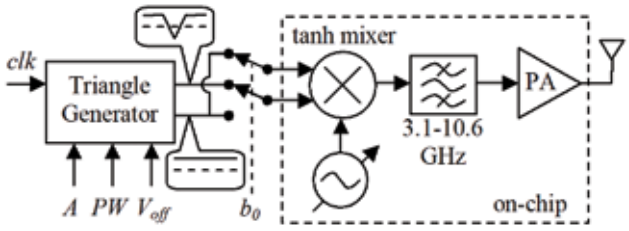

Figure 1: Block diagram of the UWB transmitter showing on-chip and off-chip components.

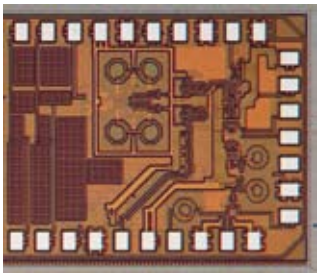

Figure 2: Die photograph of the transmitter chip.

REFERENCES:

[1] Blazquez, R., *et al.*, "A Baseband Processor for Pulsed Ultra-Wideband Signals," *IEEE Custom Integrated Circuits Conference*, October 2004.
[2] Wentzloff, D.D., A.P. Chandrakasan, "A 3.1-10.6 GHz Ultra-Wideband Pulse-Shaping Mixer," *IEEE Radio Frequency IC Symposium*, June 2005.

An Ultra-Low-Power Digital Baseband for a Pulsed Ultra-Wideband Transceiver Using Extreme Parallellization

V. Sze, R. Blázquez, A.P. Chandrakasan
Sponsorship: NSF

Following the developments in UWB communications in the recent years, it has become clear that in order to achieve large data rates in multipath environments, a very complex digital baseband must be used to recover the UWB signal, particularly in the case of long data packets. Of the two IEEE standards currently under development that use UWB signals, this project focuses on the second one, IEEE 802.15.4a.

UWB communications are allowed in the 3.1 GHz to 10.6 GHz band with a maximum Equivalent Isotropic Radiated Power of -41.3 dBm/MHz. In this bandwidth, the signal is affected by both an intense multi-path and in-band interferers. Figure 1 shows an example of channel impulse response with an RMS delay of 25 ns based on a modified Saleh-Valenzuela model as recommended by IEEE standard group 802.15.3a.

For this implementation, the metric to optimize is the total energy dissipated to demodulate a very short packet. This optimization can be achieved by using extensive parallelization to reduce the length of the required preamble and also to minimize the clock frequency of the digital circuits. The architecture shown in Figure 2 will be used.

This transceiver will be designed to deliver a maximum of 100Mbps using a minimum bandwidth of 500MHz in a 10m-channel for data packets shorter than 500 bits. These specifications make it attractive for sensor networks. An average power of 1mW would be desirable.

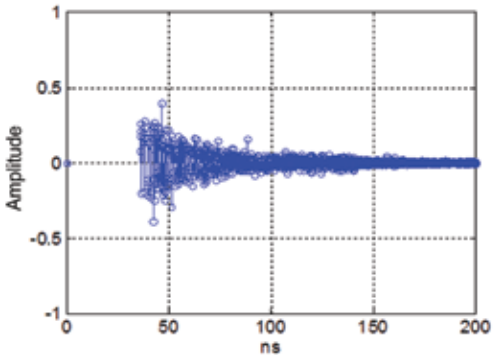

Figure 1: Example of multipath impulse response.

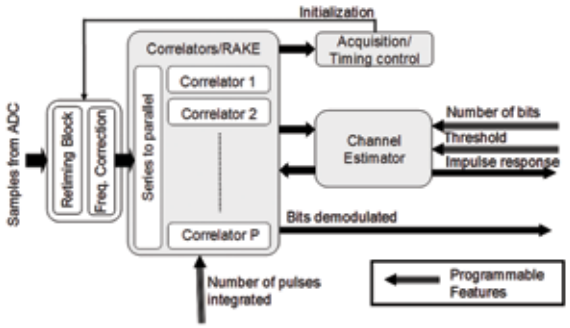

Figure 2: System level diagram of UWB digital baseband.

REFERENCES:

[1] Foerster, J., "Channel Modeling Sub-Committee Report Final", IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs). February, 2002.

[2] Blázquez, R., A. Chandrakasan, "Architectures for Energy-Aware Impulse UWB Communications", *International Conference on Acoustics, Speech, and Signal Processing,* 2005.

Ultra-Wideband Baseband and RF Front-ends in SiGe BiCMOS and CMOS

F.S. Lee, A.P. Chandrakasan
Sponsorship: NSF, HP-MIT Alliance

The FCC recently approved ultra-wideband (UWB) radio, an emerging technology, to operate in the 3.1-10.6GHz band at a low EIRP of -41.3dBm/MHz. This type of wideband, low-power signaling fits well with the trends of increasing transition frequency and decreasing breakdown voltages of ever-advancing deep sub-micron processes. The large bandwidth allows for high-rate wireless data transfer in the vicinity of 100Mbps to 1Gbps. However, because of the large bandwidth, UWB receivers are also susceptible to front-end saturation by strong in-band narrowband interferers. Effectively harnessing the potential of this unlicensed band requires exploring new RF circuits and systems that can handle large bandwidths, mitigate the dynamic range issues, and afford lowest power operation through adaptability and control in conjunction with a digital back-end. A 1GHz baseband UWB front-end has been implemented in CMOS [1].

Results from [1] were leveraged, and a 3-10GHz UWB receiver was designed in SiGe BiCMOS. Figure 1 shows the block diagram of the current implementation. Due to the large bandwidth of UWB signals, a direct-conversion receiver is best suited to recover the signal. This receiver is designed for 500MHz sub-banded pulsed-UWB signals. The front-end consists of a UWB low-power LNA, a post-LNA on-chip channel-select RF filter, active RF single-to-differential converter, a -10dB 5GHz ISM band switch-able notch-filter, two 3-10GHz LO amplifiers, mixers, and base band channel-select filters and buffers. The chip consumes 50mW of power, provides a double sideband noise figure (NF) of less than 3dB across most of the UWB bandwidth from RF to base band, achieves an overall fully differential conversion gain of 30dB, and has an RF input P1dB of -30dBm which accommodates the dynamic range of UWB signals and the assumed subset of sinusoidal interferers given by IEEE TG802.15.3a [2]. Figure 2 shows the layout of the chip.

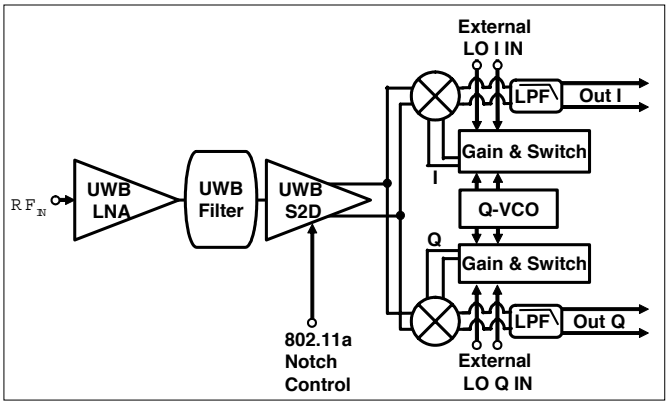

Figure 1: Block diagram for UWB receiver.

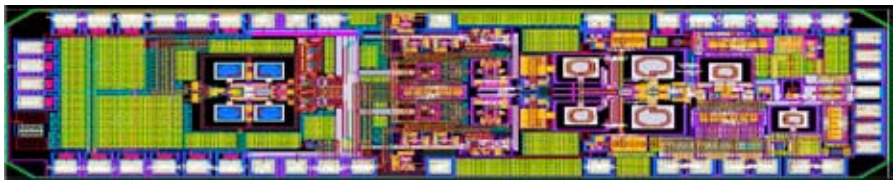

Figure 2: Layout for UWB receiver.

REFERENCES:

[1] Lee, F.S., D.D. Wentzloff, A.P. Chandrakasan, "An Ultra-Wideband Baseband Front-End", *IEEE Radio Frequency Integrated Circuits Symposium*, June 2004.

[2] Foerster, J. *et al.*, "IEEE P802.15 Wireless Personal Area Networks," IEEE document P802.15-02/368r5-SG3a.

Deep Sub-Micron CMOS Analog-To-Digital Conversion for Ultra-Wideband Radio

B.P. Ginsburg, A.P. Chandrakasan
Sponsorship: HP-MIT Alliance, NSF, NDSEG Fellowship

Ultra-wideband (UWB) radio uses low signal power spread over a very wide bandwidth and has the potential to transmit at very high data rates over short distances. The minimum FCC-compliant bandwidth of 500MHz occupies 250MHz at DC; Nyquist sampling requires a 500MSample/s analog-to-digital converter (ADC). It has previously been shown that only 4 bits of resolution are sufficient for proper reception in both noise- and interference-limited regimes [1].

A flash ADC is the typical topology used for these specifications. The principal drawback of flash converters is the exponential scaling of comparators versus resolution. Another approach is a time-interleaved successive approximation register (SAR) ADC [2]. A SAR requires only b comparisons, to resolve the b-bit digital output, which can lead to significant savings; however, a SAR suffers from a large input capacitance and high digital complexity. Figure 1 presents a theoretical comparison between flash and SAR energy requirements.

A 500MSample/s, 5b, 6-way time-interleaved SAR converter has been fabricated in 0.18µm CMOS technology. We acknowledge National Semiconductor for providing the fabrication services. A die photograph is shown in Figure 2. We are currently developing new circuit techniques [3] and exploring the usage of a larger number of time-interleaved slices to save energy. A further area of research is using deep sub-micron technology to both reduce the power supply and give substantial savings on the digital energy; these scaled technologies present their own challenges, including larger process variation and component mismatch.

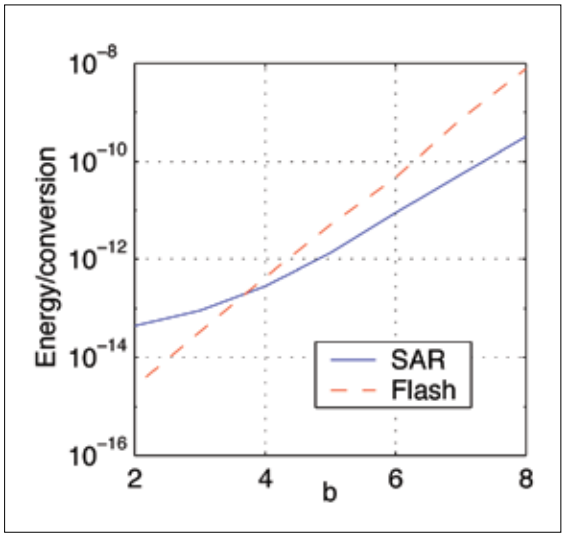

Figure 1: Model showing how the energy/conversion scales in a SAR and flash ADC versus resolution.

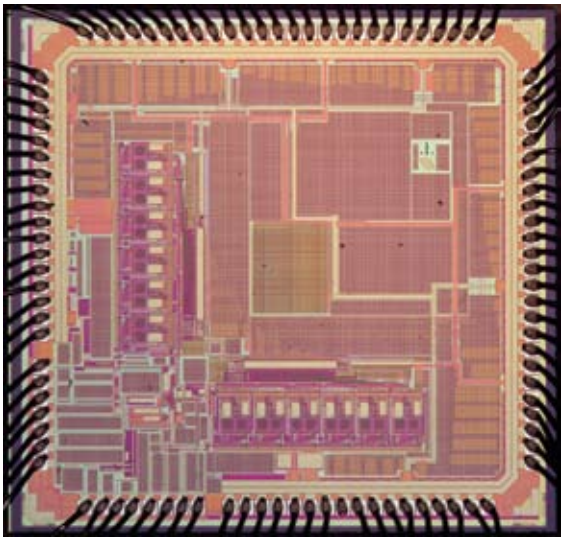

Figure 2: Die photograph of a chip containing dual, 500MSample/s 5b ADC.

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Low-Power RF Transceiver Modeling and Design for Wireless Microsensor Networks

A.Y. Wang, C.G. Sodini

Sponsorship: MIT Center for Integrated Circuits and Systems

The design of wireless microsensor systems has gained increasing importance for a variety of civil and military applications. With the objective of providing short-range connectivity with significant fault tolerance, these systems find usage in such diverse areas as: environmental monitoring, industrial process automation, and field surveillance. The main design objective is to maximize the battery life of the sensor nodes while ensuring reliable operations. To achieve this goal, the microsensor node must be designed in a highly integrated fashion and optimized across all levels of system abstraction.

A block diagram of a microsensor node appears in Figure 1. For micro-sensor networks, the RF transceiver dominates the power consumption. A system energy model is developed to take into account the effect of both communications protocols and power consumption of transceiver circuit. Using this model, it is determined that a significant fixed energy cost is associated with short-range giga-Hertz transceivers. This fixed cost comes from the RF building blocks required to perform up and down conversions. The battery life of the microsensor node can be improved significantly by increasing the data rate, reducing the start-up time, and improving the PA efficiency, as Figure 2 shows. Increasing the data rate drives down the fixed energy cost of the transceiver. Reducing the start-up time decreases the start-up energy overhead. Improving the PA efficiency lowers the energy/bit cost of the power amplifier.

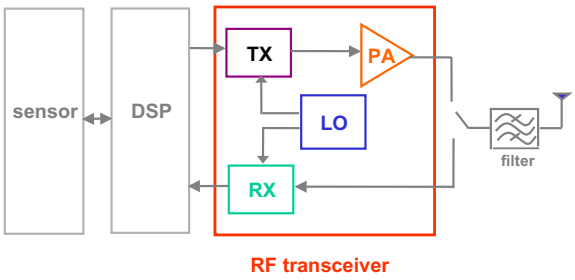

Figure 1: Microsensor node architecture. The RF transceiver dominates the power consumption.

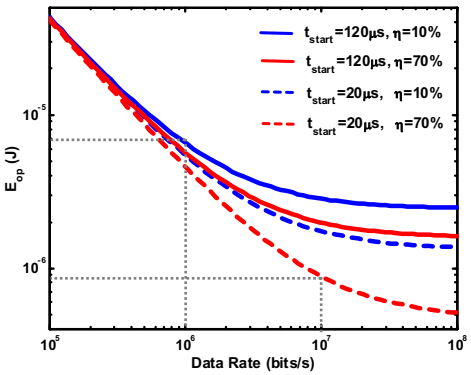

Figure 2: At low data rate, fixed cost dominates transceiver energy. At high data rate, start-up and PA energy dominate. The t_{start} is the start-up time and η is the PA efficiency.

An Ultra Low-Power ADC for Wireless Micro-Sensor Applications

N. Verma, A.P. Chandrakasan
Sponsorship: DARPA Power Aware Computing/Communication Program

In micro-sensor nodes, an analog-to-digital converter (ADC) is used to acquire target data from the environment. In an effective network, individual nodes are autonomous to enable long-term operation with no maintenance. This implies that they would, ideally, power themselves using energy harvested from the field: a generally erratic power source. Further, the ADC, composing the front end of the sensor system, is subject to dynamically varying requirement specifications due to the unpredictable environment.

As a result, a robust ADC design for low-power sensor networks should not operate statically under the assumption of worst-case environmental conditions. The ability to compromise features and performance in favor of reduced power consumption is a necessary characteristic. Additionally, because sensor nodes are typically reactive, the ADC cannot leverage sleep modes and duty cycling to the extent that back-end circuitry can; the ADC must remain on in some capacity at all times. This implies that improvements on ADC efficiency (figure of merit) are required to enable ultra low-power nodes.

This ADC has a sampling rate between 0 and 100kS/s and a resolution of either 12 bits or 8 bits. The architecture selected is the successive approximation register (SAR), which is suitable for micro-power operation due to its limited number of active components. A block diagram of the ADC is shown in Figure 1, and a die photograph is shown in Figure 2. Optimizations are made at both the circuit and architecture levels to achieve scalability and improved efficiency.

The chip was fabricated in a 0.18µm CMOS technology. We acknowledge National Semiconductor for providing the fabrication services.

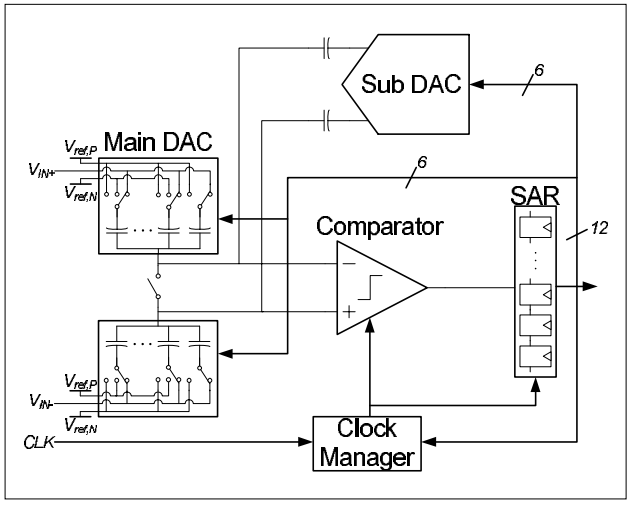

Figure 1: System block diagram of low-power SAR ADC.

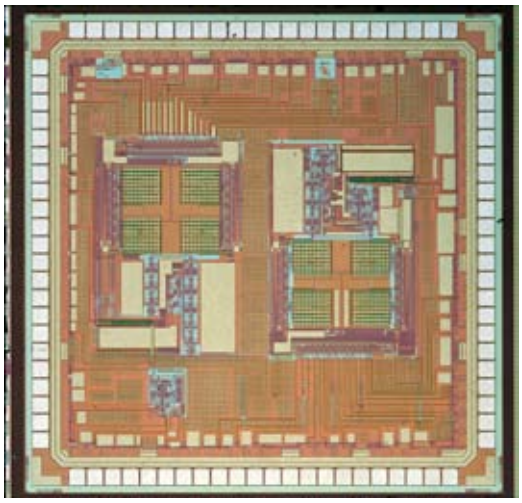

Figure 2: Die photograph of fabricated test chip.

A Micropower DSP Architecture for Self-Powered Microsensor Applications

N. Ickes, D. Finchelstein, A.P. Chandrakasan
Sponsorship: DARPA Power Aware Computing/Communication Program

Distributed microsensor networks consist of hundreds or thousands of individual, miniature sensor nodes. Each node individually monitors the environment and collects data as directed by the user, and the network collaborates as a whole to deliver high-quality observations to a central base station. The large number of nodes in a microsensor network enables high-resolution, multi-dimensional observations and fault-tolerance that are superior to more traditional sensing systems. However, the small size and highly distributed arrangement of the individual sensor nodes make aggressive power management a necessity.

The aim of the µAMPS-2 project is to build a highly integrated, yet versatile sensor system with a strong focus on energy efficiency and agility. Tracking the optimal operating point in the dynamic environments typical for sensor networks requires hardware that can vary clock rates, power supply voltages, and other circuit parameters on-the-fly. The µAMPS-2 architecture consists of a micropower DSP, surrounded by dedicated accelerator blocks for functions performed frequently by each sensor node: FFTs, FIR filters, error correction coding and decoding, and data encryption. A DMA engine efficiently moves data between the DSP and these accelerator blocks. This architecture of highly optimized, on-demand hardware support for energy intensive tasks allows for ultra low-power data manipulation and lowers the processing burden on the DSP core.

An initial implementation of the µAMPS-2 architecture was fabricated in a 0.18µm CMOS technology. We acknowledge National Semiconductor for providing the fabrication services. This implementation included the 16-bit DSP core, an FFT accelerator, and interfaces to custom ADC and radio chips. The fabricated chip operates correctly down to a supply voltage of 0.5V, consuming only 110µW. If the clocks are turned off, the chip can retain its full state using as little as 26µW.

A second-generation µAMPS-2 system is planned, which will improve upon its predecessor by incorporating extensive power-gating, enabling dynamic voltage scaling and shutdown of all individual accelerator cores. The logic will also be designed for sub-threshold operation, resulting in further reduction of signal switching energy.

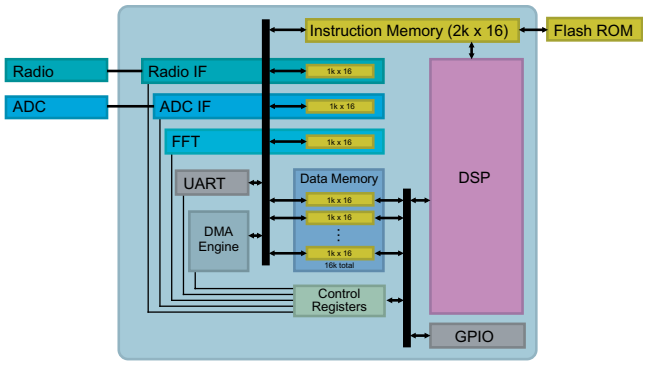

Figure 1: The µAMPS-2 DSP architecture.

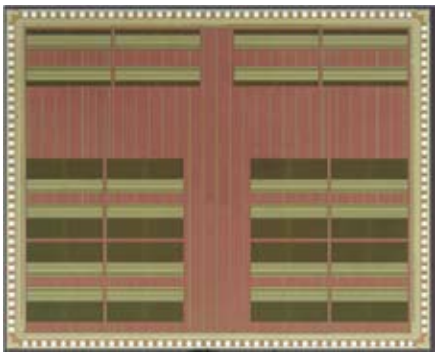

Figure 2: Die photo of first-generation DSP chip.

An Energy-Efficient RF Transceiver for Wireless Sensor Networks

D.C. Daly, A.P. Chandrakasan
Sponsorship: DARPA Power Aware Computing/Communication Program

Large-scale wireless sensor networks require a low-power, energy-efficient transceiver that can operate for years on a single battery. To meet this demand for microwatt average power consumption, the transceiver must be scalable, support duty cycling, and be energy-efficient when "on". Traditional cellular systems place a high value on bandwidth efficiency and thus use efficient modulation schemes like Gaussian Minimum Shift Keying (GMSK) and Differential Quadrature Phase-Shift Keying (DQPSK). A drawback to these modulation schemes is that they typically result in greater transceiver power consumption than modulation schemes like on-off keying (OOK) or frequency shift keying (FSK). For wireless sensor networks in which power consumption is a more important design consideration than bandwidth efficiency, OOK and FSK can be used to implement a simpler (and more energy efficient) transceiver.

We propose using OOK modulation to enable the use of a rectification-based, energy-efficient receiver. Figure 1 shows the architecture of the proposed transceiver. A key design decision for the OOK receiver is how to implement the rectifier. Super-regenerative receivers use an oscillator that is periodically quenched for envelope detection. This approach uses positive feedback and contrasts with the more common voltage- or current-mode rectifiers. The quench rate for a super-regenerative receiver must scale in proportion to the data rate. Hence, at high data rates, continuous voltage-mode or current-mode rectifiers become more practical. The OOK transmitter consists of an oscillator, a mixer, and a power amplifier. The transceiver layout appears in Figure 2.

The chip was fabricated in a 0.18μm CMOS technology. We acknowledge National Semiconductor for providing the fabrication services.

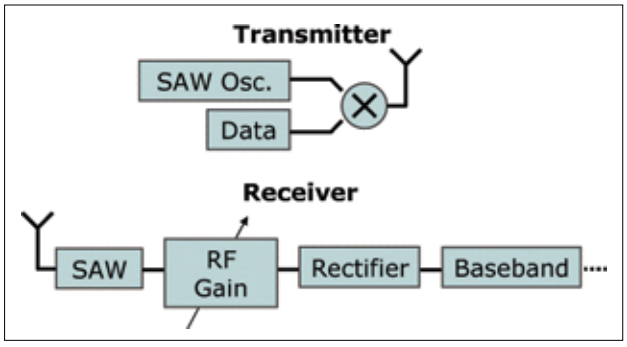

Figure 1: Architecture of the OOK transceiver

Figure 2: Chip layout of the OOK transceiver

Biasing Techniques for Sub-Threshold MOS Resistive Grids

K.H. Wee, J.J. Sit, R. Sarpeshkar

Spatial filtering circuits used in image processing are often implemented using resistive networks [1][2]. A key element of silicon retinas is a diffusion network comprising an array of lateral and shunt conductances. Spatial filters are also useful for distributed gain control in silicon cochleae [3]. Linear resistive networks using passive resistors are hard to implement in a small area in CMOS-integrated circuits and are not amenable to electronic control. Bi-directional resistive networks can be implemented with MOS transistors whose source and drain terminals are symmetrical and whose gate or bulk voltages may be varied to provide electronic control of the space constant.

Previously proposed current-mode MOS-resistive networks have the following properties: (a) Gate-to-bulk voltages (V_{GB}) are not constant and consequently, the space-constant of the network varies with the common mode in an uncontrolled fashion even as the differential voltage between lateral and shunt transistors is fixed; (b) Bulk-to-source voltages (V_{BS}) are input-dependent and consequently a MOS-resistive grid exhibits non-linear operation due to the variation of the sub-threshold exponential parameter κ with V_{BS}. As a result, prior approaches to building resistive grids with MOS transistors resulted in networks whose space-constant varied with the gate-to-bulk voltage and input current intensity. We propose two biasing techniques that alleviate these effects in a current-mode MOS-resistive grid. The first maintains a constant V_{GB} for all transistors in the network regardless of common mode. The second technique suppresses non-linearity due to the body effect induced by varying input currents. Figure 1 shows a photomicrograph of a test-chip fabricated in a 1.5-μm CMOS process. An on-chip capacitive current integration technique is used to obtain precise measurements of sub-threshold currents down to 1fA [4]. Figure 2 shows the measured impulse response of our spatial filter.

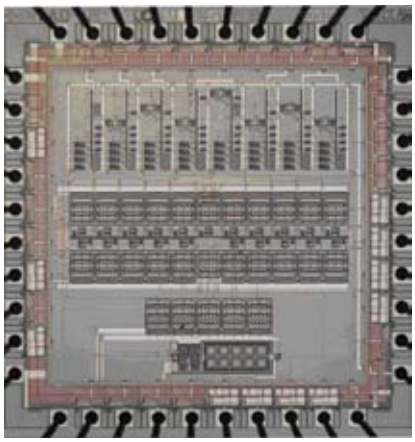

Figure 1: Microphotograph of test-chip with on-chip current measurement.

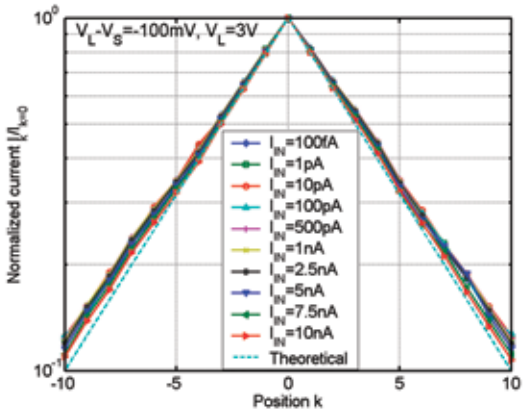

Figure 2: Measured spatial impulse response of new resistive grid at varying input current intensities (100fA<I_{IN}<10nA).

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[4] O'Halloran, M., R. Sarpeshkar, "A 10-nW 12-Bit Accurate Analog Storage Cell with 10-aA Leakage," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1985-1996, November 2004.

An Analog Bionic Ear Processor with Zero-Crossing Detection

R. Sarpeshkar, M. Baker, C. Salthouse, J.J. Sit, L. Turicchia, S. Zhak
Sponsorship: Packard Foundation

Deaf patients with more than 70dB-80dB of hearing loss cannot use a hearing aid and require a cochlear implant. The implant stimulates the auditory nerve with electrical current using 8-20 electrodes surgically implanted in the patient's cochlea. The stimulation is coded such that logarithmic spectral-energy outputs of an audio filter bank are topographically mapped to the electrode array. For programmability, cochlear implant processing has been done mostly in the digital domain by digitizing the output of a microphone front-end and feeding it to a DSP. However, the microphone front-end, A/D converter, and DSP consume a few mW of power even in very power-efficient systems. In this paper, we report a chip that implements most of the cochlear implant processing in the analog domain and delays digitization to the very end to achieve a power consumption of 251μW, while still leaving room for 750 μW of stimulation power.

In the future, an entire cochlear implant will be fully implanted inside the body of the patient and will be required to run on a 100-mAh battery with, at most, 1000 wireless recharges and no battery replacement for, at least, 30 years. This power consumption of this chip is lower than state-of-the-art A/D-then-DSP designs by a factor of 20, and thus, is able to meet the fully-implantable power requirements. The use of analog processing to substantially reduce power in portable systems of moderate complexity appears to be an emerging technology direction, for example, in a recently reported hearing-aid processor [1].

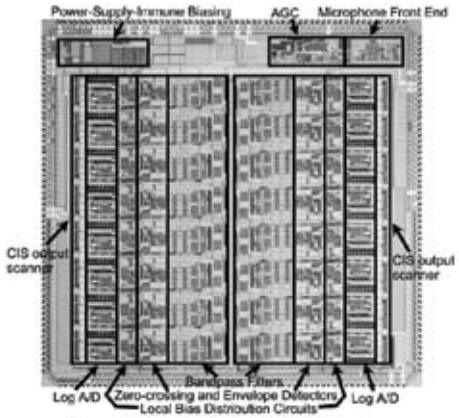

Figure 1: Die micrograph of the chip showing the various system blocks.

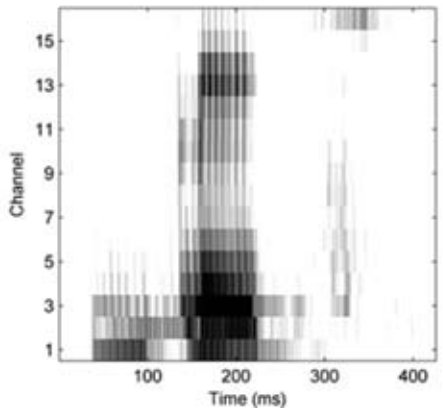

Figure 2: Spectrogram-like plots for the word /bit/. Amplitude outputs from the chip are used to construct a spectrogram.

REFERENCES:

[1] Serra-Graells, F., L. Gomez, and J.L. Huertas, "A True 1V, 300μW, CMOS Sub-Threshold Log-Domain Hearing-Aid-On Chip," *IEEE Journal of Solid State Circuits,* Vol. 39, No. 8, pp. 1271-1281, 2004.

A 10-nW, 12-Bit Accurate Analog Storage Cell with 10-aA of Leakage

M. O'Halloran, R. Sarpeshkar

Sponsorship: Center for Bits and Atoms NSF Research Grant, Office of Naval Research, Catalyst Foundation, Packard Foundation, Swartz Foundation

Medium-term analog storage offers a compact, accurate, and low-power method of implementing temporary local memory that can be useful in adaptive circuit applications. The performance of these cells is characterized by the sampling accuracy and voltage droop that can be achieved with a given level of die area and power. Hand calculations suggest past implementations have not achieved minimum voltage droop due to uncompensated MOS leakage mechanisms. In this research, the dominant sources of MOS leakage were experimentally characterized in a standard 1.5-µm CMOS process using an on-chip current integration technique, focusing specifically on the 1fA-to-1aA current range. These measurements revealed an accumulation-mode source-drain coupling mechanism that can easily dominate diode leakage under certain bias conditions, and may have limited previous designs. A simple rule-of-thumb is offered for avoiding this leakage effect, leading to a novel ultra-low leakage switch topology. A differential storage cell incorporating this new switch achieves an average leakage of 10aA at room temperature, an 8× reduction over past designs. The cell loses one bit of voltage accuracy, 700µV on a 12-bit scale and 11.3mV on an 8-bit scale, in 3.3 minutes and 54 minutes, respectively. This represents a 15× increase in hold time at these voltage accuracies over the lowest-leakage cell to date, in only 92% of the area. Since the leakage is independent of amplifier bias, the cell can operate on as little as 10nW of power. Initial measurements from a 0.5µm implementation of the switch topology demonstrate sub-attoamp leakage levels in this technology, suggesting the leakage of this switch topology decreases, approximately, with the square of process feature size.

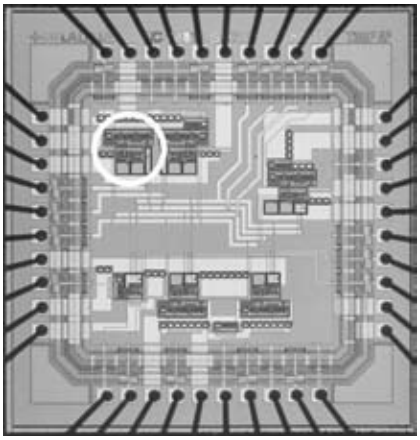

Figure 1: Die photograph (2.2mm × 2.2mm). A differential analog storage cell, which exhibits 10aA net leakage current at room temperature, is circled in white.

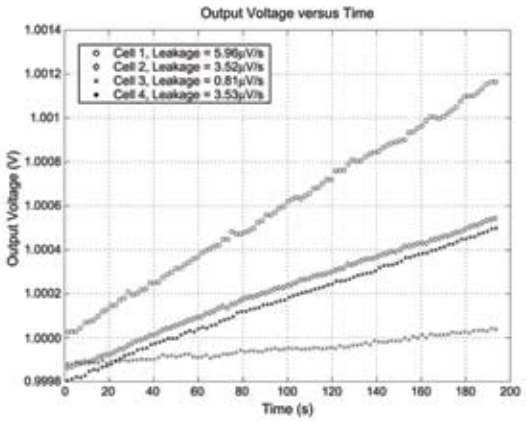

Figure 2: Differential cell leakage with a 2.5pF hold capacitor.

REFERENCES:

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[2] O'Halloran, M., R. Sarpeshkar, "A 10-nW, 12-Bit, Accurate Analog Storage Cell with 10aA Leakage", *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 11, pp. 1985-1996, November 2004.

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Intelligent Human Detection for Night-Vision Systems

Y. Fang, I. Masaki, B.K.P. Horn
Sponsorship: MTL Intelligent Transportation Research Center

Our objective is to apply machine-vision techniques to develop a new generation of night-vision systems with intelligent human detection and identification functions. Currently, more and more infrared-based night-vision systems are mounted on the vehicles to enhance drivers' visual ability, which does allow drivers to see better but also introduces new safety concerns. Drivers need to switch their attention between the windshield and a separate infrared-display screen. Specifically for senior drivers, it is still difficult to identify any abnormal scenario or potential danger in its early stage. For safety purposes, an intelligent human detection and identification system based on infrared-video sequences is expected to automatically track pedestrians' location and to detect any potential dangers based on the targets' action in the monitored environment.

Compared with conventional shape-based pedestrian detection, our new "shape-independent" detection methods include the following two innovations. First, we propose an original "horizontal-first, vertical-second" segmentation scheme that initially, divides infrared images into several vertical image stripes and then, searches for pedestrians, only within these image stripes. Second, we define unique new shape-independent multi-dimensional classification features. We demonstrate the similarities of these features among pedestrian image regions with different poses, as well as, the differences of these features between pedestrian and non-pedestrian regions of interest (ROI). Our preliminary test results, based on limited sample images, are very encouraging in terms of reliability and accuracy for detecting pedestrians with arbitrary poses. Our overall goal is to design systems for future transportation systems to make driving safer and less stressful for all travelers, regardless of age and ability.

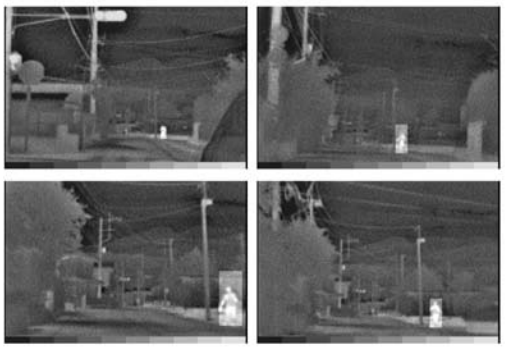

Figure 1: Four pedestrian-detection results in a sequence.

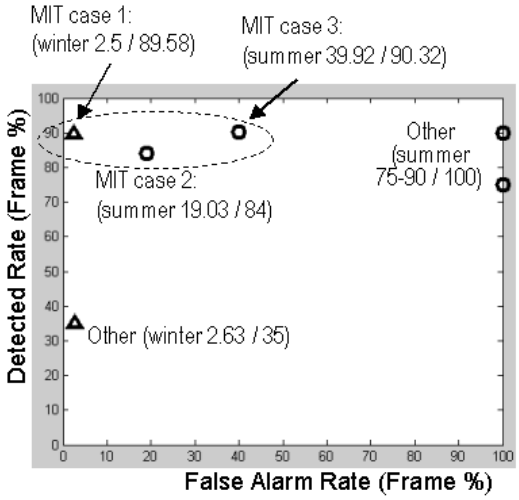

Figure 2: Preliminary results with limited samples.

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Image Fusion for Night-Driving Display

W.F. Herrington, B.K.P. Horn, I. Masaki
Sponsorship: MTL Intelligent Transportation Research Center

Visibility is reduced in a night-driving situation. Potential obstacles which would be visible during the day may not be visible at night due to the limited light provided by vehicular headlights. However, many potential obstacles are visible in an infrared image of the road in front of the vehicle, so providing the driver an infrared view of the road could be helpful. Unfortunately, an infrared image lacks key features such as stoplight color and may lack features such as lane markings, depending on the wavelength band used. The lack of key features means that the infrared image could not be used on its own to operate the vehicle. A fused image combining features from the visible image and one or more infrared images could provide the driver with the key features of the visible image and the additional information present in the infrared image(s). Our research has been directed at fusing visible, near infrared, and far infrared images for a night-driving display system.

Figure 1: Visible image of an intersection at night. The vehicle from which the image was taken was using its low-beam headlight setting.

Figure 2: Fused image of a night driving scene combining the visible image (Figure 1) with a near infrared image and far infrared image (not shown). The fused image contains more information than any individual image.

Minimum Energy Sub-Threshold Digital Circuits

Y.K. Ramadass, J. Kwong, A.P. Chandrakasan
Sponsorship: Texas Instruments, DARPA

Sub-threshold operation allows drastic energy reduction in digital circuits when energy rather than performance is the primary constraint. Substantial savings in the energy consumed by a digital circuit can be obtained by operating the circuit at the optimal supply voltage. The variation of the energy consumed per operation with the operating voltage for a FFT circuit is shown in Figure 1 [1]. This curve is dynamic in nature and changes with temperature, workload of the circuit, nature of operations performed by the circuit, and data handled. The optimum energy point shifts widely as the curve changes, which necessitates a circuit to track the optimum energy point with changing conditions. The optimal supply voltage for minimum energy operation usually falls into the sub-threshold region of operation of digital circuits. In this work, we are developing a feedback circuit to track the minimum energy point of a given system.

We are also developing a sub-threshold library that addresses the unique challenges and trade-offs in ultra-low voltage operation. Drive currents become comparable in magnitude to idle leakage currents, causing reduced output swings and possible functional errors. Due to the exponential dependence of sub-threshold currents on threshold voltage, sub-threshold circuits are particularly sensitive to environmental and process variations. As Figure 2 illustrates, this sensitivity results in a trade-off between energy and variability, which significantly impacts the functional and parametric yield of sub-threshold circuits. The sub-threshold library employs a device-sizing methodology that assures functionality at operating corners while implementing appropriate trade-offs among energy, delay, and variability. Particular attention is given to robustness of memory storage elements, where idle leakage can significantly degrade data retention capabilities. This library will serve as a platform for further exploration of parallel and error-resilient architectures in the sub-threshold regime.

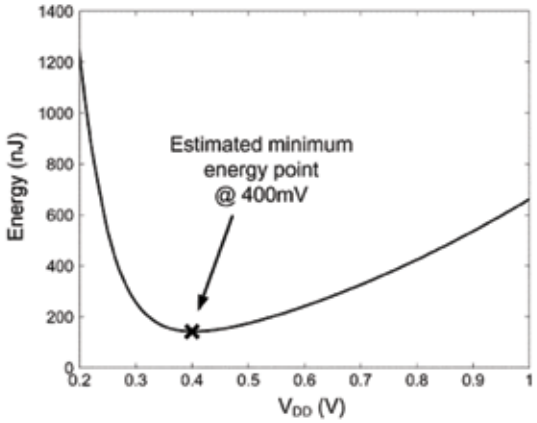

Figure 1: Estimated minimum energy point for an FFT processor. Courtesy: A. Wang and A. Chandrakasan, *IEEE JSSC*, January 2005.

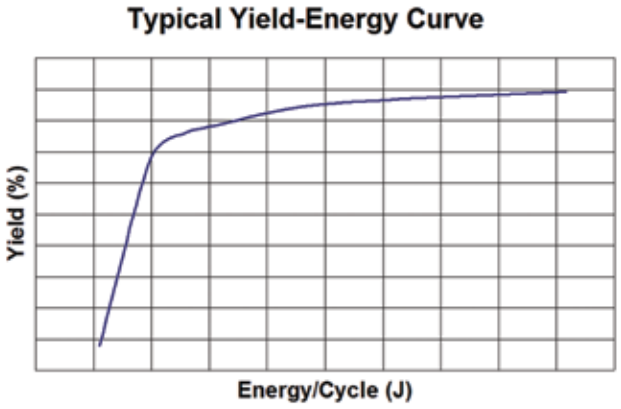

Figure 2: A typical yield-energy curve.

REFERENCES:

[1] Wang, A., A.P. Chandrakasan, "A 180-mV Sub-threshold FFT Processor Using a Minimum Energy Design Methodology," *IEEE Journal of Solid-State Circuits*, pp. 310-319, January 2005.

Low Energy Digital Circuit Design Using Sub-Threshold Operation

B.H. Calhoun, A.P. Chandrakasan
Sponsorship: DARPA, Texas Instruments

Scaling of process technologies to smaller dimensions has become a given in the solid-state circuits industry. Recently, process scaling has produced a number of engineering obstacles. Most notably, both active and leakage power of processors are increasing exponentially with technology scaling. For emerging low power applications such as distributed micro-sensor networks or medical applications, low energy operation is the primary concern instead of performance, with the eventual goal of harvesting energy from the environment. Sub-threshold operation has emerged as a promising approach to these ultra-low-energy applications because it achieves the minimum energy per operation. Lowering V_{DD} decreases active energy by V_{DD}^2. For circuits whose leakage energy becomes comparable to the active energy, an optimum V_{DD} for minimum energy operation exists. This optimum typically occurs in the sub-threshold region [1].

Previous work confirms that sub-threshold operation is functional and that it provides minimum energy operation [1][2]. Several key problems remain that prevent sub-threshold designs from becoming a competitive option. Specifically, it is essential to understand how the minimum energy point depends on different key parameters and to model it for easy application to generic designs. To this end, we have developed a model for determining the optimum point for minimizing energy [3]. We have also analyzed the impact of sizing for minimum energy in sub-threshold circuits [4]. To increase the attractiveness of sub-threshold design, we proposed a method for integrating it with high performance applications to extend DVS across orders of magnitude of frequency variation and verified ultra-DVS with a test chip [5]. Figure 1 shows the measured energy profile of the test chip, and Figure 2 shows the die photograph. We are continuing to examine sub-threshold design, focusing on SRAM design in the presence of process variation.

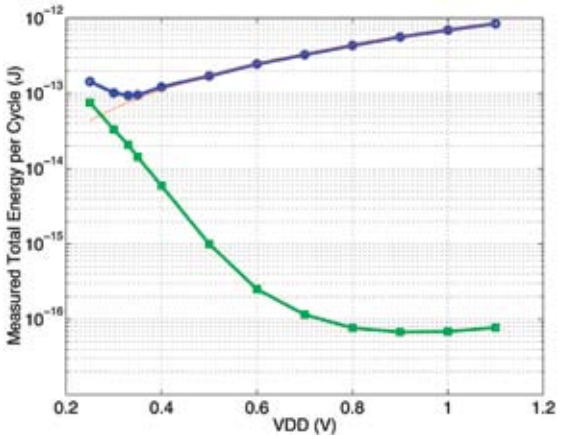

Figure 1: Measured energy characteristics of 90nm test chip.

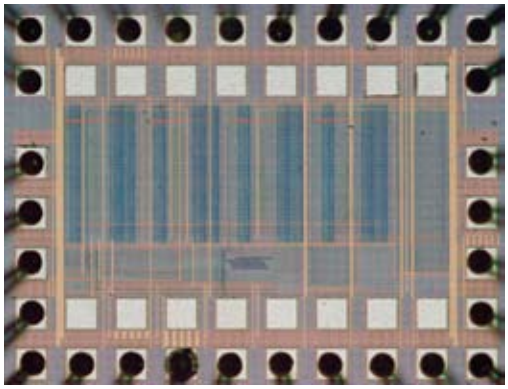

Figure 2: Die photo of 90nm test chip that demonstrates ultra-dynamic voltage scaling.

REFERENCES:

[1] Wang, A., A. Chandrakasan, S. Kosonocky, "Optimal Supply and Threshold Scaling for Sub-threshold CMOS Circuits," *IEEE Symp. on VLSI* , pp. 7-11, 2002.

[2] Wang, A., A. Chandrakasan, "A 180mV FFT Processor Using Sub-threshold Circuit Techniques," *IEEE International Solid-State Circuits Conference*, February 2004.

[3] Calhoun, B.H., A. Chandrakasan, "Characterizing and Modeling Minimum Energy Operation for Sub-threshold Circuits," *International Symposium on Low Power Electronics and Design*, pages 90-95, August 2004.

[4] Calhoun, B.H., A. Wang, A. Chandrakasan, "Device Sizing for Minimum Energy Operation in Subthreshold Circuits," *Custom Integrated Circuits Conference*, pages 95-98, October 2004.

[5] B.H. Calhoun, B.H., A. Chandrakasan, "Ultra-Dynamic Voltage Scaling Using Sub-threshold Operation and Local Voltage Dithering in 90nm CMOS," in *Proceedings of the IEEE International Solid-State Circuits Conference*, pages 300-301, 599, February 2005.

Optical-Feedback OLED Display Using Integrated Organic Technology

K. Lamba, A. Lin, K. Ryu, V. Bulovic, I. Kymissis, C.G. Sodini
Sponsorship: MARCO C2S2, MARCO MSD

Organic LEDs (OLEDs) are a promising new technology in flat panel displays that can be used to build large, thin, flexible displays. With OLEDs, the pixels are emissive instead of light-filtering, which increases contrast, decreases response time, and removes the need for a backlight, thus, decreasing the overall display thickness. However, OLEDs exhibit non-linear light output characteristics, and their power efficiency drifts over time due to operational degradation. This degradation reduces display uniformity and decreases the effective display lifetime. We propose to drive OLEDs to the desired brightness using optical feedback on the pixel level. Preliminary research [1] has shown that using feedback will increase the effective lifetime by six- to tenfold. This project aims to build a complete system that encompasses the design and fabrication of an integrated silicon control chip and an organic pixel/imaging array, which together will form a stable, usable display.

The integrated silicon control chip is composed of multiple compensation blocks, which perform feedback in parallel (Figure 1). Each compensation block is composed of two functional circuit blocks — the current sensing block and the feedback compensation block. The current sensing block is a transimpedance amplifier that converts the photo-detector output current to a voltage level. The feedback compensation block stabilizes the loop, ensuring a desirable response time and phase margin, and is implemented using a fully differential switch-capacitor filter. This control circuit is designed and fabricated using a National Semiconductor 0.35µm process. The organic pixel/imager array consists of pixels with organic field effect transistors (OFETs) that select and control OLED pixels and photo-detectors (Figure 2). The photo-detector consists of an organic photoconductor and a row-select OFET. A process for integrating the organic components and metal connections is currently being developed.

We acknowledge National Semiconductor for providing the fabrication services.

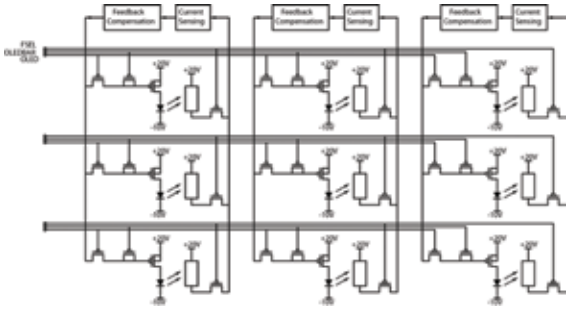

Figure 1: A sample 3x3 portion of the pixel/imager array. The display pixels in a row are driven simultaneously in a column-parallel architecture.

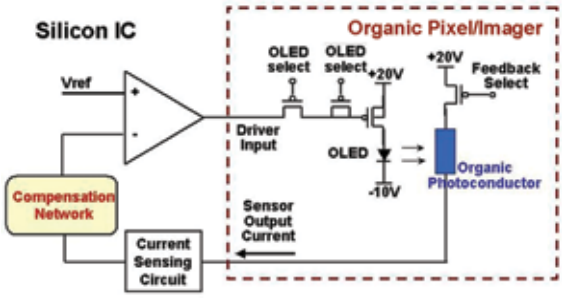

Figure 2: A schematic of an organic pixel/imager. The three pass transistors select a particular row while a fourth drives the OLED to a desired brightness. The photo-detector then converts the light output into current, which is passed to the silicon control circuit.

REFERENCES:

[1] Powell, M.R., "Integrated Feedback Circuit for Organic LED Active-Matrix Display Drivers", Master's Thesis, MIT, 2002

Characterization of Organic Field-Effect Transistors for OLED Displays

K. Ryu, I. Kymissis, V. Bulovic, C.G. Sodini
Sponsorship: MARCO C2S2

The field of organic semiconductor materials and devices is rapidly expanding due to the commercialization of novel organic electronic technologies, such as organic light-emitting diodes (OLEDs), and organic photovoltaic cells. Among the organic devices that have been actively studied are organic field-effect transistors (OFETs) which are compatible with low temperature substrates, such as plastic foils and thus, enable design of large-area circuits. The number of papers published each year pertaining to OFETs is increasing rapidly, and a new conference titled Organic Field-Effect Transistors was organized in 2002 under the Society of Photo-Optical Instrumentation Engineers (SPIE).

We are developing OFET arrays as sensors and switches for OLEDs. Today's displays, using OLEDs, consume less power and have higher contrast and better hue/saturation compared to liquid crystal displays, suggesting OLEDs may be the next generation of flat panel displays. However, OLEDs degrade severely with usage. The quality of OLED display images degrades over time because not all pixels are used equally, leading to undesirable burn-in artifacts. One solution to this problem is to use optical feedback to correct for the change in OLED pixel brightness. Optical sensors are placed behind each pixels, and the signal captured by these sensors are used to control the corresponding OLED pixel. In our implementation, the sensor/switch arrays are fabricated in OFETs because of their compatibility with OLED fabrication.

In this project, we are modeling OFET response by investigating the governing physical processes to aid the design of OFET circuits, such as the ones used in OLED display panels. Parameters such as mobility, threshold voltage, and contact resistance are extracted, and peculiarities like mobility dependency on the gate bias are explored. Mobility and contact resistance has been extracted via various methods, and charge storage in the channel and the effect of charge trapping are being investigated primarily through I-V and C-V measurements (Figure 1) and specialized structures (Figure 2).

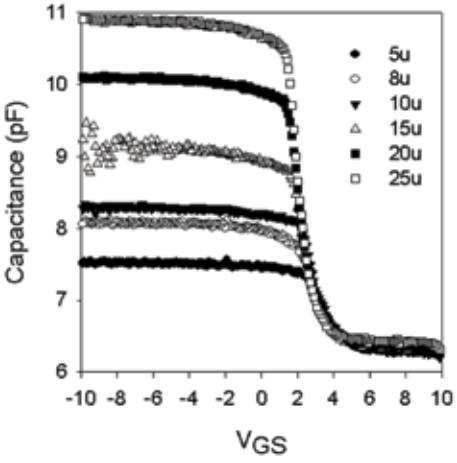

Figure 1: Capacitance vs. channel length measured directly in 1000μm-wide OFETs.

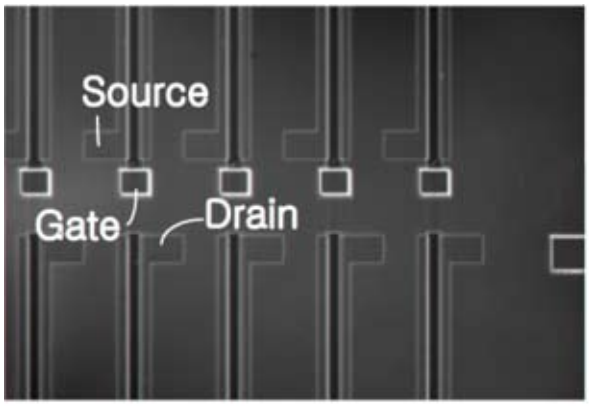

Figure 2: Array of lithographically patterned OFETs fabricated at MTL.

CMOS-Compatible Compact Display

A.R. Chen, A.I. Akinwande, H.-S. Lee
Sponsorship: MARCO C2S2

Portable information devices demand displays with high resolution and high image quality that are increasingly compact and energy-efficient. Microdisplays, consisting of a silicon CMOS backplane integrated with light- generating or -modifying devices, are being developed for direct-view and projection applications.

Toward the goal of a micro-projector suitable for portable applications, a microdisplay architecture, using silicon light emitters and image intensification, is developed. A standard low-voltage CMOS IC incorporating display drivers and an array of avalanche diodes produces a faint optical image, and an image intensifier efficiently amplifies the image to useful brightness. This architecture has high efficiency and the potential to achieve adequate luminance for projection applications. A proof-of-concept system with 16x32 arrays is implemented and evaluated.

A high-performance silicon backplane for the above system has been designed and evaluated. The backplane is a standard CMOS die including a 360x200-pixel array with silicon light emitters, and 10b precision current mode driver circuits. The driver circuits can support a number of emissive display technologies including silicon light emitters and organic LED (OLED). They employ a self-calibration technique based on the current copier circuit [1] to minimize variation and fixed-pattern noise, while reducing circuit area by half compared to a conventional solution. Two levels of calibration are used, as shown in Figure 1. A circuit technique to improve the retention time of dynamic analog memories is also developed. This technique allows a dynamic analog memory to retain 10b precision for 500ms at room temperature. A die micrograph is shown in Figure 2.

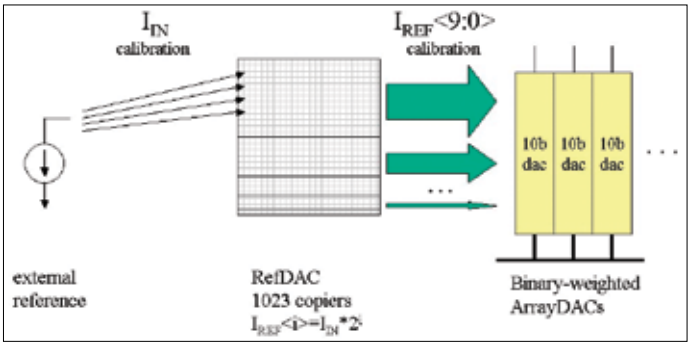

Figure 1: Two-stage calibration technique based on current-copier circuit. A reference current is replicated to make ten highly precise binary weighted-currents. These are used to calibrate the 360-array driver DACs.

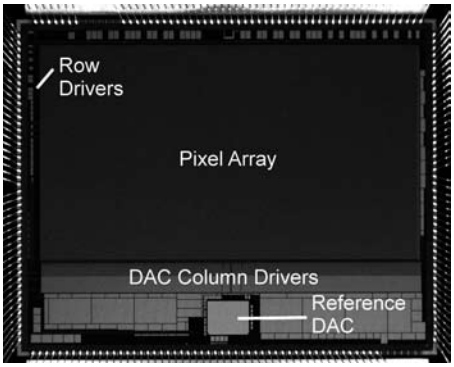

Figure 2: Die micrograph of the integrated silicon backplane.

REFERENCES:

[1] Wouter, D., J. Groeneveld, H. Schouwenaars, *et al.*, "A Self-Calibration Technique For Monolithic High-Resolution D/A Converters," I*EEE J. Solid-State Circuits* 24(6) pp. 1517-1522, December 1989.

A Low-Power Display Driver with Simultaneous Image Transformation

J. Walker, A.P. Chandrakhasan, A.I. Akinwande
Sponsorship: DARPA, Army Natick Soldier System Center

While multimedia-enabled mobile devices have recently exploded into mainstream commercial use, two major, and often conflicting, demands exist in displays for mobile devices: low power and high quality. High-quality multimedia applications demand high-resolution screens capable for displaying fast-moving images. Unfortunately, the higher the resolution and the rate of change of the images, the more energy is required to process and display them. Not only is more energy required, but higher bandwidth is also necessary since more data must be processed in a fixed amount of time.

While displays for mobile devices are the first to deal with energy and bandwidth requirements, it is easy to see that as displays move to higher resolution, these concerns begin to affect all displays. For example, a standard VGA screen has 640x480 pixels (307,200). A refresh rate of 100 Hz and 8-bits per pixel requires a data rate of 250 Mb/s. A higher definition screen of 6400x4800 pixels at a refresh rate of 100 Hz and 8-bits per pixel would require a data rate of 25 Gb/s . This bandwidth requirement increases as N^2 where N is the number of pixels required along either horizontal or vertical dimensions. Techniques that can reduce energy/bandwidth as well as scale with the resolution of the display will be extremely useful.

In this work, we designed, implemented, and evaluated the energy consumption of a system that uses a liquid crystal display to perform a one-dimensional transform. The RMS-response of the liquid crystal elements was exploited to perform a matrix multiplication (image transformation) over a single frame period. This image transformation was the last step of decompression in an image-processing system. The system was first implemented in Matlab, then as a printed circuit board, and finally as an integrated circuit. While the initial Matlab and printed circuit board implementations looked more promising, a number of practical considerations arose during the integrated circuit design that ultimately resulted in moderate performance: 14.3% energy savings.

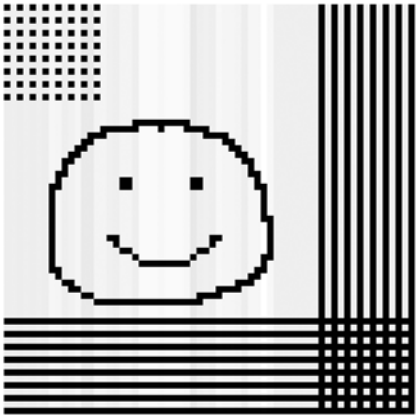

Figure 1: Matlab Implementation using DB1 Wavelet with three scales of decomposition.

Figure 2: PCB Implementation using DB1 Wavelet with three scales of decomposition.

REFERENCES:

[1] Lawrence, N.A. *et al.*, "Experimental Verification of a Novel Multiple Line Addressing (MLA) Scheme for Passive Matrix LCDs'," *EuroDisplay*, pp. 955-958, 2002.

Circuit and System Techniques for On-Chip Interconnects

B. Kim, V. Stojanovic

Signaling over global on-chip wires has been an increasingly difficult problem for the last several generations of VLSI technologies. As the technology scales, global wires scale poorly, causing a large increase in latency, and forcing the system architects to focus on small, modular designs in which they can keep the cost of inter-module communication to scale approximately the same as the gate delay. Long interconnects are used only when necessary since, in addition to the latency, they require a significant amount of power due to repeater insertion needed to regenerate the signal along the interconnect. The goal of our project is to take a look at these interconnects as micro-communication systems. We are developing signal conditioning and coding techniques that will take advantage of the interconnect channel properties and improve the data rate, latency, and power, while using very simple circuits. Our approach builds on the previous work on interconnects [1]-[3] by adding some of the techniques used in off-chip high-speed links [4].

From the perspective of communication channels, long interconnects exhibit different frequency- selective behavior depending on the geometry and density of the wires, as Figure 1 shows. Depending on the geometry of the wires and the location of the current return paths, channels can exhibit dominantly dispersive (RC) behavior, or have slightly resonant behavior (RLC). Our initial results show that even in the lossy RC regime, we can obtain about a 2x improvement in the data rate over the current state-of-the art interconnect equalization technique [1], as Figure 2 shows, with comparable if not potentially simpler circuits. We believe that the data rate and latency improvements are even higher in the RLC regime and plan to explore this next.

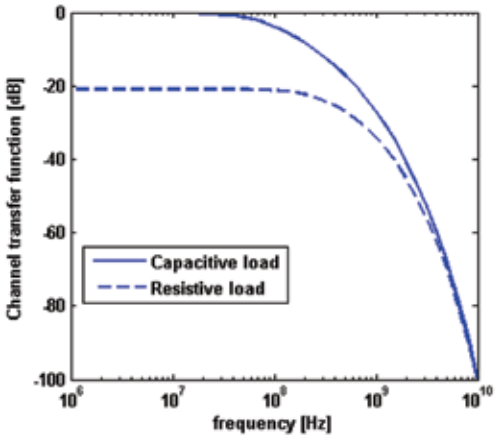

Figure 1: On-chip interconnect frequency response (10mm wire), RC regime, R_L=150Ω used in [1], and C_L=30fF used in this work.

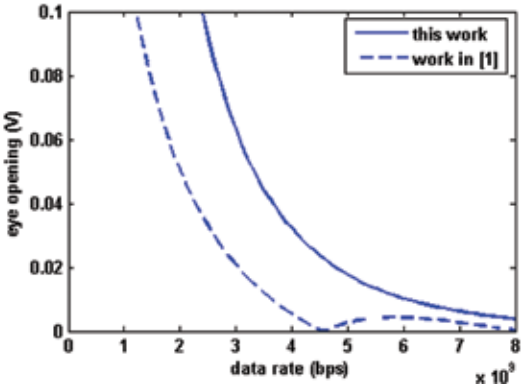

Figure 2: Eye-opening vs. data rate – comparison with [1].

REFERENCES:

[1] Schinkel, D., E. Mensink, E. Klumpernik, E. van Tuijl, B. Nauta, "A 3Gb/s Transceiver for RC-limited On-Chip Interconnects," in *Proceedings of IEEE International Solid State Circuits Conference*, February 2005.

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Evolvable Hardware

D. Sanchez, K.K. Berggren
Sponsorship: MIT Lincoln Laboratory

Harnessing all of the intrinsic data-processing power of electronic devices is impossible through traditional circuit design. While complex physical processes involving electronic, thermal, and quantum phenomena underlie the operation of the devices, standard circuit design methodology appropriately mandates a level of abstraction in which most of these phenomena are safely ignored. In this work, we investigate the possibility that enhanced data processing capabilities exist in previously neglected classical degrees of freedom of a circuit [1].

Design that explicitly incorporates the full phase space of electronic devices into the standard design methodology is fraught with problems: noise, fabrication margins, and poorly understood interactions between the various physical degrees of freedom of the system, which conspire to make a conventional approach difficult. Our approach, instead, uses reconfigurable hardware in conjunction with a genetic algorithm (GA) to search for an optimal circuit configuration based on performance evaluated in hardware. In this approach, many of the limitations of traditional design are removed because the algorithm search is based on the input-output performance and can use all degrees of freedom in the system. Our specific goal is to test these ideas by generating an analog-to-digital converter, using hardware evolution of a reconfigurable circuit controlled by a GA.

The reconfigurable circuit consists of "Totally-Reconfigurable Analog Circuit" chips from Zetex, interfaced with passive circuit elements and each other through switch arrays. Our use of switch arrays in this way departs from past work [2] and provides a way to scale the device to much larger levels of complexity. We have demonstrated the operation of our system by realizing an evolved frequency doubler on a stand-alone TRAC. We are currently working on incorporating switch arrays and digitally programmable passive elements into the system to exploit the larger phase space of the complete reconfigurable circuit.

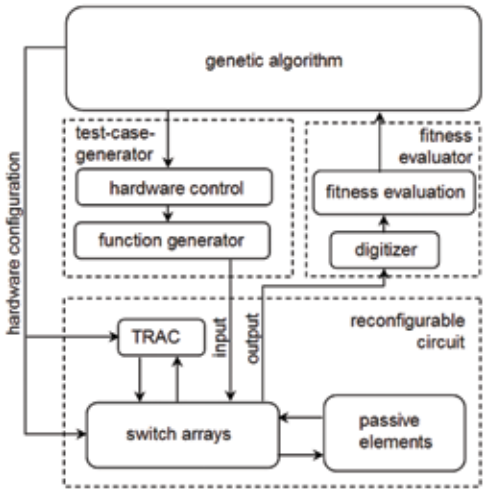

Figure 1: System representation for automated circuit design using an evolvable hardware approach. TRAC and switch configurations are generated by the genetic algorithm. These configurations are then tested using a sequence of test cases, and a fitness is assigned to each particular configuration. The fitness is used to select appropriate configurations for ensuing generations of the algorithm.

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3-D FPGA Design and CAD Flow

Y.-S. Kwon, P. Lajevardi, F. Honoré, A.P. Chandrakasan, D.E. Troxel
Sponsorship: DARPA

Performance of FPGAs is limited by the delay and energy consumption of long wires and programmable interconnects. The 3-D FPGA is a next-generation FPGA with smaller wire-length, higher speed, and lower power consumption. We have fully developed a 3-D FPGA architecture (Figure 1), and it is being fabricated with a 0.18μm Lincoln Labs SOI three-layer 3-D integration technology. The basic tile of the 3-D FPGA consists of 8 LUTs and 8 Flip-flops. The 3-D placement and routing considers speed, energy, and thermal characteristics for placing slices and routing nets in 3-D space. 3-D placement and routing is developed in this research. Experimental results show 45.4% improvement in wire length, 45.9% improvement in delay of critical paths, and 47%~90% energy reduction (Figure 2) in 3-D FPGA compared to that of 2-D FPGA. A 3-D FPGA visualization tool for the placed and routed result has been developed.

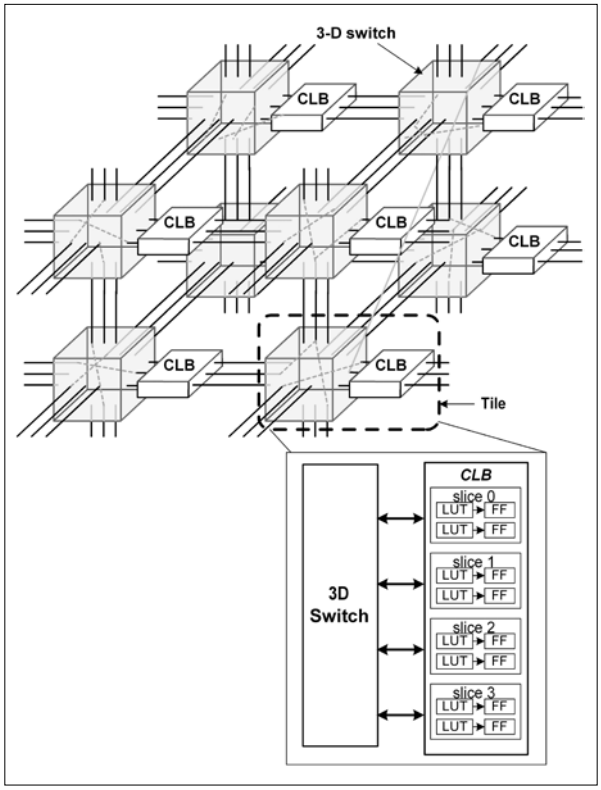

Figure 1: Block diagram of 3-D FPGA, a tile, and a 3-D switch component. The 3-D FPGA is composed of tiles where each tile is composed of 8 LUTs and 8 flip-flops.

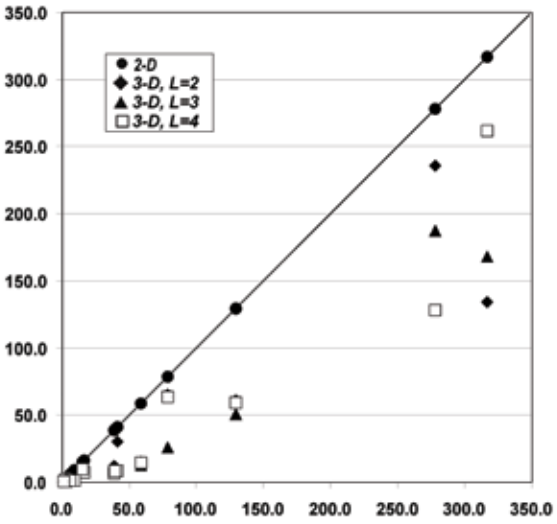

Figure 2: Comparison of power consumption for 3-D FPGA with that of 2-D FPGA.

REFERENCES:

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Low-Power FPGA Circuits and CAD

F. Honoré, A.P. Chandrakasan
Sponsorship: MARCO IFC

Reconfigurability is becoming an important factor in the design of systems. FPGAs are extending their application area from system prototyping to custom application implementation but they are much slower and less power-efficient than ASIC systems. We have developed a power- and performance-scalable multi-VDD FPGA. The interconnect overhead for FPGA's is a large fraction of the power and delay, due to the use of programmable switch elements. Fine-grain voltage domains allow low-energy operation in non-critical areas of logic and routing segments. A modified, programmable switch architecture allows long paths to be pipelined to meet critical path timing or, alternatively, allow reduced voltage operation with minimal performance impact.

A better partitioning of non-critical configuration elements to reduce wire lengths produces further reduction in interconnect capacitance. Approximately 70% reduction in the array area is achieved by relocating the switch block and CLB configuration memory to the periphery of the array, resulting in reduced parasitic capacitance on the critical routing wires.

A power-aware place-and-route tool determines which non-critical paths can run at reduced voltage and configures the various domains of the array accordingly. Thus, selecting the appropriate choice of supply voltage for each domain achieves an average 52% improvement in power for the same performance (Figure 1). Low-overhead level converters provide voltage conversion between domains. With these fine-grain controls, the software can make tradeoffs between power and performance and deliver maximum power savings with minimum performance impact. Sub-threshold leakage reduction is also achieved with fine-grain sleep regions that shut down the power supply to inactive circuits. We have designed a 3x3mm chip (Figure 2) using a customized ASIC flow to validate the approach and have developed custom CAD tools to automate the implementation of some of these techniques.

The chip was fabricated in 0.18µm CMOS technology. We acknowledge National Semiconductor for providing the fabrication services.

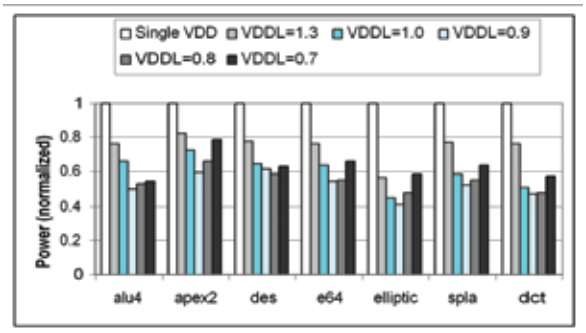

Figure 1: Benchmark results showing an average improvement of 52% at a VDDH of 1.8V and VDDL of 0.9V.

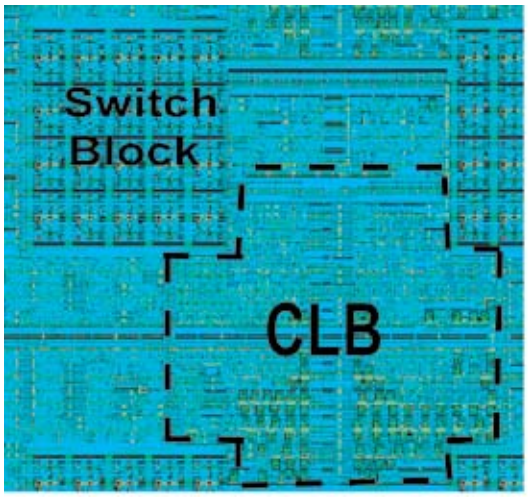

Figure 2: Layout of one logic and switch block tile.

Substrate Noise Analysis Tool for Mixed-Signal Verification

N. Checka, A.P. Chandrakasan, R. Reif
Sponsorship: Texas Instruments Fellowship, MARCO IFC

Mixed-signal circuit design has historically been a challenge for several reasons. Parasitic interactions between analog and digital systems on a single die are one such challenge. Switching transients induced by digital circuits inject noise into the common substrate. Analog circuits lack the large noise margins of digital circuits, thus making them susceptible to substrate voltage variations. This problem is exacerbated at higher frequencies as the effectiveness of standard isolation technique diminishes considerably [1]. The effect of substrate noise on the circuits within an IC is typically observed during the testing phase only after the chip has been fabricated. Determination of the substrate noise coupling during the design phase would be extremely beneficial to circuit designers, who can see the effect of the coupling and re-design accordingly before fabrication. This would reduce the turn-around time for circuits and increase the yield of working chips.

We are currently developing a Substrate Noise Analysis Tool (SNAT) that can be used at any point in the design flow. SNAT requires information on the circuit as well as the technology. The circuit information can be as descriptive as the circuit netlist complete with extracted parasitics or as coarse as a verilog netlist. Similarly, the technology information can be as descriptive as a full substrate doping profile with layout or as coarse as knowing only the substrate resistivity and die size.

The tool generates equivalent noise macromodels to describe the digital system. These macromodels are then coupled with a model for the substrate to yield noise information, such as the time domain profile or spectrum at different points on the substrate. The noise that results from shaping by different isolation techniques can also be determined. The resulting substrate noise data can then be used to simulate its effect on various analog circuits. Figure 1 shows the flow of SNAT.

We have verified the results of SNAT with measurements on a digital PLL designed in TI's 90 nm technology. SNAT yields 12% error in the RMS voltage of the substrate noise when compared to measurements. Figure 2 shows the time domain output of the substrate noise voltage.

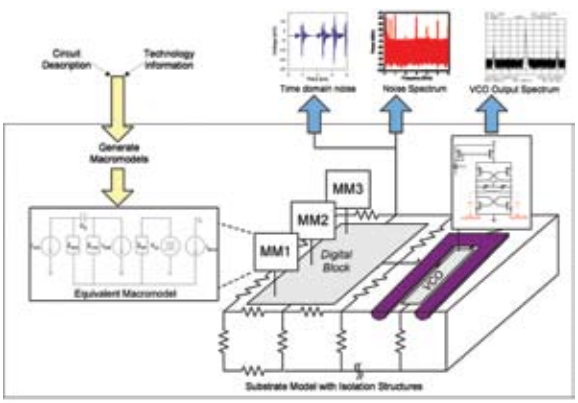

Figure 1: Diagram of Substrate Noise Analysis Tool (SNAT).

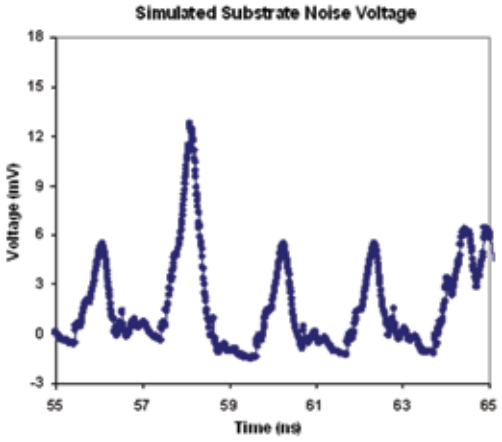

Figure 2: SNAT-generated substrate noise profile of the digital PLL.

REFERENCE:

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Convex Optimization-Aided Design of Analog and Mixed-Signal Communication Systems

R. Sredojevic, V. Stojanovic, J.L. Dawson

Many integrated communication systems today are constrained by either throughput or power dissipation. Cases from high-speed I/O interfaces in processors and routers to low-power radios in cell phones and sensors force designers to tackle one of the two dual problems – optimizing the overall data rate with given power constraints or minimizing the power for given throughput. While much work has gone into both the circuit and communications sides of the problem, the hardest part seems to be communicating the requirements/costs and characteristics of circuits and components to the algorithm level and vice versa, so that the overall optimum can occur. Many design hours and iterations on the system architectures are needed before a system is designed, and even then, very little data exists on the scope of design space or the cost/performance space of the implemented components. What is the new optimal system if the specifications change slightly? To solve these problems, we intend to use the convex optimization as a framework to connect the circuit and system design abstractions.

We are developing a design-optimization framework in which an integrated communication system is constructed out of pre-characterized macros of analog, digital, and mixed-signal circuits. Through the use of convex optimization, tradeoff functions and defined regions of operation are found for each macro. This information is then used at a higher–system design level to determine the right blend of algorithms and system architecture that implement a globally efficient communication system. Convex optimization is critical to this effort, since it also provides the sensitivities of each objective function of the underlying circuit/block parameters, which builds intuition about the design and guides the designer in making intelligent topology changes. This challenging work is currently considered akin to black magic, since the problem, in general, is combinatorial and NP-hard.

We intend to follow the Barcelona Design work [1]-[3] by putting their effort into a more general framework. We will use the Muse™ optimization language developed by Barcelona Design (made available to universities) to integrate the convex optimization framework in the IC design flow. Doing so will allow us not only to optimize a given circuit architecture, but also to explore different architectures, finding the ones that lend themselves nicely to convex optimization. We are currently working on a library of these *adjustable* or *optimizable* macros, such as mixers, VCOs, amplifiers, ADCs, DACs, and even their building elements. With this base and initial optimization results for each of the macros, we intend to engage in a system-level optimization on two example systems: a narrowband communication system (for example, a cell phone radio or a sensor) and a wideband communication system (an ultra-wideband radio or a multi-Gb/s high-speed chip-to-chip link [4],[5]).

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[4] Stojanovic, V., A. Amirkhany, M. Horowitz, "Optimal Linear Precoding with Theoretical and Practical Data Rates in High-Speed Serial-Link Backplane Communication," *IEEE International Conference on Communications*, June 2004.

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Channel-and-Circuits-Aware, Energy-Efficient Coding for High-Speed Links

N. Blitvic, M. Lee, V. Stojanovic, L. Zheng

With state-of-the-art energy-efficiency of 40mW/Gb/s, links in a chip with 40Tb/s I/O throughput, for example, would dissipate 1.6kW of power, requiring 8000 high-speed I/O pins, and the on-chip area of 4000mm^2 for 4000 10Gb/s transceivers, in 0.13µm CMOS technology. The switch card would need to be at least 8 feet wide and have a 13-feet-wide connector with today's connector density limit of 50 differential pairs per inch. Clearly, we need to improve both the energy-efficiency of the link cells and per/pin data rate by at least an order of magnitude, to avoid excessive power dissipation and maintain a reasonable size of the system. This data rate scaling is theoretically possible, since the information theoretic capacity of link backplane channels is between 80 and 110 Gb/s [1], as shown in Figures 1 and 2.

By using multi-tone modulation in links [2], we not only increase the data rate of a link, but also decrease the energy cost of signaling per bit due to parallelism in frequency domain. Unfortunately, the gap of uncoded multi-tone modulation to capacity is still very big (around 14dB) due to very low BER target of 10^{-15} in these applications and the peak swing constraint of the on-chip driver circuits. The gap is even bigger in today's state-of-the-art baseband links, where residual interference from reflections and cross-talk limits the scaling of link data rates, requiring the use of costly reflection and cross-talk cancellers.

In this project, we aim to extend the link system design to incorporate energy-efficient coding techniques. Using novel energy-efficient coding techniques for non-Gaussian noise and residual interference, we will both increase the achievable data rates and the energy-efficiency of links by drastically off-loading the low-BER target burden and hence, decreasing the complexity of the equalization/modulation level. One theoretic footing of our work is based on our recent results in [1],[3], where a new framework was developed to systematically study energy efficient transmissions in a non-ideal environment, with time-varying link quality, peak-power constraint, processing energy overhead, and even, modeling errors.

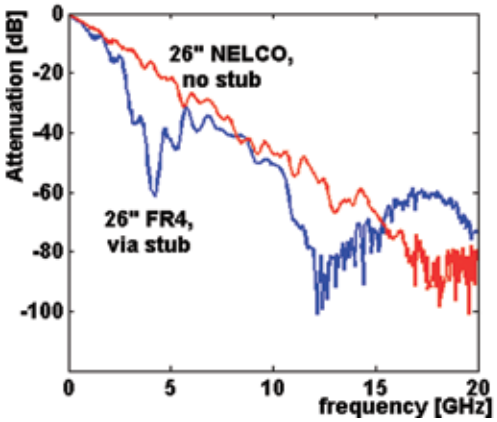

Figure 1: Legacy (FR4) and new, microwave-engineered (NELCO) backplane channels.

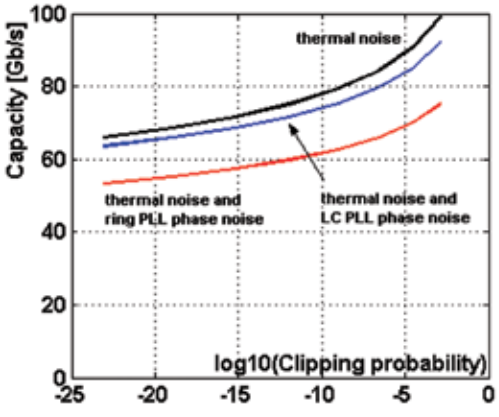

Figure 2: Legacy channel capacity with 50Ω termination thermal noise and phase noise from LC and ring VCO-based PLL.

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A Massively Parallel High-Speed, Low-Power ADC for WiGLAN

M. Spaeth, H.-S. Lee

Sponsorship: SRC, MIT Center for Integrated Circuits and Systems

The specifications for the Wireless Gigabit LAN (WiGLAN) project require the analog-to-digital converter (ADC) in the receiver to quantize a wideband 150-MHz signal at 600 MSPS with SNR and linearity in excess of 75dB (12 bits). Using a massively parallel architecture (128 active ADC channels), the requisite speed for each channel is reduced, enabling the use of sub-threshold circuits in an extremely low power (<100mW, core) solution. In a parallel time-interleaved system, any mismatches between channels result in undesired,spurious tones. While most existing time-interleaved ADCs either employ a low degree of parallelism, such that the tones appear outside the signal band, or are low enough in resolution that the tones are below the quantization noise floor, all gain, offset, and timing skew mismatches must be calibrated away to achieve the stated high-performance specifications.

The top-level block diagram shown in Figure 1 describes the general organization of the chip. The 128 14-bit pipeline ADCs are arranged into 16 blocks of 8 channels each. The hierarchal organization of the design allows individual blocks to be pulled out for background calibration, while the remaining blocks continue to quantize the input signal. Standard techniques are used to measure and remove gain and offset mismatches between channels, but several novel techniques are being explored in this design to calculate and remove systematic timing skew between channels. An additional channel is added to the design to act as a timing reference for some of the timing skew measurement algorithms. A novel token-passing control scheme is used to generate local clock phases for the individual blocks and channels, minimizing the number of clock lines that must be routed across the chip.

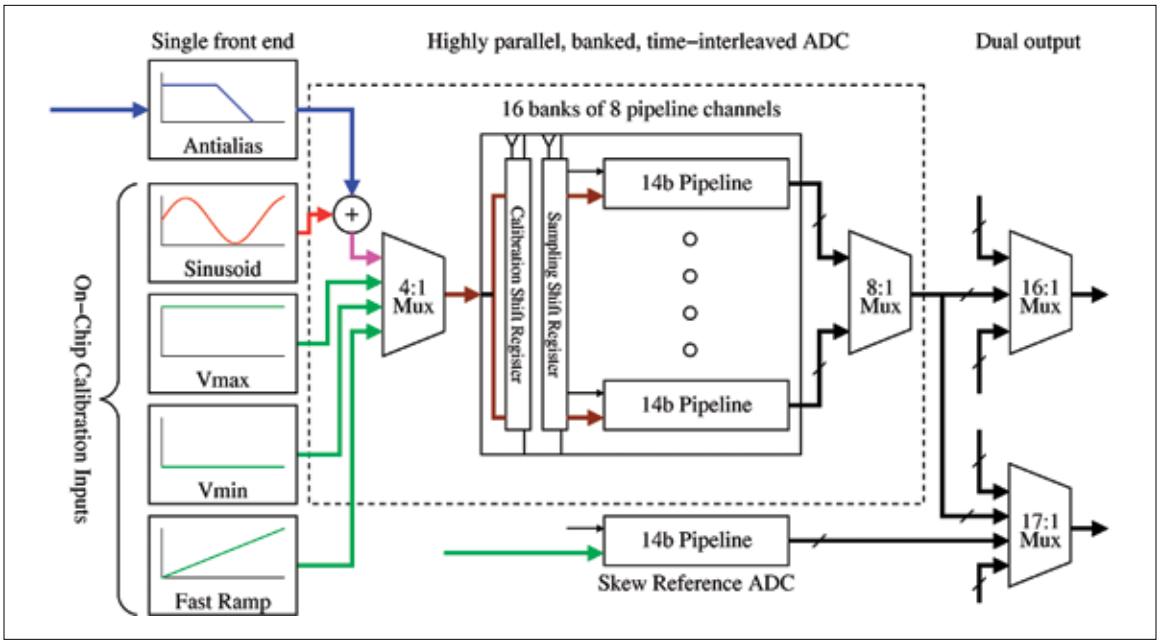

Figure 1: Top-level block diagram of the massively parallel ADC.

Background Self-Calibration of A/D Converters by Direct Transition Point Alignment

L. Brooks, H.-S. Lee, G. Wornell
Sponsorship: MIT Center for Integrated Circuits and Systems

Traditional calibration methods for A/D converters employ either foreground or background calibration. The foreground calibration requires a separate calibration phase during which regular conversion must be halted. Often, the converter must be recalibrated due to the drift of the converter characteristic. Each recalibration requires discontinuing the regular conversion until the calibration is complete. The background calibration circumvents these issues by continuously calibrating the converter in the background while the converter is working normally. However, in order to accommodate background calibration, typically redundant channels or stages of converters are required so that the extra channel/stage can be replaced for those that are being calibrated. A slow, but accurate, "reference" ADC is often employed to calibrate the fast converter against. Some techniques employ special input signals, such as the reference voltage and/or ground for the calibration. Alternately, some background calibration methods use a "skip-and-fill" technique, in which normal conversion samples are skipped and filled by digital interpolation. During the skipped samples, calibration is performed. Such calibration requires a complicated interpolation algorithm to fill the missing data as well as to reduce the input signal bandwidth.

In this research, we are developing a novel background digital self-calibration method applicable to any A/D converter topology. The only requirement is that the raw A/D converter must be free of "wide" codes that cannot be removed by digital calibration alone. This condition is necessary for any fully digital calibration. The absence of wide codes can be easily guaranteed, either by introducing over-range capability or intentionally reducing the inter-stage gain. The background calibration in this research requires neither redundant channels for calibrating off-line nor special input signal, such as the reference voltage or ground. Instead, the errors are calibrated directly from the digital output statistics from regular input signals.

The advantages of the new direct calibration method are numerous. There is no need for either additional analog hardware, such as a redundant channels or stages of the converter, or a "reference" converter to calibrate against. The calibration is highly accurate because the transition points are directly aligned. Also, since the calibration is performed from regular input signals, no special signals are necessary for calibration.

The behavioral simulation indicates calibration to a very high accuracy is feasible. Presently, we are working on a detailed system design using the new comparator-based switched capacitor (CBSC) concept.

Cartesian Feedback for High-Bandwidth Power Amplifier Linearization

J.W. Holloway, J.L. Dawson

Current RF power amplifier (PA) linearization techniques are presently being investigated to improve PA linearity and power efficiency. One such linearization technique, Cartesian feedback (CFB), makes use of analog feedback to linearize a nonlinear plant (Figure 1). The commanded baseband symbol, I and Q, are compared to the symbol being transmitted by the PA, the baseband symbol is predistorted to correct for PA nonlinearities. Due to significant delay through the PA and parasitic loop poles, the loop must be compensated (H(s) in Figure 1) to ensure an adequate phase margin. The loop dynamics inherently restrict the baseband symbol bandwidth. This limitation is juxtaposed with CFB's insensitivity to changes in PA characteristics over time, temperature, and load impedance. Given the difficulty in modeling these PA characteristics, CFB is attractive compared to other linearization methods requiring detailed PA models [1].

Much work has been done with Digital Predistortion (DPD) linearization techniques. These techniques rely on a mapping of baseband symbols to predistorted symbols. This mapping makes use of a predetermined inversion of the PA model. Transmitters using DPD are open-loop systems, supporting very large symbol bandwidths. However, these techniques make use of cumbersome PA models and cannot compensate for changes in PA dynamics. To deal with this limitation, adaptive DPD schemes, in which the predistortion mapping is periodically updated or refined, are employed. This solution still requires a significant amount of PA modeling and the addition of power-hungry DSP hardware [2].

We consider a linearization system in which a CFB loop is used as an analog computer, providing a DPD system with a symbol mapping (Figure 2). The CFB loop is closed periodically on a low-bandwidth set of symbols, training the DPD system. When the CFB system has finished training the digital predistorter, the feedback loops are broken, leaving an open-loop system. So equipped, the DPD system can be used to linearize the PA with high-bandwidth symbol streams [3].

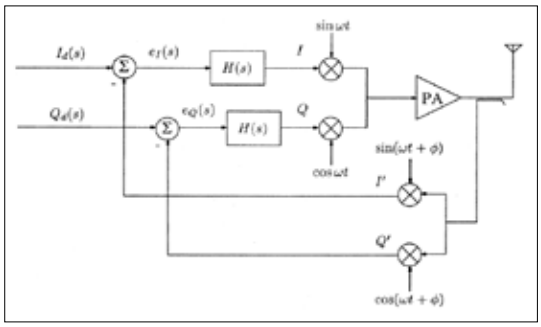

Figure 1: Conceptual Cartesian feedback linearization for a quadrature modulation transmitter [1].

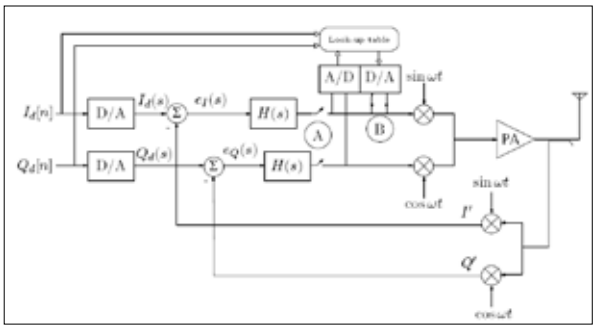

Figure 2: Cartesian feedback-trained digital predistortion technique [3].

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Chopper Stabilization in Analog Multipliers

A. Hadiashar, J.L. Dawson
Sponsorship: National Semiconductor

Analog multiplication is widely used in systems today ranging from analog building blocks to phase-alignment systems. As with any system, analog multipliers are plagued by DC offset. The Gilbert multiplier cell in Figure1 shows common mismatches in resistor sizes, transistor W/L's, and threshold variations that contribute to the offset. We can model this offset by three quantities-- δ_x, δ_y, and δ_z--as shown in the block diagram in Figure 2. These offsets can lead to inaccurate results in critical calculations. For example, in a phase-alignment system integrated with Cartesian Feedback, any significant errors in the sum of products IQ'-QI', which is critical to the phase alignment, can lead to instability in the loop [1].

Chopper stabilization is a well known technique for removing DC offset from amplifiers. We propose a new application of chopper stabilization to analog multipliers for improved DC performance. In order to apply this method, two necessary modifications must be made, as Figure 2 shows: the first is to chop the two inputs in quadrature, and the second is to perform the down chopping operation at twice the input-chopping frequency. The result is, effectively, to separate the offset terms from the desired output. Our goal is to produce an in-depth analysis of the performance and to examine the limitations of this new technique when applied to analog multiplication.

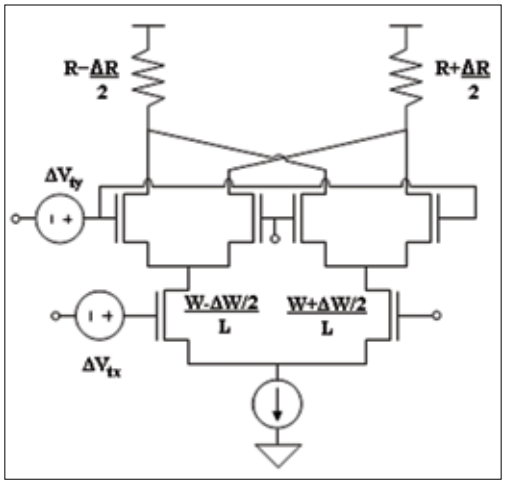

Figure 1: Standard Gilbert multiplier cell with offsets.

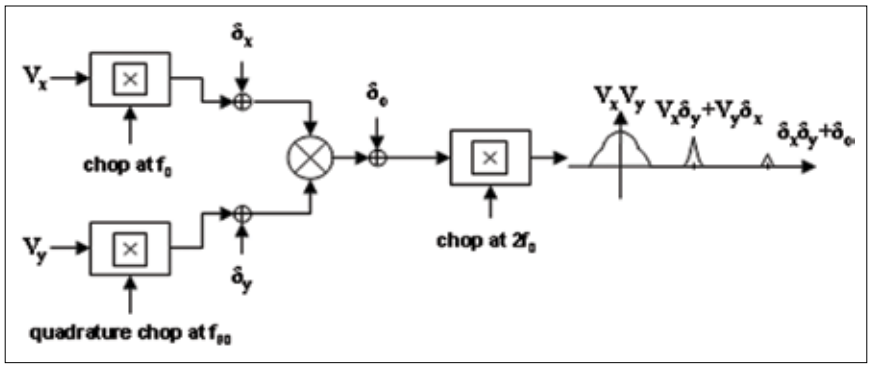

Figure 2: Block diagram for chopper stabilization system applied to analog multiplication.

REFERENCES:

[1] Dawson, J.L., T.H. Lee, "Automatic Phase Alignment for a Fully Integrated Cartesian Feedback Power Amplifier System," *IEEE Journal of Solid-State Circuits*, pp. 2269-2279, December 2003.

Comparator-Based Switched Capacitor Circuits (CBSC)

J. Fiorenza, T. Sepke, P. Holloway, H-S. Lee, C.G. Sodini
Sponsorship: MARCO C2S2, MIT Center for Integrated Circuits and Systems

Traditional analog designs are based on feedback circuits using operational amplifiers (op-amps). In scaled technologies, the design of op-amps becomes extremely challenging. The high gain required for analog feedback systems has traditionally been achieved using cascoded amplifiers. The cascode becomes less attractive at low power supply voltages due to the limits it places on signal swing. In order to achieve the required gain, cascading several stages is required. However, placing a cascade of several amplifiers in feedback compromises the stability and/or frequency response of the system.

A new comparator-based design methodology that eliminates op-amps is proposed. Figure 1 shows two versions of a multiply-by-2 amplifier: (a) the traditional op-amp based design, and (b) the proposed comparator based design. In both circuits, the capacitances C_{1a} and C_{1b} are equal. During phase ϕ_1 the input voltage is sampled onto capacitors in both circuits. During phase ϕ_2 of the op-amp based circuit, the op-amp forces node V_X to the common mode voltage (V_{CM}). All the charge from C_{1b} is transferred to C_{1a}, causing the output to settle to $2*V_{IN}$. During phase ϕ_2 of the comparator-based circuit, the current source charges the output node until the comparator detects that node V_X has reached the common mode voltage (V_{CM}). At this moment, the current source is disabled and the charging stops. All charge from C_{1b} has been transferred to C_{1a} and the output is at $2*V_{IN}$. In the comparator-based circuit, an additional short phase is required between ϕ_1 and ϕ_2 to preset V_X below V_{CM}. This phase is omitted from Figure 1.

The comparator that replaces the op-amp determines the accuracy of the proposed method. The required comparator is a continuous-time comparator. The comparator detects the threshold crossing that determines completion of the charge transfer. This event is not synchronized to any system clock. Three factors affect the accuracy of the comparator decision: the offset voltage (V_{OS}), delay (t_d), and jitter (σ_{td}). These effects are illustrated in Figure 2. Offset voltage, due to device mismatch and finite comparator delay, result in signal independent errors that can be corrected. The comparator jitter is a statistical uncertainty in the detection of the threshold crossing due to transistor noise sources. This timing uncertainty can be translated into an equivalent input-referred noise voltage that is superimposed on the comparator threshold voltage. Because of its random nature, noise is a fundamental limitation of accuracy.

Currently, a proof of concept 10-bit, 10-MHz Analog-to-Digital Converter (ADC) is being designed for fabrication in National Semiconductor's 0.18-μm process. The goal of the design is to demonstrate the methodology of the comparator-based switched capacitor circuit and investigate the accuracy of the comparator.

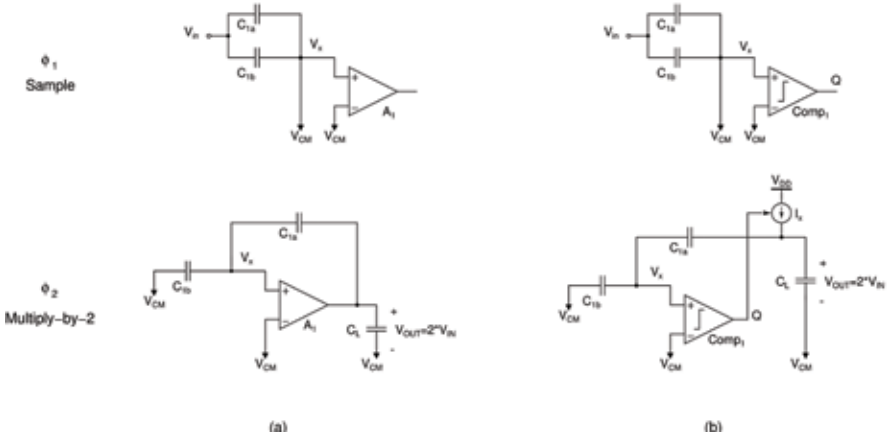

Figure 1: (a) Traditional op-amp based multiply-by-2 amplifier versus (b) proposed comparator based multiply-by-2 amplifier.

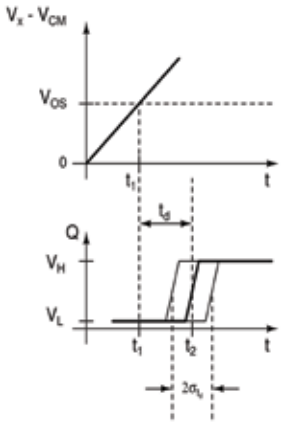

Figure 2: Continuous-time comparator performance metrics.

Analog-Digital Hybrid Signal Processing and Data Conversion

M. Guyton, H-S. Lee
Sponsorship: MIT Center for Integrated Circuits and Systems

This work investigates hybrid signal processing, i.e., signal processing with parallel analog and digital signal paths. Applications of hybrid signal processing will focus on filtering and data conversion. The motivation for hybrid processing is to mitigate the traditional kT/C noise constraint in an analog/digital data-sampling interface. Mitigating this constraint will allow higher signal-to-noise ratios (SNR) to be achieved under the low power-supply voltages of scaled CMOS technologies. To accomplish this goal, hybrid signal processing will be used to reduce linearity requirements in continuous-time circuits.

In a sampling circuit, the sampling function introduces kT/C noise. Because continuous-time (CT) sigma-delta (SD) modulators use CT loop filters, the sampling function takes place after signals pass through the loop filter, allowing sampled noise to be shaped and eventually attenuated. Thus, this project focuses on CT SD modulators.

One difficulty in implementing SD modulators is the implementation of a precise transfer function. Sampled-data circuits such as discrete-time (DT) switched-capacitor filters have precisely controlled transfer functions. In contrast, CT filters require tuning to achieve precise filter characteristics. In general, using tunable components greatly compromises the linearity of the filter.

To alleviate linearity requirements in this tunable filter, hybrid signal processing can be used (Figure 1). In this topology, the anti-aliased input signal is first digitized by a coarse, fast ADC. An analog residue is created using a coarse DAC and a subtractor, analogous to a stage of a pipelined ADC. This small residue passes through the CT filter/SD modulator combination. The output of the coarse ADC passes through a digital filter that matches the SD ADC's STF and gets combined with the digital output of the SD modulator. In this manner, the amplitude of the SD modulator input is much reduced and so its linearity requirement is relaxed.

It is hypothesized that removing the coarse bits from the input will not affect noise-shaping and signal filtering. Assuming that the coarse DAC is accurate, any quantization errors made by the coarse ADC will be cancelled when the coarse bits are added back at the SD ADC output.

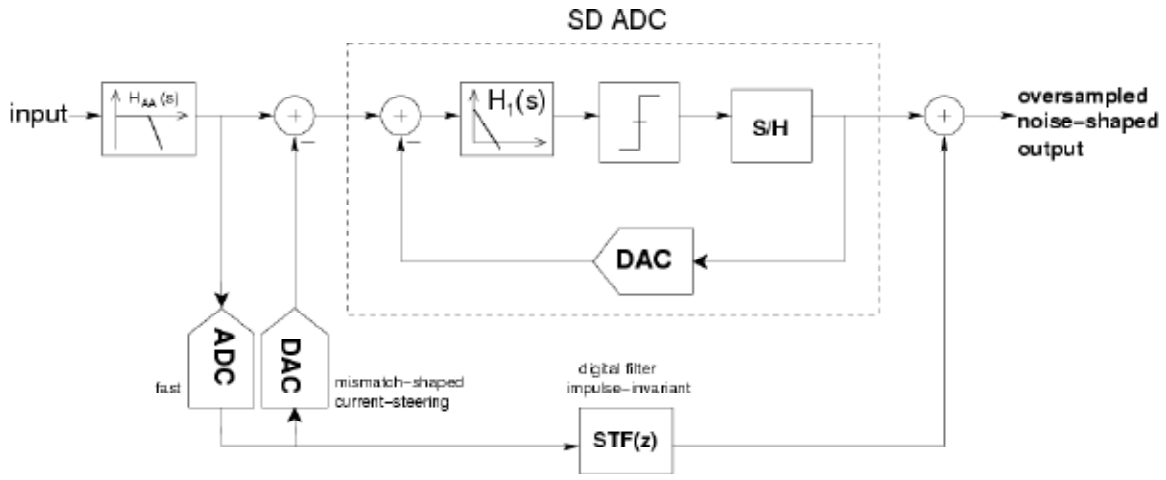

Figure 1: Proposed topology

Digital Implementation and Calibration Technique for High-Speed Continuous-Time Sigma-Delta A/D Converters

M. Park, M.H. Perrott
Sponsorship: NSF

A/D converters are essential building blocks for many applications. In particular, mobile communication devices require low-cost, low-power, and high-performance A/D converters. A sigma-delta A/D converter is often chosen for wireless applications because high resolution and wide bandwidth are achievable by increasing the oversampling ratio and designing the appropriate loop filter. High oversampling ratios are relatively easy to achieve because state-of-the-art CMOS technologies are capable of high frequency operation. However, implementing a low power discrete-time loop filter becomes very challenging as the sampling frequency increases. Therefore, a continuous-time sigma-delta A/D converter is better for a mobile application than its discrete-time counterpart because of its low power consumption.

However, device mismatch is a serious issue for a continuous-time loop filter. Since the mismatch of passive and active elements directly degrades performance, calibration or compensation is necessary to implement a high- resolution and wide-bandwidth A/D converter. In this work, we propose an automatic calibration and compensation technique for a continuous-time loop filter using digital circuits.

The core technique consists of an algorithm that estimates the individual component values of the loop filter. The spectrum of the digital output signal from the sigma-delta converter contains the quantization noise that is shaped by the noise transfer function (NTF). The NTF can be estimated by system identification techniques. A DSP building block is designed to evaluate the parameters of passive and active elements from the estimated NTF. Then, a feedback loop calibrates the passive and active elements. An adaptive digital filter is also used to deal with non-ideality, which cannot be calibrated due to the technology limitations such as finite rising or falling time of signal.

We acknowledge National Semiconductor for providing the fabrication services.

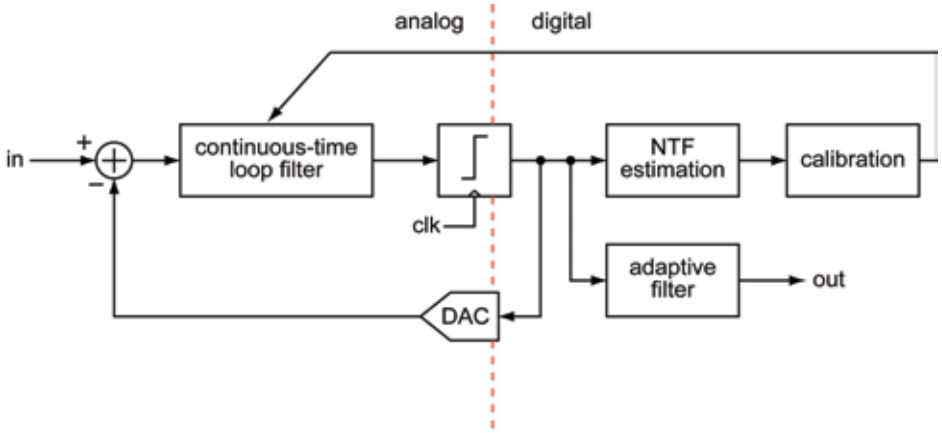

Figure 1: Continuous-time sigma-delta A/D converter using digital calibration and compensation

Advanced Delay-Locked Loop Architectures for Chip-To-Chip Communication

C.-M. Hsu, M.H. Perrott

A challenging component in high-speed data links is the clock and data recovery circuit (CDR). Two primary functions of a CDR are to extract the clock corresponding to the input data and then to resample the input data. The conventional technique uses a phase-locked loop to tune the frequency and phase of a voltage-controlled oscillator (VCO) to match that of the input data. In some applications, such as chip-to-chip communication, a reference clock that is perfectly matched in frequency to the signal sequence is available. However, the clock and data signals are often mismatched in phase due to different propagation delays on the PC board. In such cases, using a delay-locked loop, as shown in Figure 1, instead of phase-locked loop allows for much simpler design, since only a phase adjustment is necessary [1].

The aim of this research is to develop advanced delay-locked loop architectures for chip-to-chip communication. In order to provide a fine-resolution and wide-range delay, a digital adjustable delay element consisting of a sigma-delta fractional-N frequency synthesizer is proposed, as shown in Figure 2. This new architecture also provides low-sensitivity to process, temperature, and voltage variations compared to conventional techniques using analog adjustable delay elements, as shown in Figure 1. In addition, a new sigma-delta modulator architecture is proposed to provide a compact design with reasonable power dissipation.

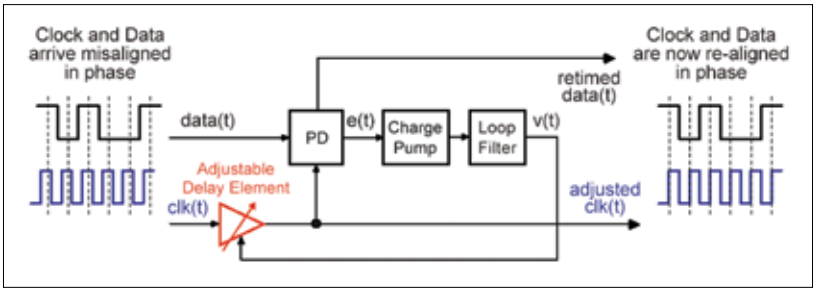

Figure 1: DLL-based data recovery circuit with analog adjustable delay element.

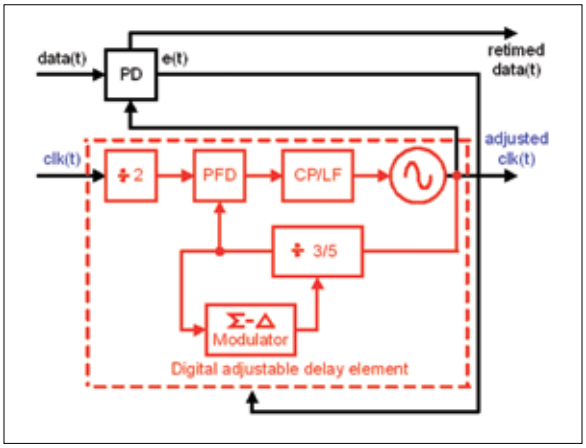

Figure 2: Proposed DLL-based data recovery circuit with digital adjustable element.

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[1] Lee, T.H., J.F. Bulzacchelli, "A 155-MHz Clock Recovery Delay- and Phase-Locked Loop," *IEEE J. Solid-State Circuits,* vol. 27, no. 12, pp. 1736-1746, December 1992.

Optical/Electrical Implementation Techniques for Continuous-Time Sigma-Delta A/D Converters

M. Park, M.H. Perrott
Sponsorship: DARPA

With large-scale monolithic integration of both circuits and optical devices less than a decade away, the field of opto-electrics is poised for a rapid and comprehensive transformation. Indeed, the numerous benefits that accompany full system integration (e.g. lower cost, area, and power consumption; better matching, greater device customization, etc.) will enable designers to create high-performance opto-electrical communication systems that are more affordable and more portable. This reality has the potential to galvanize the telecommunications industry while providing consumers with the next generation of high-speed products. But full-scale monolithic integration also raises many exciting, fundamental questions concerning the boundaries between the optical and electrical worlds. Integrated opto-electronics allows the leveraging of optical devices and their unique properties (e.g. modulators, wave-guides, amplifiers, etc.) in systems that were once exclusively implemented with electronics, resulting in hybrid systems that have superior speed, precision and linearity. Such high performance systems will find innumerable applications in all sectors of industry and may even spur on new technological innovations and inventions. To that end, this project addresses the design of novel circuits and systems with applications in areas that traditionally have not been associated with opto-electronics. Work has begun on an opto-electrical continuous-time sigma-delta analog-to-digital converter. Here, structures employing both optical and electrical signals and devices are utilized to minimize the impact of non-idealities (i.e. input-stage noise/non-linearity, clock jitter, quantizer metastability) that limit the resolution of high-speed converters.

Fast Offset Compensation of High Speed Limit Amplifiers

E.A. Crain, M.H. Perrott
Sponsorship: MIT Center for Integrated Circuits and Systems, National Semiconductor, MARCO C2S2

High gain amplifiers require offset compensation to achieve high input sensitivity. Classic offset compensation in wide bandwidth applications with Non-Return to Zero data streams, as encountered in SONET applications, utilizes a feedback path from the output of the amplifier back to its input through an RC low-pass filter [1][2]. Unfortunately, this approach leads to an undesirable tradeoff between offset compensation time and output jitter – a high offset compensation bandwidth has the benefit of achieving fast settling time at the expense of increased data-dependent jitter. Due to this limitation, current approaches suffer from long compensation times, typically greater than 1 ms for SONET OC-48 applications and often require an off-chip capacitor to achieve an acceptably low compensation bandwidth. Although the long compensation times are acceptable for point-to-point links, they pose a severe obstacle for many-to-one links since the speed of the offset compensation loop may determine how quickly one can switch between input channels.

We propose a compensation scheme that leverages a novel CMOS peak detector structure and a variable tap feedback system that dramatically improves the tradeoff between offset compensation settling time and data-dependent jitter due to the offset correction loop. The proposed system enables a 3 orders-of-magnitude improvement in offset compensation time over the classical approach, while maintaining very low data-dependent jitter levels. To demonstrate the technique, a 7-stage resistor-loaded limit amplifier, which utilized the proposed offset compensation technique, was fabricated in National Semiconductor's 0.18 µm CMOS process. The chip micrograph is shown in Figure 1. Measured results demonstrate offset settling times less than 1 ms while still meeting SONET OC-48 jitter specifications (< 4 ps RMS @ 2.5 Gb/s) (Figure 2).

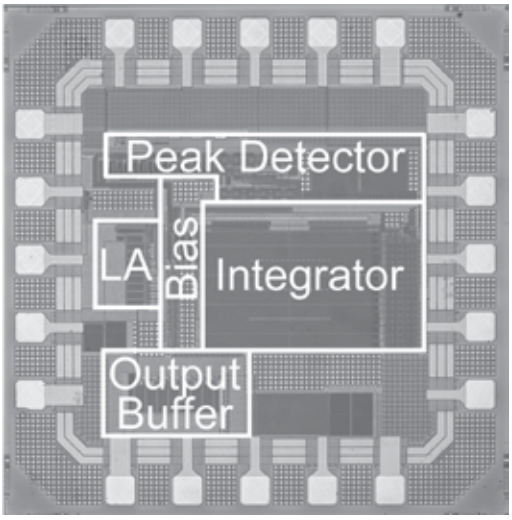

Figure 1: Chip Micrograph highlighting major system blocks.

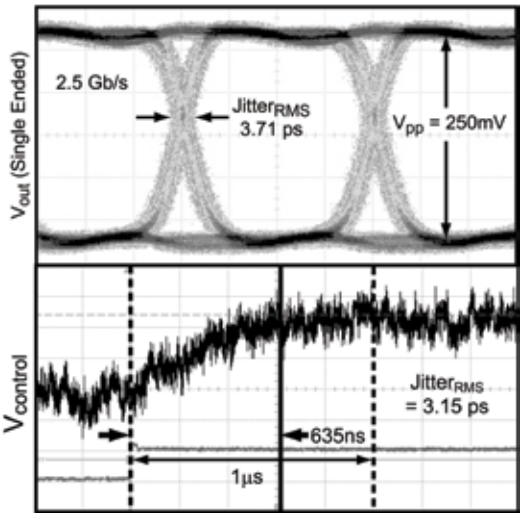

Figure 2: Top - Eye diagram of limit amplifier output with 2.5 mVpp PRBS input; Bottom – Step response of control voltage for closed-loop bandwidth of 1 MHz with 5.0 mV_{pp} PRBS input.

REFERENCES:

[1] Sackinger, E. *et al.*, "A 3-GHz 32-dB CMOS Limiting Amplifier for SONET OC-48 Receivers," *IEEE Journal of Solid State Circuits*, vol. 35, pp. 1884-1888, December 2000.

[2] Galal, S. *et al.*, "10Gb/s Limiting Amplifier and Laser/Modulator Driver in 0.18μm CMOS Technology," *IEEE Journal of Solid State Circuits*, vol. 38, pp. 2138-2146, December 2003.

Techniques for Low-Jitter Clock Multiplication

B. Helal, M.H. Perrott
Partial Sponsorship: MARCO C2S2

High frequency clocks are essential to high-speed digital and wireless applications. The performance of such clocks is measured by the amount of jitter, or phase noise, their outputs exhibit. Phase-Locked Loops (PLLs) are typically used to generate high frequency clocks. However, a major disadvantage of PLLs is the accumulation of jitter within their Voltage Controlled Oscillators (VCOs) [1]. Multiplying Delay-Locked Loops (MDLLs) have been developed in recent years to drastically reduce the problem of jitter accumulation in PLLs [2].

Jitter accumulation is reduced in an MDLL by resetting the circulating edge in its ring oscillator using a clean edge from the reference signal. The Select-logic circuitry commands the multiplexer, using the Edge_select signal, to pass the reference edge instead of the output edge at the proper time, as shown in Figure 1.

The major drawback of a typical MDLL is that it suffers from static delay offset, which causes its output to exhibit deterministic jitter. Static delay offset is caused mostly by phase offset in the phase detector and by various device mismatches. Figure 2 illustrates the problem of static delay offset in a locked MDLL, showing a deterministic jitter of Δ seconds peak-to-peak.

The goal of this research is to develop a technique that detects and cancels static delay offset in MDLLs, thereby, allowing their use in applications that require low-jitter, high-frequency clocks. Behavioral simulations were used to validate the feasibility of the technique and a test chip implementing the proposed approach will be fabricated using National Semiconductors' 0.18μm process.

We acknowledge National Semiconductor for providing the fabrication services.

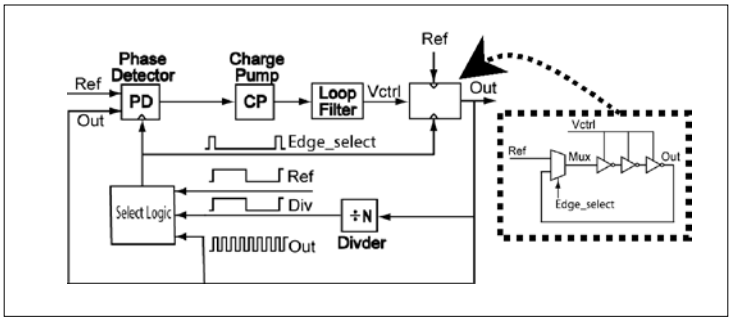

Figure 1: MDLL block diagram.

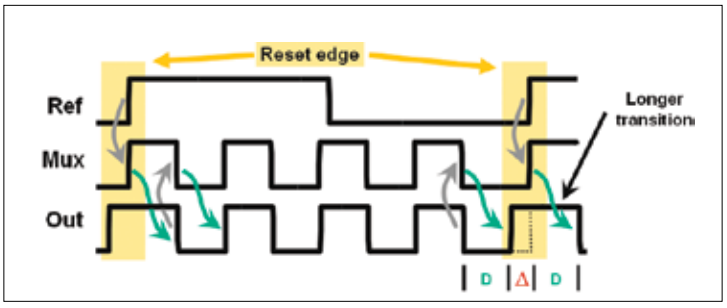

Figure 2: Timing diagram illustrating the problem of static delay offset. Transition time, D seconds, is less than ideal, causing the transition of Out, after the edge reset, to be longer by Δ seconds.

REFERENCES:

[1] Kim, B., T. Weigandt, P. Gray, "PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design," in *Proc. Int. Symp. Circuits and Systems*, vol. 4, pp. 31–38, 1994.

[2] Farjad-Rad, R. *et al.*, "A Low-Power Multiplying DLL for Low-Jitter Multigigahertz Clock Generation in Highly Integrated Digital Chips," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1804–1812, December 2002.

Digital Implementation Techniques for High-Performance Clock and Data Recovery Circuits

C. Lau, M.H. Perrott
Sponsorship: MARCO C2S2

Clock and data recovery (CDR) is a critical function in high-speed digital communication systems. Data received in these systems are asynchronous and noisy, so they must be properly recovered. CDR circuits must also satisfy stringent specifications, defined by communication standards, such as the SONET specification. Other desirable performance metrics, such as fast acquisition time, must also be considered.

A conventional CDR, as shown in Figure 1, employs a phase-locked loop with analog components, including: a phase detector, charge pump, loop filter, and a voltage-controlled oscillator (VCO). Though this analog implementation works well in most current applications, we have already started to see its limitations, as with the scaling of CMOS fabrication technology. For example, this analog system relies on low-leakage capacitors to hold values when the phased-locked loop is locked. The input of the VCO must be held stable in order to minimize frequency drift and jitter in the recovered clock. However, the leakage problem is becoming more dominant as CMOS technology process continues to scale.

In view of the problem described above, our research aims to develop a novel high-speed CDR circuit that leverages digital circuits to achieve high performance, specifically, fast acquisition rate and low-jitter performance. As shown in Figure 2, we have chosen a highly digital structure. While this structure resembles a classical CDR, we have replaced many of the analog building blocks with their digital counterparts. In particular, we use a digitally-controlled VCO to achieve fast acquisition. It also helps to alleviate other problems that are common in the conventional CDR circuits, such as frequency drift due to leakage paths in analog components. Moreover, this architecture also offers high flexibility in integrating other desirable digital functions in the CDR. As a result, our design achieves a compact CDR circuit with fast acquisition and low-jitter performance.

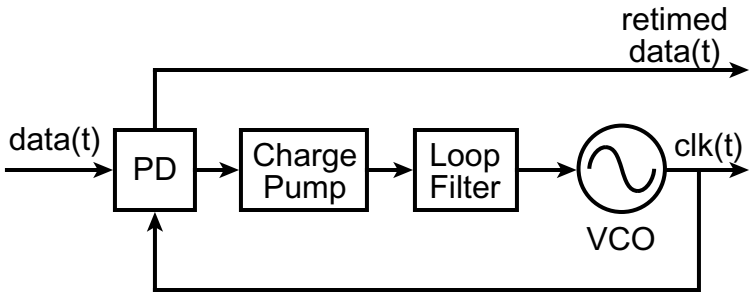

Figure 1: A conventional CDR architecture.

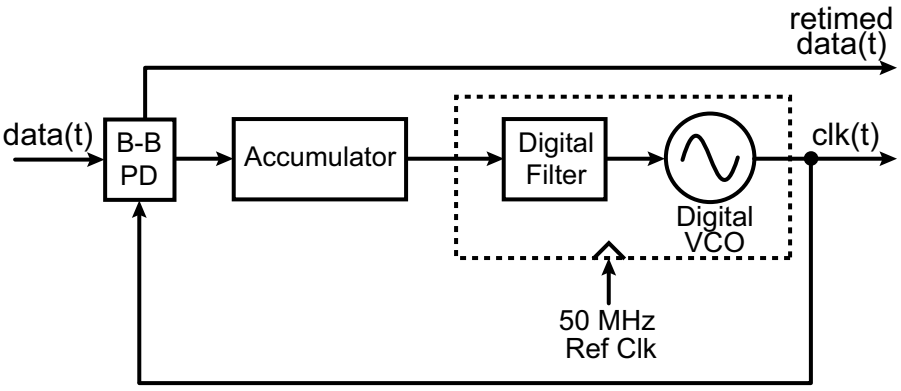

Figure 2: The proposed digital CDR architecture.

Low Phase Noise, High Bandwidth Frequency Synthesizer Techniques

S.E. Meninger, M.H. Perrott
Sponsorship: MARCO C2S2, MIT Center for Integrated Circuits and Systems

Frequency synthesis is an essential technique employed in RF systems. Fractional-N synthesis offers the advantage over integer-N based systems of decoupling the choice of synthesizer resolution from bandwidth. Fast settling, high resolution synthesis becomes possible, giving greater design flexibility at the system level. The central idea behind fractional-N synthesis is dithering of the divide value so that, on average, a fractional divide value is obtained. Dithering the divide value introduces a new noise source to the system. This research focuses on techniques to reduce the impact of the fractional-N dithering noise.

Two approaches have emerged for performing fractional-N frequency synthesis. The first, known as phase interpolation, uses a digital-to-analog converter (DAC) to cancel the dithering noise that appears at the phase/frequency detector (PFD) output. However, mismatch between the DAC output and dithering noise results in poor cancellation. More recently, ΣΔ synthesis, which eliminates the DAC in favor of using a ΣΔ modulator to control the divider, has become popular. The dithering noise is shaped with a high-pass characteristic and must be filtered by the synthesizer dynamics, often resulting in low bandwidths. This work returns to phase interpolation, but imbeds the DAC into the PFD to achieve inherent matching, similar to [1], with the key addition of added circuitry to account for mismatch internal to the PFD/DAC structure. When compared with a 2nd order ΣΔ synthesizer, the proposed architecture results in >31 dB broadband noise reduction with a 7-bit PFD/DAC. The resulting synthesizer exhibits a 1MHz bandwidth yet still achieves -154dBc/Hz phase noise at 20MHz offset from a 3.6GHz carrier. When compared to different phase noise cancellation techniques published in the literature, the PFD/DAC achieves 50% to 200% higher bandwidth and more than 15dB greater noise attenuation.

We acknowledge National Semiconductor for providing the fabrication services.

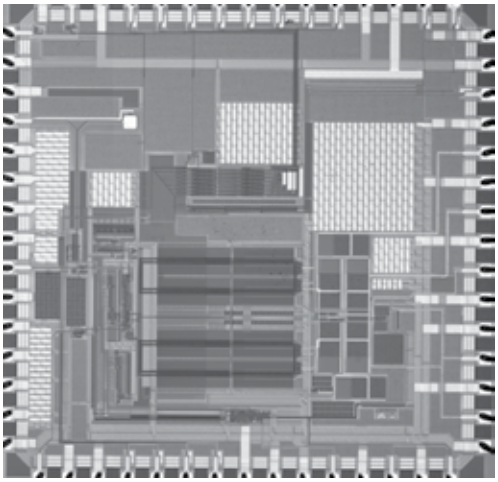

Figure 1: Fabricated 0.18-μm CMOS Synthesizer Chip

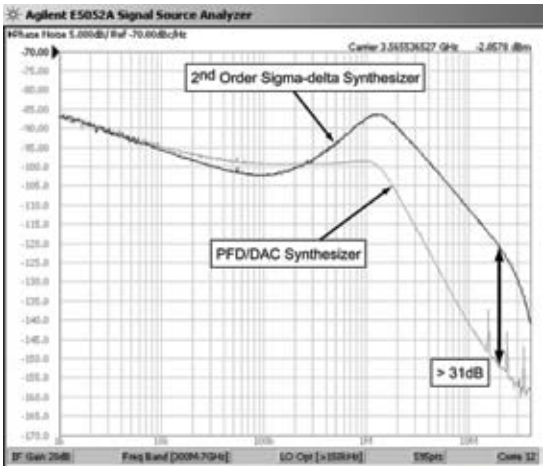

Figure 2: Measured Phase Noise Improvement for Classical 2nd order ΣΔ Synthesizer vs. proposed PFD/DAC Synthesizer.

REFERENCES:

[1] Dufour, Y. "Method and Apparatus for Performing Fractional Division Charge Compensation in a Frequency Synthesizer," US Patent No. 6130561, 2000.

Test Circuits For IC Variation Assessment

K.G.V. Gettings, D. Boning
Sponsorship: Bell Labs CRFP Fellowship, IBM

The study of process variations has greatly increased in importance due to the aggressive scaling of technology. Previous research [1] has shown the substantial impact that process variations in front end of line structures have in reducing yield in integrated circuits. Robust circuit design depends on a more complete characterization of these variations and their impact on circuit-level parameters. This project addresses this issue by developing a methodology capable of testing a large number of front-end-of-line (FEOL) and back-end-of-line (BEOL) structures, and modeling variations in threshold voltage, leakage currents and power dissipation, among others. This is achieved by designing and implementing test circuits that include a large number of high performance devices-under-test (DUTs) controlled by low leakage switches and sensors to ensure a nominal value at the DUT terminals. Accessing analog characteristics of a large number of DUTs will make it possible to gather the statistics necessary to identify and model these variations and to prevent them from contributing to performance failure. This architecture provides a replicable methodology so that the effect of variation sources may be quantified in different technologies. This project studies variations in circuits due to the two fundamental sources of variations in integrated circuits, as noted by Nassif [4]: environmental factors (e.g. power supply variation) and physical factors (e.g. variation in polysilicon dimension). Physical factors can fall into two categories: "die-to-die physical variations" and "within-die physical variations." Analysis includes separation of spatial, layout-dependent, and random variation components, both within die and as a function of wafer location.

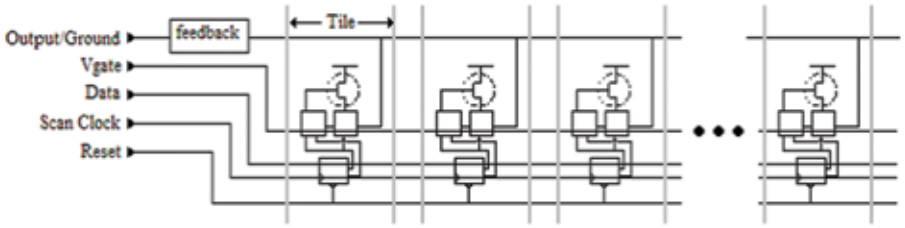

Figure 1: Array of transistors controlled by a limited number of pads

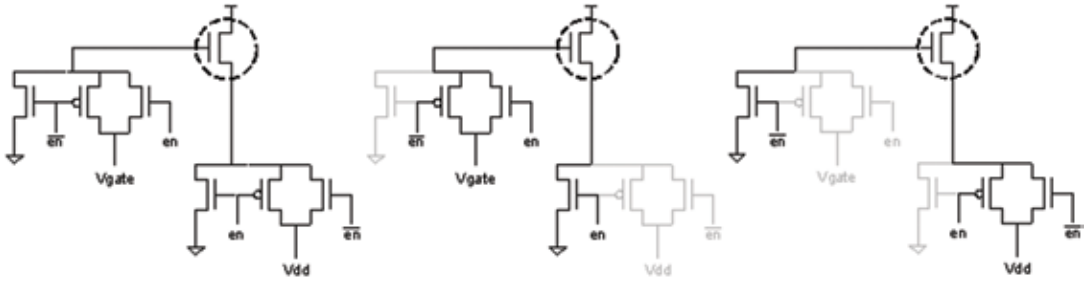

Figure 2: Low leakage switch (left), when enabled (center) and when not enabled (right) and DUT (circled)

REFERENCES:

[1] González-Valentín, K.M., "Extraction of Variation Sources Due to Layout Practices," [*S. M. Thesis*], Cambridge, MA: MIT, 2002. Available through MIT Libraries, Institute Archives Microforms, Noncirculating Collection 3, Cambridge, MA.

[2] Lefferts, R., C. Jakubiec, "An Integrated Test Chip for the Complete Characterization and Monitoring of a 0.25μM CMOS Technology that Fits into Five Scribe Line Structures 150µM by 5,000µm," *International Conference on Microelectronic Test Structures*, pp. 3-63, March 2003.

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[4] Nassif, S., "Modeling and Analysis of Manufacturing Variations," *IEEE Conference on Custom Integrated Circuits*, pp. 223-228, 2001.

Variation Analysis and Reduction Techniques for System- and Circuit-Level Design for Manufacturability (DFM)

M. Gazor, D. Lim, D. Boning
Sponsorship: MARCO C2S2

Modern circuit design needs efficient methods to characterize and model circuit variation in order to obtain high-yielding chips. Circuit and mask designers need accurate guidelines to prevent failures due to layout-induced variations. We address this need by contributing methodologies and new test structures to characterize the variations at the device, interconnect, and system levels. We introduce a methodology to minimize the parameter mismatch in a pair of two large devices, such as transistors and capacitors, using fine-grain parallelism. A large device pair can be divided into a number of small pairs connected in parallel. With a small digital circuitry, we can minimize the total mismatch by adjusting the contribution of the mismatch of each pair. This reconfigurable structure can optimize the mismatch of the whole devices and reduce [or "it reduces"] the non-linearity in circuit behavior. We verify the feasibility of this methodology by probabilistic modeling and Monte Carlo simulation, using estimated variation parameters.

In addition, we study the impact of variation in manufacturing at the system level. Manufacturability at this level is slowly becoming a critical facet of future circuit and system designs. Reduction of geometric primitives, optimal binning, pattern density uniformity, performance robustness, designs for testing, and layout regularity must now be emphasized at even the lowest design levels. We examine this push for more regular circuit and system architectures to reduce the variation component. A design methodology in the form of regular fabrics is introduced and analyzed for its effectiveness in curbing the systematic variation component in digital ICs. Manufacturability of regular, semi-regular, and custom designs are evaluated to understand the impact of regularity on variation, the implications of the various designs on performance, and associated tradeoffs.

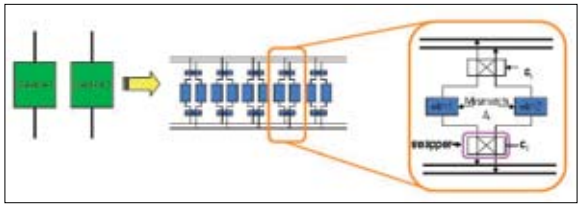

Figure 1: Fine-grain, reconfigurable device-matching structure with swapper cells.

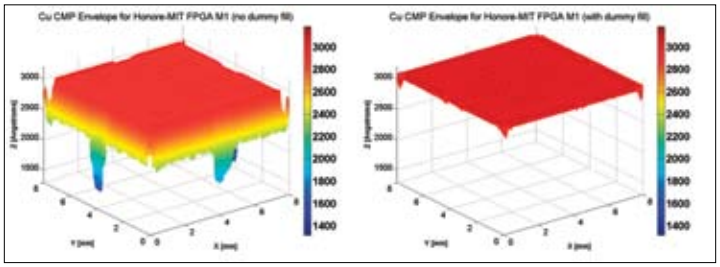

Figure 2: System Level Manufacturability Analysis of Regular Fabric (FPGA) without dummy fill (left) and with (right).

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[1] Strojwas, A., "Design for Manufacturability and Yield," *Proceedings of the 26th ACM/IEEE Conference on Design Automation*, 25-28 , pp. 454-459, June 1989.

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Vibration-to-Electric Energy Harvesting Using a Mechanically-Varied Capacitor

B.C. Yen, J.H. Lang

Sponsorship: Laboratory for Electromagnetic and Electronic Systems

To become a feasible alternative to electrochemical cells, energy harvesting circuits require an energy flyback mechanism that can send harvested energy into a storage node for future use. We present simulated and experimental data for a charge-constrained circuit topology containing an inductive energy flyback that periodically transfers energy harvested from a vibrational source back into a reservoir capacitor. Using a mechanical spring steel variable capacitor with capacitance variation from 415.16 pF to 884.84 pF and an out-of-plane resonant mode of 1560 Hz, the system delivers 1.8 μW at 6 V steady-state voltage to a resistive load. Because the circuit contains only one active device used for controlling the energy flyback rate, timing signal generation is greatly simplified. Unlike previous works, a source-referenced timing scheme was explored in order to prevent unwanted energy injection into the harvesting circuit, which would artificially inflate experimental results. Finally, the system exhibits a startup voltage requirement below 89 mV, indicating that it can potentially be turned on using just a piezoelectric film.

In a typical harvesting cycle, charges are delivered onto a parallel plate capacitor while the capacitance is at its maximum value. As the plates are mechanically pulled apart, vibrational energy performs positive work on the charges, which are momentarily constrained from leaving the plate. When the capacitance reaches its minimum value, the charges are moved off the parallel plate capacitor and harvested through an optimized power electronics network.

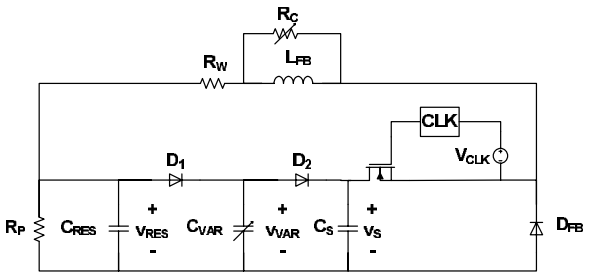

Figure 1: Schematic representation of the electric energy harvesting circuit with inductive flyback. The flyback MOSFET is controlled by a clock referenced to its source to prevent undesired energy injection. Variables R_W and R_C model the wire loss and core loss of the flyback inductor while R_P represents the resistive load being powered by the circuit.

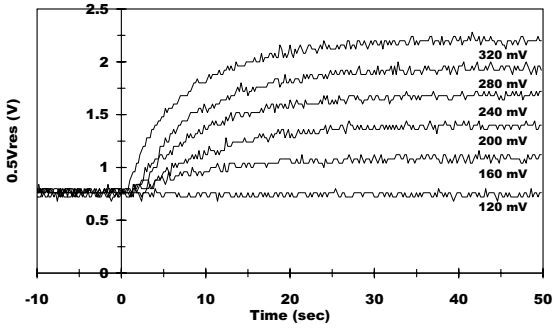

Figure 2: Evolution of v_{RES} for different levels of mechanical shaking. The number immediately below the curves indicates the peak-to-peak shaker amplifier input used to generate that curve. As the vibration level increases, the reservoir capacitor is able to charge up to a higher steady-state voltage, limited by nonlinear inductor core loss.

REFERENCES:

[1] Meninger, S., J.O. Mur-Miranda, R. Amirtharajah, A. Chandrakasan, J. Lang, "Vibration-to-Electric Energy Conversion," in *International Symposium on Low Power Electronics and Design*, pp. 48–53, August 1999.

A research specialist examines his work on a wafer in the Hoyt lab.

EMERGING TECHNOLOGIES

TABLE OF CONTENTS

Microelectronically Fabricated $LiCoO_2/SiO_2$/Polysilicon Power Cells

N. Ariel, G. Ceder, D.R. Sadoway, E.A. Fitzgerald
Sponsorship: CMSE-NSF MRSEC Program, Partial support from ARO

Monolithic on-chip integration was successfully demonstrated in Si CMOS technology. The enhanced development in electronics and optoelectronics technologies has increased the need for an integrative power unit that will also decrease conduction leaks, power losses, and cross talking [1]. We present a rechargeable, all-solid-state thin-film battery compatible with microelectronics technology in its materials, fabrication method, and applications.

Our cells consist of $LiCoO_2$ and polysilicon electrodes and an ultra-thin SiO_2 electrolyte. Solid-state battery electrolytes typically contain lithium and are 1-2-μm-thick. The only lithium-free electrolyte reported was a 0.5-2-μm-thick, porous SiO_2-15 at % P_2O_5 in a Li-battery [2]. Our cells contain an electrolyte of 7-50-nm-thick, silicon technology-compatible SiO_2.

The high-quality, ultra-thin oxide allows fast lithium ion transport and thereby, compensates for the film's higher resistance compared to that of common electrolytes. The cells were fabricated using microelectronics technology as described schematically in Figure 1. Utilizing CMP, we have succeeded in creating highly planar interfaces, enabling the use of an ultra-thin electronically insulating electrolyte. The polysilicon electrode is doped to improve electronic conductivity, and the SiO_2 is thermally grown from a 10-20-nm-thick, undoped polysilicon layer for better oxide quality. Figure 2 is a XTEM image of a cell consisting of 7-nm-thick, lithium-free SiO_2 electrolyte thermally grown from a 20-nm, undoped polysilicon layer. We were able to successfully charge and discharge such cells.

We have demonstrated the utilization of microelectronics processing in fabricating a $LiCoO_2/SiO_2$/poly-Si cell consisting of an ultra-thin SiO_2 layer as a novel lithium-free thin solid electrolyte.

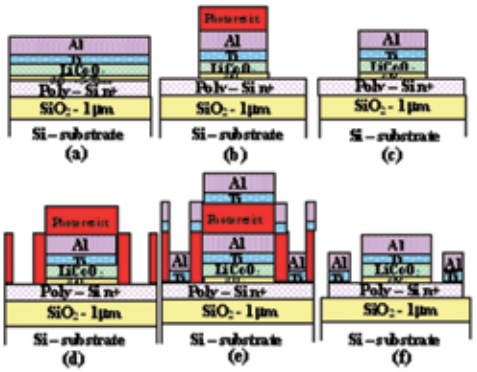

Figure 1: Cell fabrication: (a) poly deposition, CMP and oxidation, $LiCoO_2$ and cathode contact deposition; (b) photolithography and etching to poly level; (c) structure after etching; (d) photolithography to define anode contact; (e) e-beam deposition of anode contact and lift-off; and (f) photolithography and poly etch for isolation of cells.

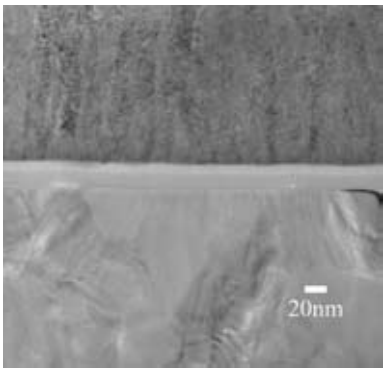

Figure 2: TEM picture showing a $LiCoO_2/SiO_2$/Poly-Si cell, which consists of a 7-nm-thick SiO_2 electrolyte.

REFERENCES:

[1] Balkanski, M., *Solar Energy Materials and Solar Cells*, 62, 21 (2000).
[2] Kushida, K., Kuriyama, K. Nozaki, T., *Applied Physics Letters*, 81, 5066 (2002).

RF Power Potential of 90 nm CMOS

J. Scholvin, J.A. del Alamo, in collaboration with D. Greenberg (IBM)
Sponsorship: IBM Faculty Award, IBM PhD Fellowship

Our research presents the first detailed comparative study of the RF power potential of the various device options offered in a state-of-the-art 90-nm CMOS foundry technology. The roadmap for integration of the RF and digital functions on a chip inevitably goes through the 90-nm node, which offers clear advantages for digital CMOS. However, implementing RF functions, particularly RF power amplification, on deeply scaled CMOS brings unique concerns about performance and reliability. The problem is the low operating voltage that this technology can support. In a modern foundry process, in addition to the nominal digital devices, it is common to offer devices with thicker gate oxides and longer gate lengths for analog and input/output (I/O) functions. This comes at the cost of increased process complexity. When considering the RF power potential of a deeply scaled CMOS technology generation, it is essential to evaluate the suitability of the entire set of devices from a performance as well as a reliability point of view.

Scaling trends of CMOS devices used for power amplifiers have traditionally followed the CMOS roadmap with a delay of 1 or 2 generations (Figure 1). Aggressive technology scaling has recently resulted in power CMOS devices with gate lengths that are shorter than the most advanced III-V RF power FETs. The benefits of scaling for power amplifiers are primarily an increase in gain that can be exploited to increase the power added efficiency (PAE).

We have characterized CMOS devices of different gate lengths and gate oxide thicknesses in a 90nm foundry process, and demonstrated excellent power performance of the nominal (thin gate oxide) 90-nm device [1]. A comparison between the nominal 90-nm device and a thick-oxide 250-nm I/O device integrated on the same wafer is shown in Figure 2. We can see that at a constant voltage of 1 V, the nominal 90-nm thin gate-oxide logic devices offer the best performance, showing a power density of 34 mW/mm and 59% PAE. Operating at 1 V might be required if the system is constrained to have a single voltage supply, which will be determined by the digital portion of the chip. However, if multiple design voltages are available to the designer, and the operating voltage can be selected, the 250-nm long thick gate-oxide I/O devices offer the highest power density and efficiency at 2.5 V.

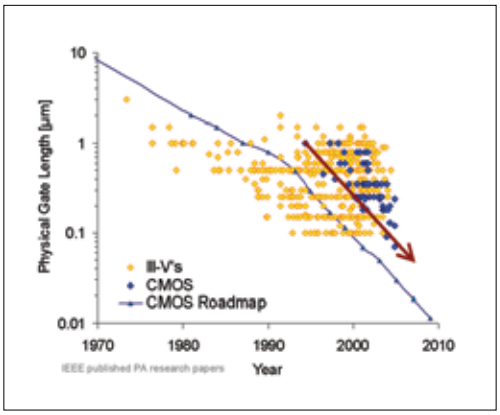

Figure 1: Physical gate length as a function of year showing the scaling trend of CMOS devices and III-V FETs used in RF power amplifiers.

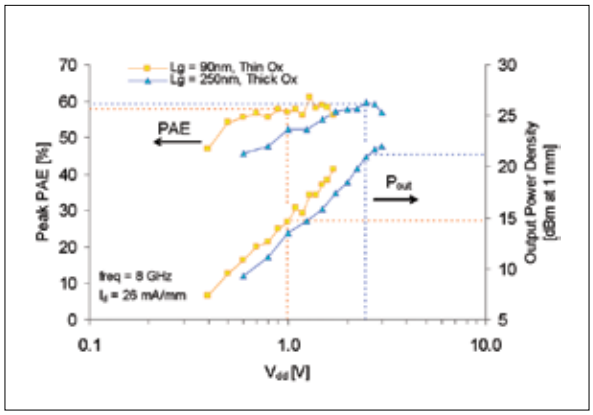

Figure 2: Power performance at 8 GHz for the nominal (thin-oxide) 90-nm device, and the thick-oxide, 250-nm I/O device, as a function of drain bias.

REFERENCES:

[1] Scholvin, J., D.R. Greenberg, and J.A. del Alamo, "RF Power Potential of 90 nm CMOS: Device Options, Performance, and Reliability", *IEEE International Electron Devices Meeting*, 2004, pp. 455-458.

Electron Transport in Ultra-Thin Body SOI MOSFETs

I. Lauer, D.A. Antoniadis
Sponsorship: SRC

Thin-body MOSFET geometries such as double-gate, finFET, and tri-gate devices are attractive because they can offer superior scaling properties compared to bulk and thick-body SOI devices. The electrostatics of a MOSFET limit how short a gate length can be achieved without the gate losing control over the channel. In bulk-like devices, the device designer keeps the gate in control with gate oxide scaling and doping profile design. In thin-body geometries, silicon thickness is a new, powerful scaling parameter. Much like with gate oxide scaling, the electrostatics improve (the gate has more control of the channel) with thinner films. This relationship means that the limits of scaling thin-body devices are closely tied to the limit of scaling silicon film thickness.

The limit of scaling silicon thickness, at least from a theoretical perspective, is determined by the properties of carrier transport. As the silicon film thickness is reduced into the ultra-thin regime, where the film is thinner than the bulk inversion layer thickness, quantum confinement of carriers begins to be observed. For the most part, these effects act to degrade mobility, reducing performance and making further scaling less rewarding.

This project focuses on what can be done to maintain good mobility in ultra-thin silicon films. We are examining uniaxial and biaxial strain in thin and ultra-thin films as a solution to reduced mobility caused by silicon film scaling. By building ultra-thin SOI and SSDOI (Strained Silicon Directly on Insulator) MOSFETs and measuring mobility while applying uniaxial strain, it is possible to examine the transport mechanisms of ultra-thin strained films. We find that strain does enhance mobility in SSDOI and ultra-thin films. Further work is being done to add quantitative physical insight to this observation.

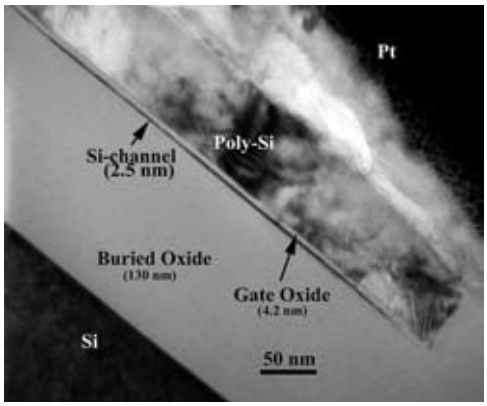

Figure 1: XTEM image of an ultra-thin silicon MOSFET. Uniform single-crystal silicon films of <5 nm can successfully be fabricated.

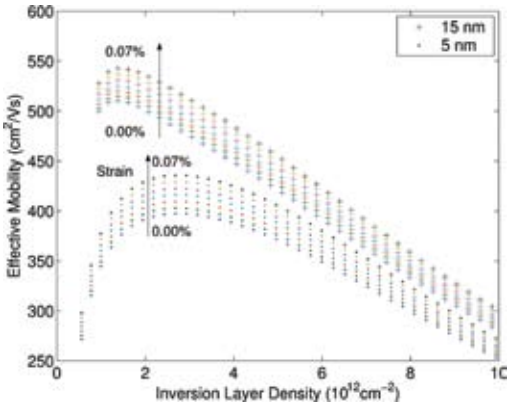

Figure 2: Electron mobility vs. inversion layer density for a thick (15 nm) and ultra-thin (5 nm) SOI film under various levels of strain. More enhancement from strain is observed in the ultra-thin film.

Raised Source/Drain Technology for Ultra-Thin Fully Depleted SOI

L. Gomez, J.L. Hoyt, J.A. Burns, C. Chen
Sponsorship: MIT Lincoln Laboratory

Ultra-thin fully depleted (FD) SOI is an attractive alternative to bulk CMOS because of benefits that include excellent latch-up immunity, higher achievable device density, reduced junction capacitance, and suppressed short channel effects [1]. However, process integration issues (e.g. silicide formation on ultra-thin Si) and high series resistance can hamper this technology. These issues can be addressed by the selective epitaxial growth (SEG) of raised source/drain structures. The focus of the present work is to develop a process to selectively grow raised source/drain structures on FD SOI MOSFETs, and to assess the associated device performance benefits. Future work may include the use of heteroepitaxial SiGe and $Si_{1-y}C_y$ source/drain structures, which can modify channel strain (and thus enhance mobility) and may offer higher dopant solubility and hence lower series resistance.

The incorporation of high quality raised source/drains requires an effective *in-situ* cleaning procedure that rids the active surface of C and O prior to epitaxial growth, while minimizing the thermal budget. In this work, the pre-bake was optimized by varying the process parameters and using Secondary Ion Mass Spectrometry (SIMS) to determine which settings produce minimal amounts of O and C at the epi/substrate interface. An *in-situ* cleaning procedure of 2 minutes at 825ºC in hydrogen ambient was found to be an effective surface preparation prior to selective Si growth (Figure 1). Selective growth is achieved using a dichlorosilane and hydrogen chloride chemistry. Figure 2 shows the successful integration of 30 nm-thick raised source drains on a 0.1um gate-length SOI MOSFET.

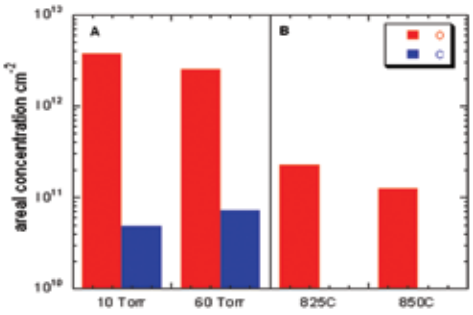

Figure 1: O and C areal density of peaks observed by SIMS at the epi/substrate interface, as a function of (A) bake pressure, and (B) bake temperature. The C content at the interface in part B remained below the SIMS detection limit at both 825ºC and 850ºC.

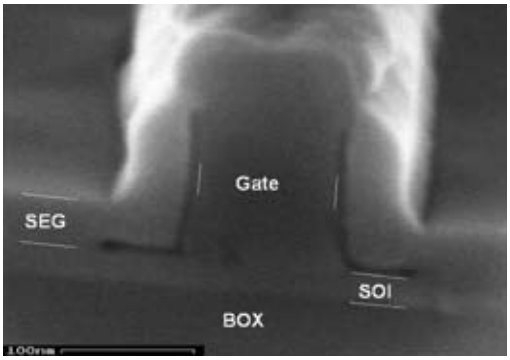

Figure 2: Cross-sectional SEM of 0.1um nFET (25nm SOI) with 30nm raised source/drain structures. Dual nitride/LTO spacers are used to isolate the source/drain SEG from the gate poly-Si.

REFERENCES:

[1] Kuo, J.B., K. Su, CMOS VLSI Engineering Silicon-on-Insular (SOI). Norwell, Ma: Kluwer, 1998, pp. 2–9.

Improved Hole Mobilities and Thermal Stability in a Strained-Si/Strained-$Si_{1-Y}Ge_y$/Strained-Si Heterostructure Grown on a Relaxed $Si_{1-x}Ge_x$ Buffer

S. Gupta, M.L. Lee, D.M. Isaacson, E.A. Fitzgerald
Sponsorship: MARCO MSD

A dual channel heterostructure consisting of strained-Si/strained-$Si_{1-y}Ge_y$ on a relaxed $Si_{1-x}Ge_x$ buffer ($y>x$), provides a platform with high hole mobilities (μ_{eff}) that depend directly on Ge concentration in the $Si_{1-y}Ge_y$ layer. Ge out-diffusion from the strained-$Si_{1-y}Ge_y$ layer into the relaxed $Si_{1-x}Ge_x$ buffer, which occurs during high temperature processing, reduces the peak Ge concentration in the strained-$Si_{1-y}Ge_y$ layer and degrades hole μ_{eff} in these dual-channel heterostructures.

We present a tri-layer heterostructure of strained-Si/strained-$Si_{1-y}Ge_y$/strained-Si grown on a relaxed $Si_{1-x}Ge_x$ buffer. The Ge diffusion coefficient in tensilely strained Si is very low, leading to much reduced Ge out-diffusion from the strained-$Si_{1-y}Ge_y$ layer in the tri-layer heterostructure. Numerical simulations were undertaken in order to investigate the diffusion characteristics of the dual channel. A diffusion coefficient of Ge that matches well with the existing literature values over an entire range of Ge concentration was used for the diffusion simulation. A new finite difference scheme, which has much improved accuracy over the ones described in literature, has also been used for the simulations.

Numerical investigations and SIMS results establish that tri-layer heterostructures retain a higher peak Ge concentration in the strained-$Si_{1-y}Ge_y$ layer than corresponding dual-channel heterostructures after identical thermal treatment. Ring-shaped MOSFETs were fabricated on both platforms and subjected to varying processing temperatures in order to compare the extent of μ_{eff} reduction with thermal budget. Hole μ_{eff} enhancements are retained to a much greater extent in a tri-layer heterostructure after high temperature processing as compared to a dual channel heterostructure. The improved thermal stability of a tri-layer heterostructure combined with improved hole μ_{eff} provides a platform for fabricating high μ_{eff} p-MOSFETs that can be processed over higher temperatures without significant losses in hole μ_{eff}.

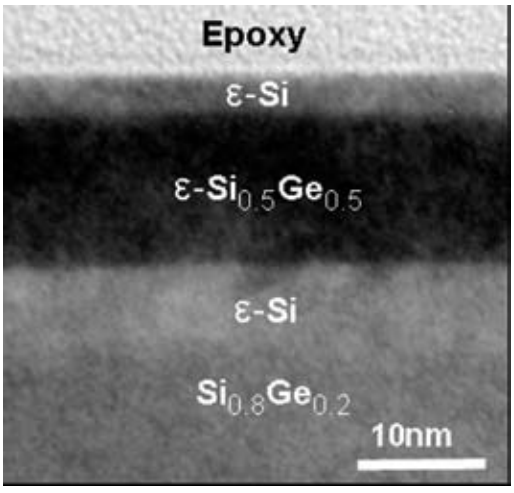

Figure 1: XTEM of a tri-layer heterostructure.

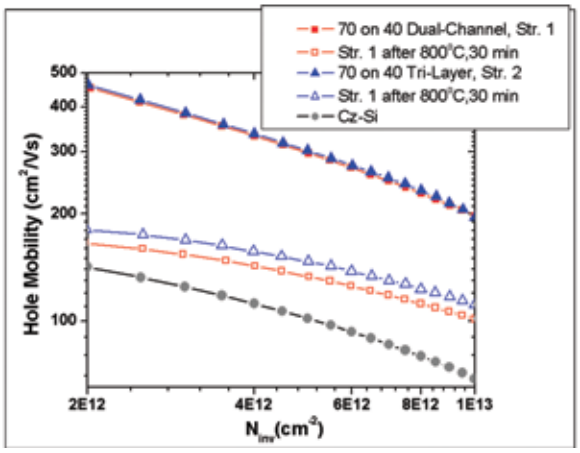

Figure 2: Mobility plot showing that higher enhancements are retained in a tri-layer heterostructure as compared to a dual -channel heterostructure, after similar high temperature processing.

Novel High Thermal Conductivity CMOS Platforms by Wafer Bonding and Layer Transfer from Relaxed SiGe Buffer

D.M. Isaacson, A.J. Pitera, N. Ariel, S. Gupta, E.A. Fitzgerald
Sponsorship: SMA, ARO

Over the past decade, the relaxed graded SiGe buffer has enabled the development of a multitude of novel CMOS-compatible strained-Si, -SiGe, and -Ge heterostructure platforms with enhanced carrier transport properties relative to bulk Si. However, one significant drawback to the relaxed graded SiGe buffer platform is the low thermal conductance of such a structure. This results in a local temperature increase near the device channel, a condition known as the self-heating effect. This self-heating effect is especially pronounced in high-power devices and can lead to significant reductions in both mobility and drain current.

As possible solutions to this self-heating problem, we report the creation of two CMOS-compatible platforms for high-power applications: strained-silicon on silicon (SSOS) and strained-silicon on silicon-germanium on silicon (SGOS). SSOS substrate has an epitaxially-defined, strained silicon layer directly on bulk silicon wafer without an intermediate SiGe or oxide layer. SSOS is a homochemical heterojunction, i.e. a heterojunction defined by strain state only and not by an accompanying compositional change, and therefore in principle SSOS may ease metal-oxide-semiconductor (MOS) strained Si fabrication as SiGe is absent from the structure. SGOS has an epitaxially-defined SiGe layer between the strained silicon channel and the Si substrate, which is necessary to prevent excessive off-state leakage in MOS devices due to overlap of the source-drain contacts and the interfacial misfit array. Plan-view transmission electron microscopy revealed edge-type interfacial misfit dislocation arrays with an average dislocation spacing of approximately 40 nm for both structures. This spacing indicates that the strained Si layer of SSOS is fully strained and that the SiGe layer of SGOS is fully relaxed. Complete relaxation of the intermediate SiGe layer in SGOS was confirmed by Raman spectroscopy, and since this layer is thin (<100nm), its inclusion is not expected to detrimentally affect the overall thermal conductivity of the structure.

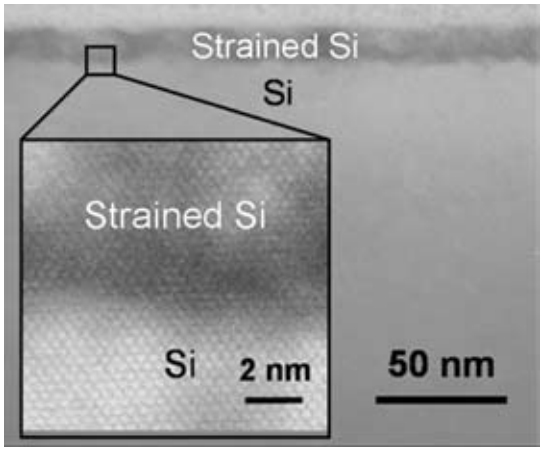

Figure 1: Cross-sectional transmission electron microscopy image of the strained-Si on Si (SSOS) heterostructure.

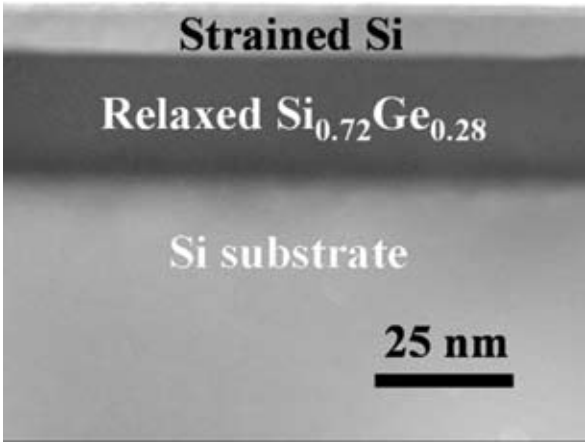

Figure 2: Cross-sectional transmission electron microscopy image of the strained-Si on SiGe on Si (SGOS) heterostructure .

Epitaxial Growth of SiGe Buffers on Si (111) and (110)

M.L. Lee, E.A. Fitzgerald, D.A. Antoniadis
Sponsorship: MARCO MSD

The band structure that a carrier experiences in a MOSFET inversion layer depends strongly on the crystallographic orientation of the substrate surface. Surface orientation also influences the relaxation and dislocation morphology of mismatched epitaxial semiconductor films. Recently, the emergence of local and global strain techniques to enhance VLSI circuit performance has brought about renewed interest in the influence of surface orientation on μ_{eff}, particularly Si(110) surfaces for *p*-FETs, and Ge(111) and (110) surfaces for ultra-scaled *n*-FETs [1]. The ability to control defect densities in SiGe buffers grown on arbitrary substrate orientations would allow the coupled effects of surface orientation and strain on μ_{eff} to be studied in greater detail.

Most dislocations in diamond cubic semiconductors are 60° a/2[101] total dislocations that are slightly dissociated into 90° and 30° Shockley partials. For compressive films on (111) and (110) substrates, the 90° a/6[211] dislocation leads the 30° partial and also experiences a larger resolved shear stress. Therefore, 60° dislocations in compressive films grown on (111) and (110) substrates can dissociate, resulting in stacking fault growth.

In PVTEM, we have observed high densities of dislocation pileups in SiGe layers grown on both (111) (Figure 1) and (110) substrate orientations. Cross-sectional TEM images and diffraction patterns indicate that these pileups consist of 90° a/6[211] partial dislocations that nucleate at the surface and glide to the hetero-interface on neighboring (111) glide planes, resulting in the formation of microtwins (Figure 2).

In general, low-mismatch SiGe layers grown on Si (111) and (110) exhibit dislocation densities several orders of magnitude greater than those grown on (001). Since relaxation processes on these substrate orientations tend to involve the glide of partial dislocations and the formation of stacking faults, achieving high quality SiGe buffer layers on Si (111) and (110) is intrinsically more challenging than on (001).

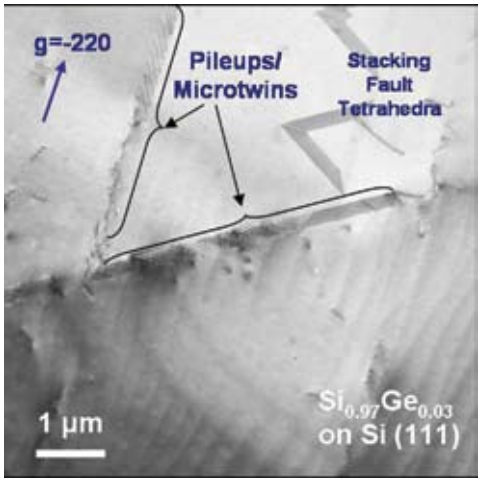

Figure 1: PVTEM of 1 µm thick $Si_{0.97}Ge_{0.03}$ film on Si (111) showing dislocation pileups and stacking fault tetrahedra.

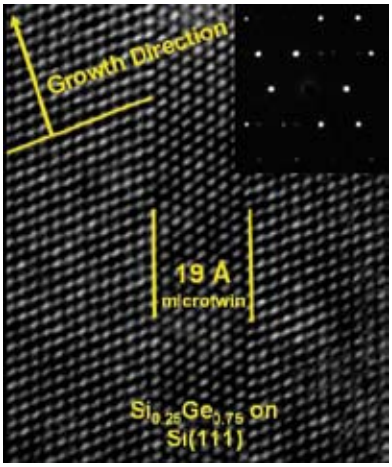

Figure 2: XVTEM of microtwin in $Si_{0.75}Ge_{0.25}$ grown on Si (111). *Inset*- Selected area diffraction pattern showing twin spots.

REFERENCES:

[1] Takagi, S., "Re-examination of Subband Structure Engineering in Ultra-Short Channel MOSFETs under Ballistic Carrier Transport," presented at Symposium on VLSI Technology Digest of Technical Papers, 2003.

Interdiffusion in Strained Si/Strained SiGe Heterostructure Devices

G. Xia, J.L. Hoyt

In the past decade, SiGe-based strain and bandgap engineering have received increasing attention for CMOS applications. Carrier transport is enhanced by applying strain in the Si channel, or by the use of strained SiGe as the p-MOSFET channel material, as in dual-channel and heterostructure-on-insulator (HOI) MOSFETs. One issue for these structures is interdiffusion at the strained Si/strained SiGe interface during processing, which degrades device performance by reducing strain and carrier confinement and increasing alloy scattering. To date, research on Ge diffusion has been focused on Ge self-diffusion in $Si_{1-x}Ge_x$ [1] and interdiffusion in compressively strained SiGe superlattices with low Ge fractions ($x < 0.25$) grown on Si [2]. Basic understanding of interdiffusion, such as Ge fraction, strain, and temperature dependence, and the influence of point defects generated during oxidation, nitridation, and other processes is inadequate. In addition, little data is available for SiGe interdiffusion in device structures, such as Strained Si/Strained $Si_{1-y}Ge_y$/relaxed $Si_{1-x}Ge_x$ with Ge content $y>0.3$.

In this work, interdiffusion is studied in Strained Si/Strained $Si_{1-y}Ge_y$/relaxed $Si_{1-x}Ge_x$ structures under various point defect injection conditions. In one experiment, Boltzmann-Matano analysis is used to obtain SiGe interdiffusivity experimentally. With transient diffusion taken into account, a TSuprem4 interdiffusion model is set up based on the interdiffusivity obtained. This model will be tested by application to various annealing conditions, especially to rapid thermal processing (RTP) of dual channel and HOI structures. Figure 1 shows examples of Ge profiles used for Boltzmann-Matano analysis, for Ge fraction up to 0.4. The interdiffusivity model is based on the interdiffusion coefficients obtained from Boltzmann-Matano analysis (Figure 2), which has a similar form to the model used in [2] for compressive SiGe at lower Ge fractions.

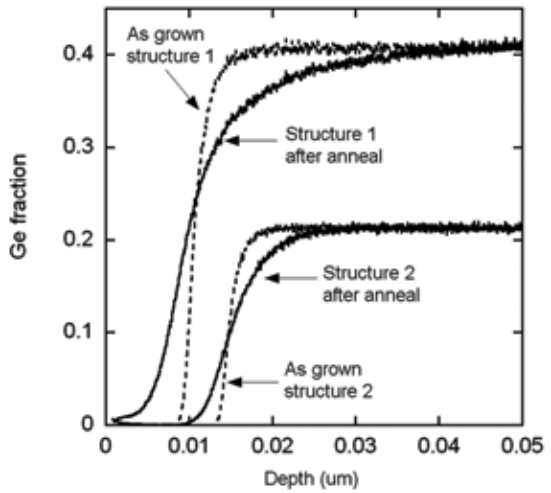

Figure 1: Ge profiles measured by SIMS for Boltzmann-Matano analysis. Both samples are annealed at 920C for 60min in nitrogen.

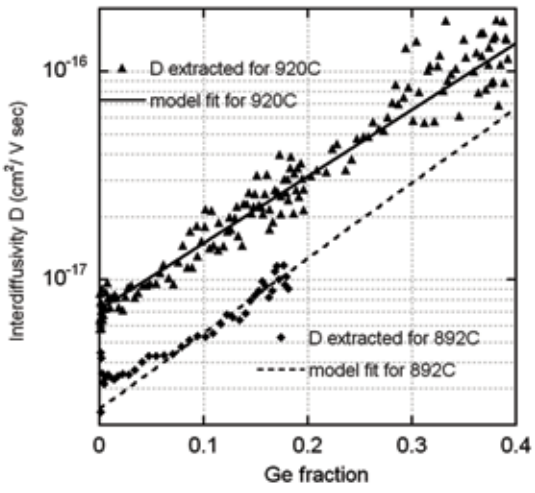

Figure 2: SiGe interdiffusivity (D) extracted from Ge profiles similar to those in Figure 1 (symbols), and model fit (lines) at two different temperatures.

REFERENCES:

[1] Aubertine, D.B., P. C. McIntyre, "Influence of Ge Concentration and Compressive Biaxial Stress on Interdiffusion in Si-Rich SiGe Alloy Heterostructures," *J. Appl. Phys.,* vol 97, n 1, pp. 013531-1-013531-10, January 2005.

[2] Zangenberg, N.R., J. L. Hansen, J. Fage-Pedersen, A. N. Larsen, "Ge Self-Diffusion in Epitaxial $Si_{1-x}Ge_x$ Layers," *Physical Review Letters*, v 87, pp. 125901-1-125901-4, September 2001.

Extraction of Band Offsets in Strained Si/Strained $Si_{1-Y}Ge_y$ on Relaxed $Si_{1-X}Ge_x$ Dual-Channel Enhanced Mobility Structures

C. Ní Chléirigh, C. Jungemann, J. Jung, O. Olubuyide, J.L. Hoyt
Sponsorship: MARCO MSD, SRC, Applied Materials

In this work, for the first time, the valence band offset, ΔE_V, between strained Si and strained $Si_{1-y}Ge_y$ on relaxed $Si_{1-x}Ge_x$, has been measured using a combination of experimentation and modeling. Such structures have been shown to offer large mobility enhancements for both electrons and holes, and knowledge of the band parameters is critical in order to optimize and predict device behavior [1-3]. The positions of the conduction band edge in the strained Si and the valence band edge in the strained $Si_{1-y}Ge_y$ significantly affect the effective bandgap of the structure and can be used to tune the threshold voltage of both n- and p-MOSFETs for use with a single workfunction metal gate [4]. Theoretical predictions of these band parameters are uncertain by ±100 meV [5]. P-type metal-oxide-semiconductor (MOS) capacitors were fabricated on epitaxial structures containing strained $Si_{1-y}Ge_y$ layers ($0.4 < y < 0.8$) grown on relaxed $Si_{1-x}Ge_x$ layers ($0.2 < x < 0.4$). DEV was extracted by fitting simulated results to the experimental capacitance-voltage (C-V) characteristics of the MOS capacitors (Figures 1 and 2). The impact of the valence band edge density of states, N_V, on the extraction of ΔE_V is investigated. The effect of these band parameters on threshold voltage and subthreshold slope of a dual channel p-MOSFET is demonstrated using simulations.

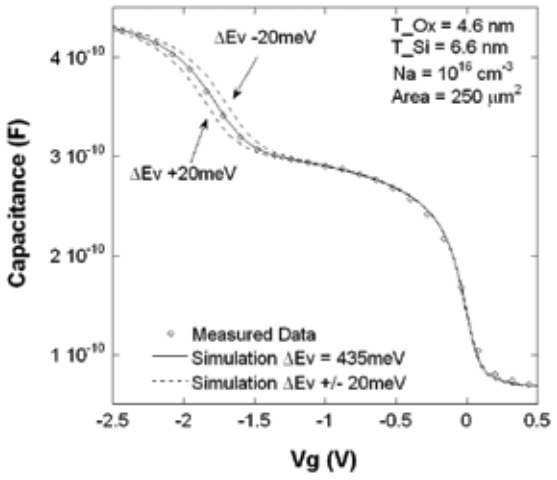

Figure 1: ΔE_V extraction and sensitivity for strained Si, strained $Si_{0.4}Ge_{0.6}$ on a relaxed $Si_{0.7}Ge_{0.3}$ substrate. Measured data with simulation of $\Delta E_V = 435$meV ± 20meV.

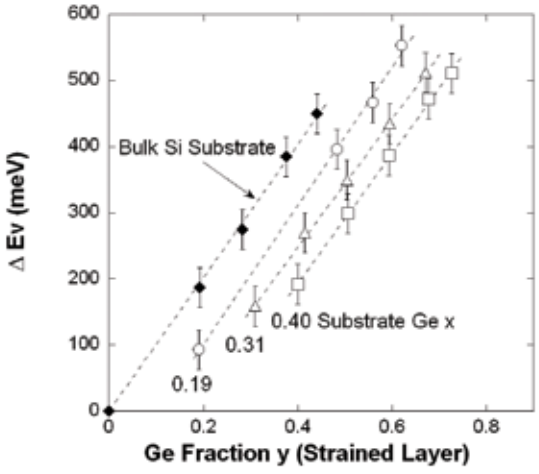

Figure 2: Extracted ΔE_V for strained Si on strained $Si_{1-y}Ge_y$ on various relaxed $Si_{1-x}Ge_x$ substrates.

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Electron and Hole Mobility in Thin-Body Strained Si/Strained SiGe/Strained Si Heterostructures on Insulator

I. Åberg, J.L. Hoyt
Sponsorship: MARCO MSD, SRC, Applied Materials

Geometric scaling of MOSFETs can no longer provide all the current drive enhancements necessary to maintain historic performance gains. Channel strain and novel materials may provide additional transport improvements. At the same time, fully depleted or double gate technologies may be required to maintain electrostatic integrity in deeply scaled MOSFETs. To address these issues, fully depleted MOSFETs were fabricated on strained Si/strained SiGe (46% Ge)/strained Si heterostructures on insulator (HOI), demonstrating both high electron and hole mobility enhancements while maintaining excellent subthreshold swing of 66-70 mV/dec. Subthreshold characteristics are improved compared to bulk dual-channel MOSFETs [1]. The total thickness of the heterostructure on insulator is less than 25 nm. At an inversion charge density of $1.5x10^{13}$ cm^{-2}, mobility enhancements of 90% and 107% are obtained for electrons and holes respectively. The tri-layer heterostructure on insulator was fabricated by using a bond and etch-back technique [2]. Electron mobilities are enhanced by a factor of 1.8-2X over regular SOI (Figure 1) as in the case of strained Si directly on insulator, while hole mobilities are enhanced by ~2X even at high inversion charge densities depending on the Ge concentration of the buried layer, strain level, and cap thickness design (Figure 2) [2]. For example, for a cap thickness of 4 nm, hole mobility improves when the Ge concentration of the buried SiGe channel increases from 35% to 46%.

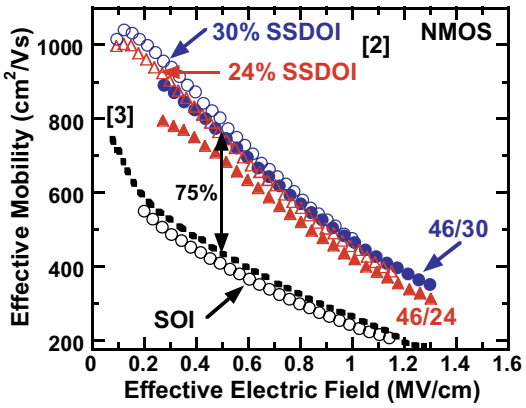

Figure 1: NMOS effective mobility as a function of Eeff. $\mu_{eff}=L/W*I_D/(Q_{inv}V_{DS})$ was extracted by integration of C_{GC}, measuring I_D at an applied V_{DS}=50mV. The universal mobility is indicated [3].

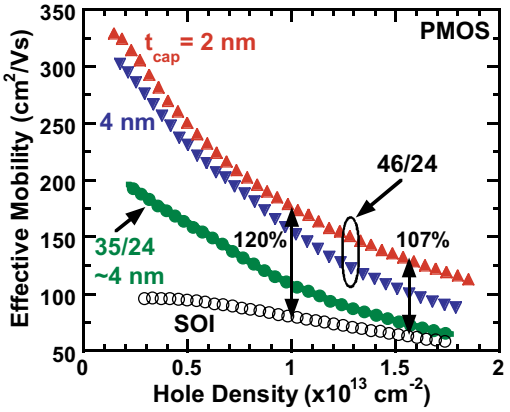

Figure 2: PMOS effective mobility as a function of N_{inv}. The enhancement compared to the SOI control at N_{inv}= $1x10^{13}$ cm^{-2} is 120%. As the Ge content of the buried channel is increased (keeping the cap thickness constant), the mobility is increased.

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Germanium-on-Insulator Fabrication by Hydrogen-Induced Layer Transfer

J. Hennessy, D.A. Antoniadis
Sponsorship: MARCO MSD

Germanium is considered a promising material for high performance CMOS devices because it possesses higher bulk electron and hole mobility than Si. Similarly, the on-insulator structure is also a good candidate for improved device performance due to the electrostatic benefits it holds over bulk technologies. This project is meant to combine both advantages in the fabrication of Germanium-on-Insulator (GeOI) substrates.

The initial goal of this work is to develop a process to transfer a high quality Ge layer to a less expensive and more readily available Si handle wafer. This goal is accomplished by first implanting a bulk Ge transfer wafer with a high dose of hydrogen, and then direct-bonding the Ge wafer to an oxidized Si handle wafer. As the bonded wafer pair is annealed, the activation of the implanted hydrogen leads to the formation of micro-cracks near the peak of the implant and the eventual exfoliation of a thin Ge layer from the transfer wafer (Figure 1). By incorporating an epitaxial etch-stop layer in the transfer wafer, the implant-damaged Ge can be selectively removed by wet etching. This technique also allows for arbitrarily thin GeOI because the device layer is defined epitaxially and not by a polishing or etching step.

The most challenging aspect of this approach is the mismatch of the thermal coefficients of expansion between Ge and Si. A typical hydrogen activation anneal is performed at 300-400°C for Si applications. At this temperature, the Ge/Si bonded pair will break due to the great increase in thermal stress. For the fabrication of GeOI, it is necessary to reduce the temperature at which layer transfer will occur. One approach being investigated is the use of a second SiGe epitaxial layer as a gettering layer for the implanted hydrogen (Figure 2). This gettering layer is seen to reduce the time required for layer exfoliation at a given annealing temperature. Future work on this project will include device fabrication and analysis on partially depleted and fully depleted GeOI substrates.

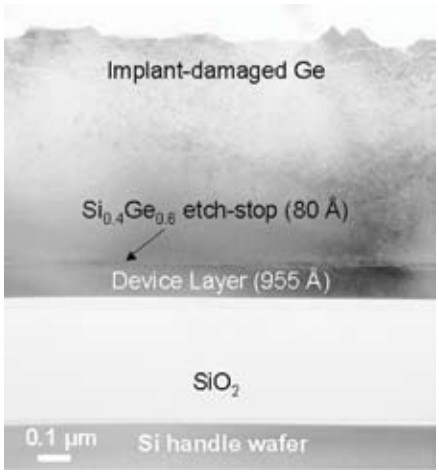

Figure 1: Cross-sectional TEM of GeOI structure immediately after layer transfer.

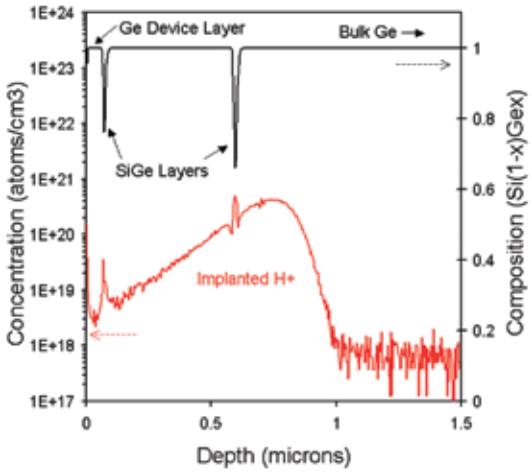

Figure 2: SIMS analysis of a hydrogen-implanted transfer wafer with a double etch-stop structure.

RTP Growth of Germanium Oxynitride for MOSFET Fabrication

A. Khakifirooz, A. Ritenour, D.A. Antoniadis
Sponsorship: MARCO MSD

Germanium channel MOSFETs are considered one of the promising options for high performance CMOS technology because of the high electron and hole mobility, as well as high ballistic carrier injection velocity in germanium. One of the most important challenges in integrating the Ge MOSFETs is the formation of high quality gate dielectrics on the Ge surface. Several attempts have been made in recent years to deposit high-k dielectrics on Ge [1, 2]. However, by far the highest mobility reported for Ge MOSFETs is obtained using a thermally grown germanium oxynitride [3]. A rapid thermal processing (RTP) version of such processes is of interest for providing realistic EOT values for futuristic devices, while offering the possibility of obtaining high carrier mobility values similar to those reported earlier for Ge MOSFETs with an oxynitride dielectric grown in a furnace. Germanium oxynitride gate dielectrics are grown on 6" (100) n-type germanium wafers as well as relaxed p-type Ge layers epitaxially grown on silicon. A special "RCA-equivalent" cleaning process has been developed to minimize Ge loss during the cleaning step and to give reasonably smooth surface (R_a ~ 0.25 nm). Oxidation is performed in an RTP chamber at 550°C for 30-60 s and in oxygen, followed by a nitridation step at 600°C for 60-300 s in ammonia. From spectroscopic ellipsometry the thickness of the oxynitride layer is determined to be 50±5 Å. Upon nitridation, the refraction index of the film measured at 600 nm is increased from 1.3 to 1.7, indicating the oxynitride formation. From CV measurements the effective electrical oxide thickness is about 30 Å, corresponding to a dielectric constant of about 6.5. MOS capacitors made by depositing Al gates on as grown oxynitride dielectrics show a kink in the CV characteristics measured at lower frequencies. A forming gas annealing step at 400°C effectively removes this kink and reduces the density of surface states. The midgap D_{it} extracted from the conductance method is roughly 8×10^{11} cm^{-2}. PMOS transistors were fabricated with a TiN metal gate and show a peak effective mobility of 280 cm^2/V.s which corresponds to 40% enhancement over p-channel Si MOSFETs.

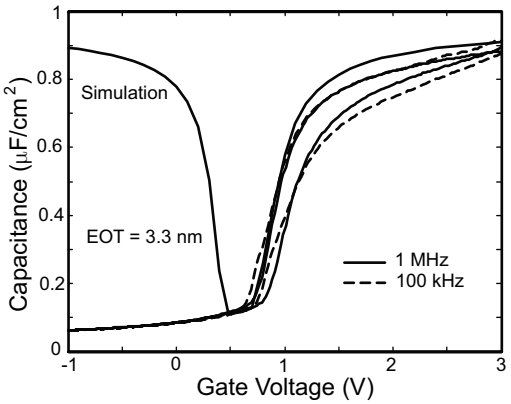

Figure 1: CV characteristics of the MOS capacitor fabricated using RTP Ge oxynitride and after a post-metal annealing in forming gas.

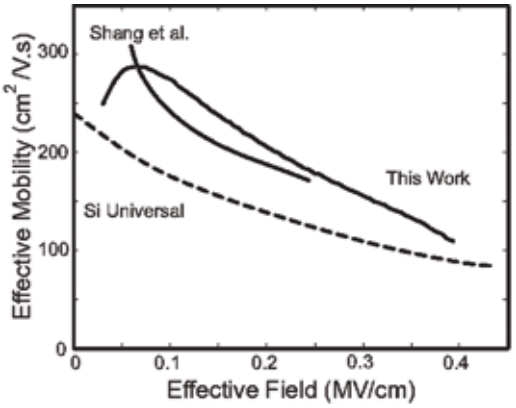

Figure 2: Effective hole mobility in the Ge MOSFETs. An enhancement of about 40% is observed compared to silicon.

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Bulk Germanium MOSFETs Using High-K Gate Dielectrics

A. Ritenour, R.Z. Lei, D.A. Antoniadis
Sponsorship: MARCO MSD

The advent of high-k gate dielectrics provides a new opportunity to consider semiconductors other than silicon for future ultra-scaled MOSFETs. Germanium has started to receive attention because it simultaneously offers significant enhancements in bulk carrier mobility relative to silicon; however, the inherent instability of germanium oxide makes interface engineering particularly challenging. Advanced techniques such as molecular beam deposition (MBD) and atomic layer deposition (ALD) are being explored as options for gate stack deposition. Figure 1 shows the transfer characteristics for a germanium p-MOSFET with an MBD GeON-HfO2-TaN gate stack. Figure 2 shows the extracted hole mobility for this device. MBD gate stack deposition was performed by A. Dimoulas at the NCSR in Greece.

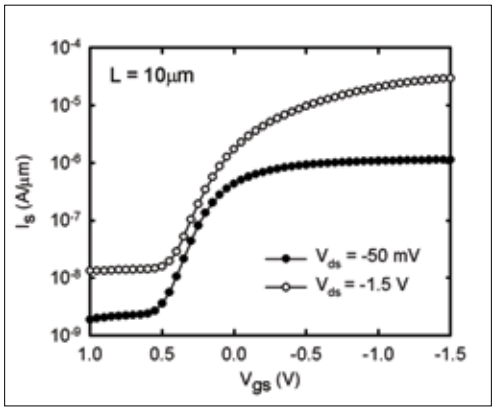

Figure 1: Typical as-measured I_s-V_g characteristics for bulk Ge p-MOSFETs with MBD GeON-HfO2-TaN gate stack.

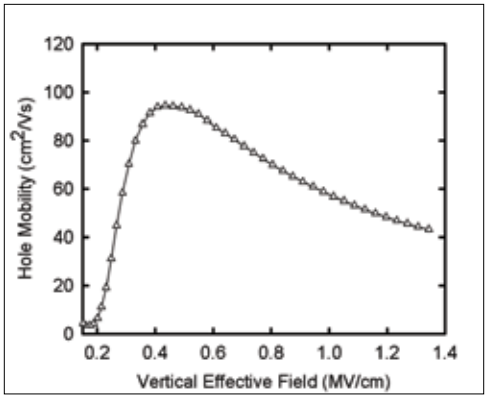

Figure 2: Extracted hole mobility for Ge MBD p-MOSFET.

Modeling and Simulation of Advanced Transistors with Novel Channel Materials

O.M. Nayfeh, D.A. Antoniadis
Sponsorship: MARCO MSD, SRC

Recent experimental results [1] have demonstrated significant mobility enhancement in transistors such as the dual channel heterostructure-on-insulator (HOI). Germanium is optimally incorporated in the channel to provide increase in mobility. The increase in mobility in an HOI structure is due to Germanium's bulk nature, and also from strain effects due to the lattice mismatch between silicon and germanium. In this work, we examine by modeling and simulation, electrostatics and transport of such devices, in order to understand the physical mechanisms that contribute to enhanced mobility as compared to Silicon-On-Insulator counterparts. Moreover, we determine the performance limits of such channel materials for integration in deep sub 45 nm transistors.

Modeling of such advanced devices requires the determination of key electrostatic parameters; either theoretically, or from measurements of experimental structures. These parameters are affected by strain, quantum-mechanical, and high-field effects. Figure 1 shows the Hole density in an HOI structure at a cut through the center of the channel. The silicon cap thickness is 7 nm and the SiGe layer is ~12.5nm. The gate potential is –1.7 V. Shown is the solution from a Schrödinger/Poisson calculation, and also from the calibration of the Density-Gradient quantum mechanical correction model. Figure 2 shows the respective Gate-Capacitance vs. Gate-Voltage curves. Both plots show good agreement between the two models after calibration.

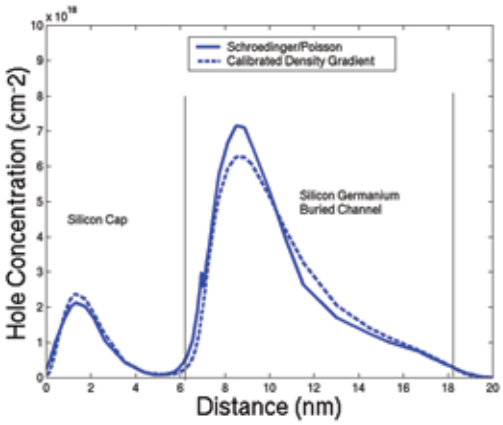

Figure 1: Cut of simulated Hole density through the center of the channel of an HOI device. Shown are the Schrödinger/Poisson calculation, and also the result from the calibration of the Density Gradient quantum mechanical correction model. The gate potential is –1.7 V.

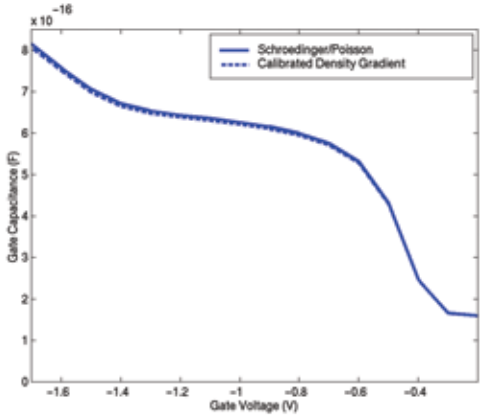

Figure 2: Respective Capacitance-Voltage curves of the device in Figure-1. Notice the hump in the curves due to population of the Silicon cap at high gate fields. Calibration of the DG provides good agreement with the Schrödinger/Poisson calculation.

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An Equivalent Circuit Model of a Faraday Cage for Substrate Noise Isolation

J.H. Wu, J.A. del Alamo
Sponsorship: Applied Materials Fellowship

Substrate crosstalk between digital, analog, and RF blocks is a major problem for System-on-Chip applications. A promising approach that is both compact and effective up to millimeter-wave frequencies is a Faraday cage embedded in the substrate that surrounds a noisy or sensitive circuit. This Faraday cage uses through-wafer vias with solid copper cores that are shorted at the top and to the backside ground plane (Figure1a) [1]. These Faraday cages significantly improved isolation by 41 dB at 1 GHz, 30 dB at 10 GHz, and 16 dB at 50 GHz with respect to a reference at a distance of 100 µm [1]. In order to better understand the exceptional performance of this Faraday cage, we have developed a physics-based equivalent circuit model [2].

We developed a model for the Faraday cage (Figure 1b) starting from the simple substrate model in [3]. The lumped elements R_1 and C_1 represent the substrate between the transmitter and receiver pads. R_3 and C_3 represent the substrate from the surface to the backside of the wafer. We modified the substrate model in [3] to include the effect of the Faraday cage by exposing a node that corresponds to the center of the substrate between the transmitter and receiver pads and shunting this center node to ground. The entire effect of the Faraday cage is captured by lumped elements R_v and L_v. The smaller R_v and L_v are, the more effective the shunting of the substrate between the transmitter and receiver, resulting in a reduction in crosstalk.

The equivalent circuit model was simulated using Agilent ADS. Figure 2 shows S_{21} measured and simulation data for the reference and Faraday cage structures. The simulation data matches the experimental data well into the millimeter-wave regime. This model will be useful in evaluating the effectiveness of Faraday cages in circuits.

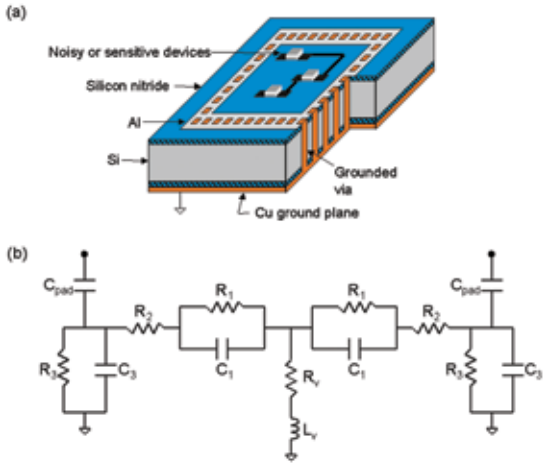

Figure 1: (a) Schematic diagram of a Faraday cage constructed using through-wafer vias. (b) Equivalent circuit model of the Faraday cage.

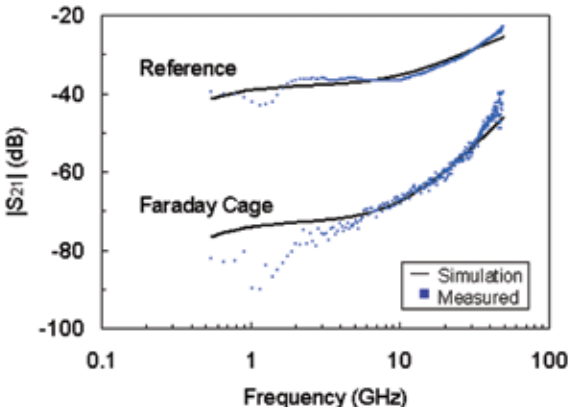

Figure 2: S_{21} of the reference and Faraday cage at 100-µm pad separation distance.

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Approaching the InP Lattice Constant on GaAs

N.J. Quitoriano, E.A. Fitzgerald
Sponsorship: Walsin Lihwa

Integrating different materials onto a Si platform brings new functionality to Si. InP on Si could allow the integration of optical and electronic (e.g. CMOS) devices. By growing high-quality GaAs on Si, our group has been able to demonstrate a GaAs laser grown on Si. Our research goal is to expand the lattice constant beyond GaAs and grow high-quality InP on GaAs. Having explored many materials systems and methods (e.g. InGaAs, InGaP, and InGaAlAs), to date, we have grown low dislocation-density $In_{(0.43)}Al_{(0.57)}As$ on GaAs with a dislocation-density of 1.4E6/cm^2, more than an order-of-magnitude less dislocations than typical commercial metamorphic buffers. After achieving high-quality InP on GaAs, we will work to grow InP on Si. Bringing low-defect density InP onto Si may bring high-speed InP based devices into new markets because the processing and material cost for a given area will be drastically reduced and allow for high-frequency and/or low-power operation.

Figure 1: Plan-view TEM of $In_{(0.43)}Al_{(0.57)}As$ on GaAs with a dislocation density of 1.4E6/cm^2.

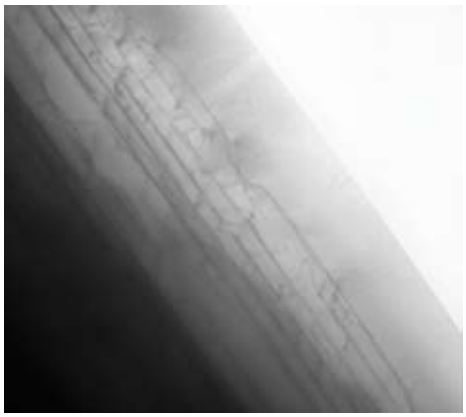

Figure 2: Cross section of $In_{(0.43)}Al_{(0.57)}As$ on GaAs.

The Impact of Recess Length on the RF Power Performance of GaAs PHEMTs

M.F. Wong, J.A. del Alamo, A. Inoue, T. Hisaka, K. Hayashi
Sponsorship: Mitsubishi Electric

Due to their excellent performance, reasonable cost, and relative technological maturity, AlGaAs/InGaAs Pseudomorphic High Electron Mobility Transistors (PHEMTs) constitute an attractive choice for RF power applications. Theoretically, increasing the gate-to-drain recess length (L_{RD}) should lead to an increase in breakdown voltage, which ought to allow the selection of a higher drain voltage bias point and subsequently yield higher output power. However, we have experimentally found that not to be the case. In fact, beyond a certain value, we have observed that further increasing L_{RD} results in a decrease in saturated output power and peak power-added efficiency (PAE), (Figure 1). In addition, we have observed a decrease in output power and peak PAE with increasing frequency that cannot be accounted for by existing large signal models.

In our investigation into the origins of this anomalous behavior, we have identified two contributing explanations. First, a comparison of the output characteristics reveals an increase in $V_{DS,SAT}$ when L_{RD} is increased; this trend reduces the peak-to-peak voltage swing possible during RF operation and adversely affects the output power that can be delivered from the device.

Secondly, we have observed a reduction in both gain and short-circuit current-gain frequency (f_T) with increasing L_{RD}. To gain further insight into the reduction of f_T, we have performed a delay time analysis and extracted the drain delay, which is associated with the electron drift through the depletion region on the drain side of the device [1]. Figure 2 shows a plot of the intrinsic delay versus drain voltage, where the minimum intrinsic delay is the same for all four devices with different L_{RD} and represents the transit of electrons in the gate region. As the drain voltage is increased, the depletion region widens toward the drain, contributing an additional delay associated with the electron drift through this region and hence, increasing the intrinsic delay. This drain delay becomes longer as L_{RD} is increased and appears to be a significant limitation at high frequency, large drain voltage operation.

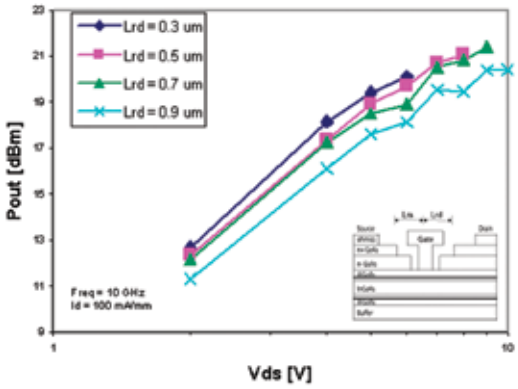

Figure 1: Saturated output power versus drain voltage for different L_{rd} devices. Inset: Schematic cross-section of the GaAs PHEMT under study.

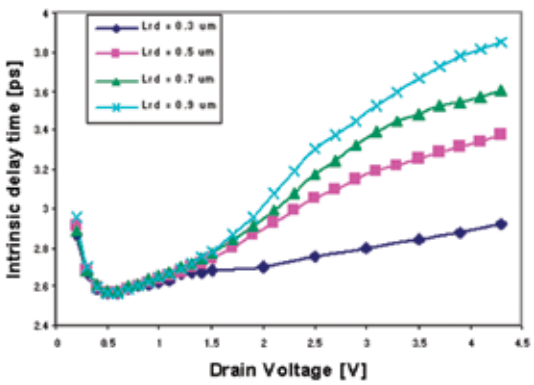

Figure 2: Intrinsic delay time of GaAs PHEMTs versus drain voltage for different L_{rd} devices. Vgs was chosen to correspond with the value with the lowest intrinsic delay time.

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Electrically-Induced Changes in Threshold Voltage and Source Resistance in RF Power GaAs PHEMTs

A.A. Villanueva, J.A. del Alamo
Sponsorship: Mitsubishi Electric

GaAs Pseudomorphic High-Electron Mobility Transistors (PHEMTs) have great potential for RF power applications. A major issue with these devices is electrical reliability–the gradual degradation of certain electrical characteristics that occur under prolonged high-voltage biasing. The degradation of the extrinsic drain (observed via an increase in the drain resistance R_D and a decrease in the maximum drain current I_{max}) is usually of primary concern; however, under high-bias stress, significant shifts in the threshold voltage V_T and in the source resistance R_S are also observed. Since such changes affect the long-term electrical performance of the device, it is important to understand the underlying mechanisms behind these changes.

In our study, experimental RF power PHEMTs were electrically stressed using a bias-stressing scheme that kept the impact-ionization rate constant [1]. During stressing, the devices were characterized at frequent intervals. In our experiments, we observed negative shifts in V_T (Figure 1) and decreases in R_S (Figure 2), which were both accelerated with increasing temperature. Both the changes in V_T and R_S tended to saturate with stressing and could be modeled well by an exponential fit. Additional tests showed that the V_T shift was recoverable with unbiased storage at room temperature. This all makes ΔV_T consistent with a trapped electron recombination mechanism occurring under the gate, as previously identified in [2]. In this mechanism, the trapped electrons recombine with holes generated from impact ionization on the drain side of the device. As for R_S, through additional experiments on simple test structures, we were able to attribute the decrease in R_S to an increase in sheet carrier concentration (n_s) on the source. This suggests the presence of a similar electron-trapping and recombination mechanism on the source side. All these findings provide a better understanding of the cause for these device instabilities and thus, should be instrumental in developing effective solutions to this problem.

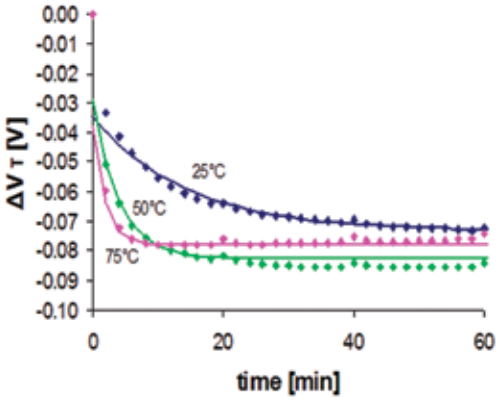

Figure 1: Time evolution of the threshold voltage shift of GaAs PHEMTs stressed at I_D=400 mA/mm, and $V_{DG0}+V_T$ = 6.0 V, at 25, 50, and 75°C in N_2. Solid lines show exponential fits to data.

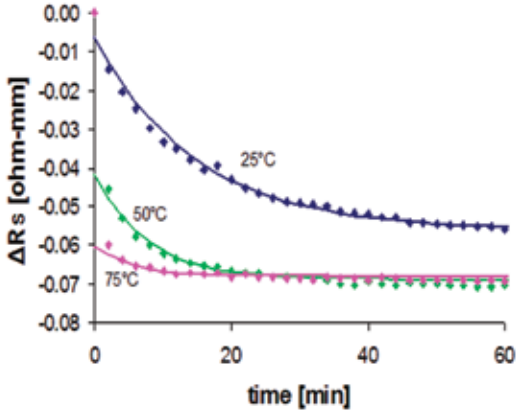

Figure 2: Time evolution of the source resistance decrease of GaAs PHEMTs stressed at I_D=400 mA/mm, and $V_{DG0}+V_T$ = 6.0 V, at 25, 50, and 75°C in N_2. Solid lines show exponential fits to data.

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InP-Based HEMTs for Large Scale Logic Applications

N. Waldron, J.A. del Alamo
Sponsorship: MARCO MSD

InP High Electron Mobility Transistors (HEMTs) have been shown to have the best intrinsic frequency performance of all the families of semiconductor devices (Figure 1). However, this superior intrinsic performance has not translated into the best circuit or system performance. Much of the reason for this is that these devices have been developed for millimeter wave rather than digital applications, resulting in a large extrinsic footprint and high parasitics. In contrast Si CMOS, which dominates the digital IC market, has benefited from aggressive gate scaling coupled with close attention to extrinsics and packing density. However, CMOS even now is approaching the end of the scaling roadmap, and more and more radical changes in the design of logic technology can be expected. Considering the current trend towards heterogeneous integration of various material systems, e.g. SiGe on Si, InAlAs on GaAs, the time perhaps has come to investigate III-V FETs as a post-CMOS logic technology. Of all III-V systems, the InAlAs system closely lattice-matched to InP is the most promising, and that is the one we are investigating in this project.

In order to realize the potential of InP-based HEMTs in large scale digital circuits, it is necessary to address the problems of the extrinsic resistances and capacitances that the non self-aligned design and large footprint bring about. To this end, we have designed a device architecture that incorporates a novel shallow trench isolation and self-aligned gate scheme (Figure 2). The BCB shallow trench design provides a low capacitive isolation scheme while maintaining a planar surface. The self-aligned gate process reduces the parasitic source and drain resistances with the added benefit of reducing the device footprint. The non-alloyed tungsten ohmic contacts allow for well-defined contact geometries. The process architecture offers the promise of a reliable, highly manufacturable process needed to realize the complex circuits required for large scale digital applications.

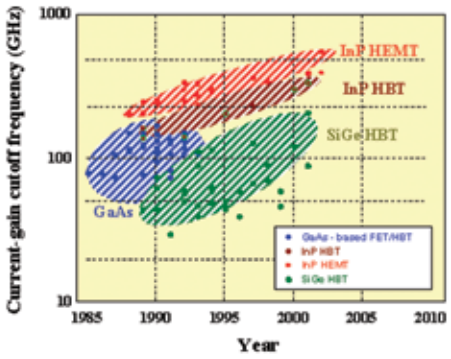

Figure 1: f_T of InP HEMTs compared to other III-V devices and SiGe HBTs. InP HEMTs have the best intrinsic performance. [Courtesy of T.Enoki, NTT].

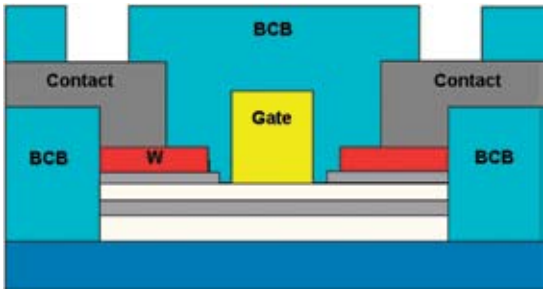

Figure 2: Cross section of the proposed new device architecture. Features include: BCB planar isolation, a self-aligned gate, and non-alloyed ohmic contacts. The architecture has the flexibility of being compatible with a wide variety of heterostructure designs.

Concepts and Devices for Micro-Scale Thermo-Photovoltaic Energy Conversion

H.K.H. Choy, C.G. Fonstad, Jr., in collaboration with R. Dimatteo (Charles Stark Draper Laboratory)
Sponsorship: Charles Stark Draper Laboratory

The first order proximity enhancement of thermo-photovoltaic (TPV) energy conversion that we and the C. S. Draper Laboratory (CSDL) demonstrated for the first time several years ago [1, 2] leads to a dramatic and important increase in energy conversion rate, but only a modest increase in the efficiency of the conversion process. The present challenge is to use the micro-scale geometry (in which the hot and cold surfaces are in extreme proximity) to increase the efficiency of TPV as significantly as we have increased the conversion rate.

Our work supports the CSDL effort on micro-scale thermo-photovoltaic (MTPV) electrical power sources. We have provided InAs-based MTPV cells to the CSDL effort, we have analyzed the impact of the enhancement effect on TPV cell performance, and we have evaluated more sophisticated, quantum-effect-based phenomenon that can be used to enhance significantly the energy selectivity of the energy transfer, and thereby dramatically increase the efficiency of the thermal to electrical energy conversion. We have most recently also begun work on dot-junction, back-side illuminated solar cells, and in the past year we designed an original InGaAlAs-on-InP heterostructure, shown in Figure 1, suitable for fabricating high performance dot-junction, back-side illuminated solar cells. The final n+ InGaAs layer is the n-side of the junction and a low resistance contact layer. The InGaAlAs layers shield the minority carriers created in the wide, p-type InGaAs light absorbing layer from surface recombination; the Al composition is graded to eliminate any barrier to electron flow from the absorbing layer to the n-side of the junction. The lowest p+ InGaAs layer reduces resistance as carriers flow laterally to ohmic contacts made to the p-side of the junction. The first sample of this heterostructure has been grown and has been given to CSDL researchers for device fabrication and testing.

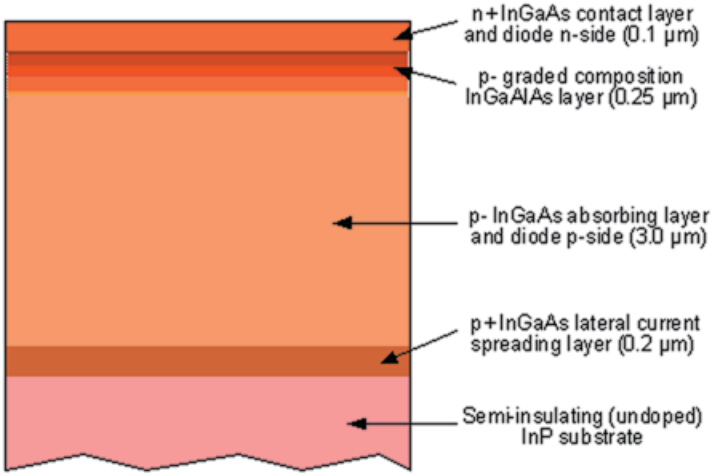

Figure 1: The layer structure for dot-junction, back-illuminated TPV and MTPV cells

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[2] Pan, J.L., H.K.H. Choy, C.G. Fonstad, Jr., "Very Large Radiative Transfer Over Small Distances from a Black Body for Thermo-Photovoltaics," *IEEE Trans. Electron Dev.*, 47 (2000) 241-249.

Temporal and Spatial Current Stability of the Smart Field Emission Arrays

C.-Y. Hong, A.I. Akinwande
Sponsorship: CreaTV Micro Tech, NIH, DARPA

Field emission can be described as two sequential processes—the flux of electrons to the emitter surface followed by the transmission of electrons through the surface barrier. Either of these processes could be the determinant of the emission current. Emission current instability and current non-uniformity could be explained by the variation in the electron transmission process. Unstable emission current is due to absorption/desorption of gas molecules on the emitter surface (barrier height variation), and non-uniform emission is usually due to spatial variation of tip radius (barrier width change). These problems could be solved if the emission current is determined by the electron supply to the emitter surface instead of the electron transmission through the surface barrier. In this work, we use the inversion layer of a MOSFET to control the electron supply. It moves the current controlling barrier from the tip emitter surface (semiconductor/vacuum interface), which is susceptible to adsorption/desorption processes and spatial variation, to the source/channel interface (pn junction barrier), which is immune to adsorption/desorption and spatial variation.

Emission current stability and the spatial uniformity of field emission devices are improved when a lightly doped drain-MOSFET (LD-MOSFET) is integrated with a field emission array (FEA). At comparable current levels, the emission noise (ΔI/I) decreased from 16.9 % to 1.8%. Emission current fluctuation was reduced in the integrated device compared to the FEA device even in the presence of gasses (Figure 1). Spatial current uniformity was achieved in the integrated MOSFET/FEA devices at different wafer positions (Figure 2) and for different array sizes. The results are explained by a two-step field emission process, which consists of an electron supply step determined by the MOSFET inversion layer and an electron transmission step determined by the field emission barrier width. The device structure also results in low voltage control of emission current.

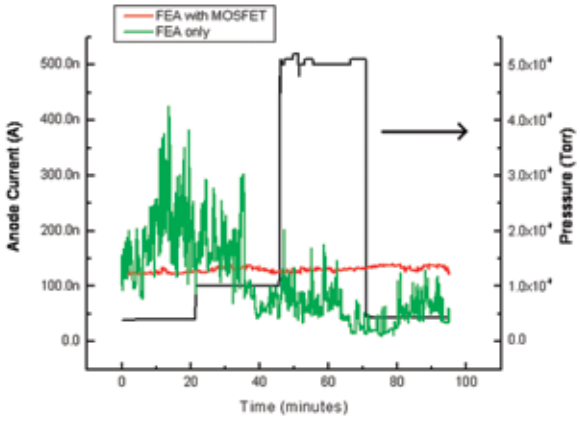

Figure 1: Emission current stability in an integrated LD-MOSFET/FEA device with and without MOSFET control in nitrogen.

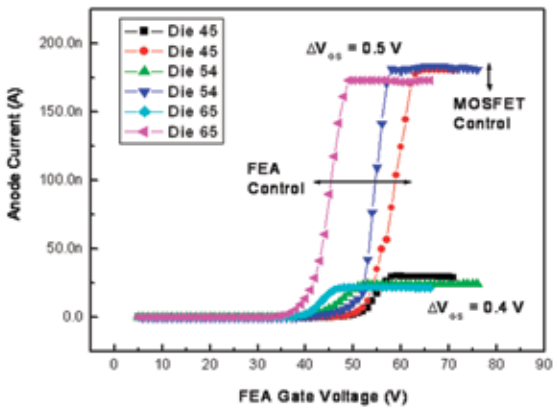

Figure 2: Spatial emission current uniformity in the integrated devices on different positions of the wafer. ΔV is 0.5 V (anode current is 170 nA) and 0.4 V (anode current is 25 nA).

Double-Gated Silicon Field Emission Arrays

L-Y. Chen, A.I. Akinwande
Sponsorship: CreaTV Micro Tech, NIH, DARPA

There is a need for massively parallel, individually addressed and focused electron sources for applications such as flat panel displays, mass storage, and multi-beam electron beam lithography. Because of this need, double-gated FEAs have drawn much attention in the past decade for their effective beam collimation ability. Among the approaches, Dvorson, Tang, Itoh, and Py discussed and showed that a local and out-of plane (L/OP) focal electrode provides the best focusing albeit at a slightly higher gate voltage [1-4]. This project fabricates and characterizes L/OP double-gated field emission devices with high aspect ratio. One of the gates extracts the electrons while the second gate focuses the electrons into small spots. High aspect ratio silicon field emitters were defined by reactive ion etching of silicon followed by multiple depositions of polycrystalline oxide insulators and silicon gates. The layers were defined by a combination of lithography, chemical mechanical polishing, and micromachining. We obtained devices with 0.4μm gate aperture and 1.2μm focus aperture. The anode current has very little dependence on the focus voltage, and the ratio of the focus field factor to the gate field factor β_F / β_G is 0.015. Scanning electron micrographs (SEM) of the devices, numerical simulation, and spot size measurements on a phosphor screen confirmed these results. Figure 1 and Figure 2 prove that the gate has a stronger effect on the initial beam spread than the focus gate. An e-beam resist, PMMA, was successfully exposed using the FEA device as an electron source.

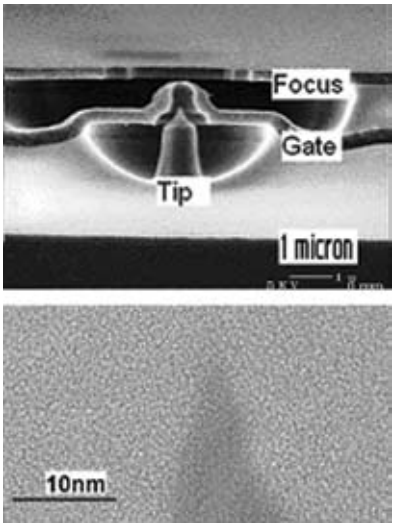

Figure 1: (Top) SEM picture of the cross section of the completed device. (Bottom) Transmission Electron Microscopy (TEM) picture of the sharp tip. According to the TEM, the tip has about 3nm tip radius.

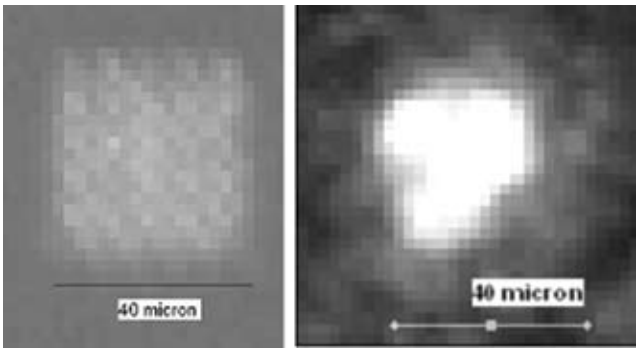

Figure 2: (Left) An optical microscope photo of an original 5x5 array, which has a 40x40μm array size. (Right) A 5x5 array generated a spot, whose diameter is about 40μm, at V_G=70V and V_F=20v on the phosphor screen.

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Three-Dimensional Oxidation of Shaped Silicon Surfaces

C.-Y. Hong, A.I. Akinwande
Sponsorship: CreaTV Micro Tech, NIH, DARPA

As silicon device dimension decreases, a three-dimensional silicon oxidation mechanism becomes more important. The device can no longer be assumed to have one or two dimensions, but all three dimensions have to be taken into account. The objective of this work is to study the three-dimensional silicon thermal oxidation behavior by examining the oxidation sharpening process for forming silicon field emission tips. Field emission arrays (FEAs) have been studied as potential electron sources for a number of vacuum microelectronic device applications. A field emitter is usually a high aspect ratio microstructure (tip height >> tip diameter). It results in a high electrostatic field at the apex when a voltage is applied to a proximate annular electrode.

Three-dimensional thermal oxidation behavior on silicon is examined by studying the oxidation process for forming silicon field emitters. Oxide growth rate on the convex surface of a silicon feature is retarded due to stress. The sidewalls of the silicon features have a slightly higher oxidation rate because the sidewalls have more atomic steps due to their curvature increasing the reaction surface area. The oxidation rate of the top of the silicon post depends on the stress relief from the convex edges and the influx of excess oxidants from the convex edge. Figures 1 and 2 show the transmission electron microscope (TEM) images of the silicon features with different original oxide cap size.

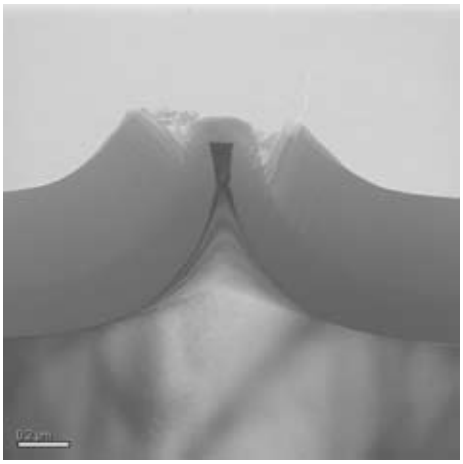

Figure 1: Transmission electron microscope (TEM) image of the silicon feature (original oxide cap size is 1.1 μm) oxidized at 950 ^{o}C for 15 hours.

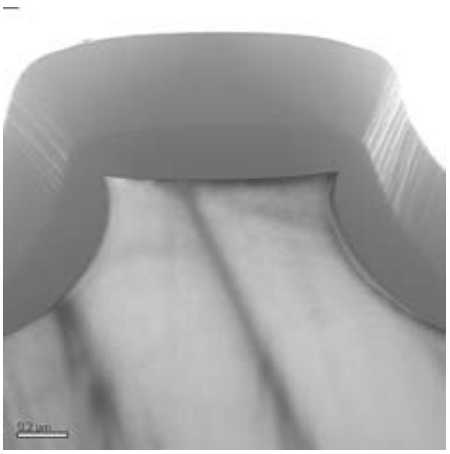

Figure 2: TEM image of the silicon feature (original oxide cap size is 1.8 μm) oxidized at 950 ^{o}C for 15 hours.

Oxidation Sharpening Mechanism for Silicon Tip Formation

C.-Y. Hong, A.I. Akinwande
Sponsorship: CreaTV Micro Tech, NIH, DARPA

Sharp silicon tips have a number of device applications such as (a) silicon field emission arrays, (b) atom probes, (c) atomic force microcopy probes, and (d) field ionization probes for biological and electric propulsion. The radii of the silicon tips for most of these applications are required to be as small as several nanometers. Sharp silicon tips are usually fabricated by isotropic silicon etch followed by oxidation sharpening. Oxidation sharpening is feasible for the silicon tip formation process mainly due to the much slower oxide growth rate on the curved silicon surface. The objective of this work is to study the thermal oxidation mechanism in the oxidation sharpening step for forming sharp silicon tips.

A new silicon tip formation mechanism is proposed. A neck fracture stage precedes the formation of the sharp silicon tip rather than the continuous oxidation of hyperbolic shaped silicon neck as was previously believed to be the case. Stress from the volume difference between silicon and silicon dioxide is the main reason for the silicon neck fracture. Micro-cracks form around the neck at high temperature due to stress from Si/SiO_2 volume difference. It is followed by oxide growth into the cracks after crack formation (Figure 1) and a sharp silicon tip is then formed by further oxidation (Figure 2). After the sharp silicon tip is formed, extensive over-oxidation will shorten and blunt the tips, but a short over-oxidation will only shorten the tip without altering the small tip radius.

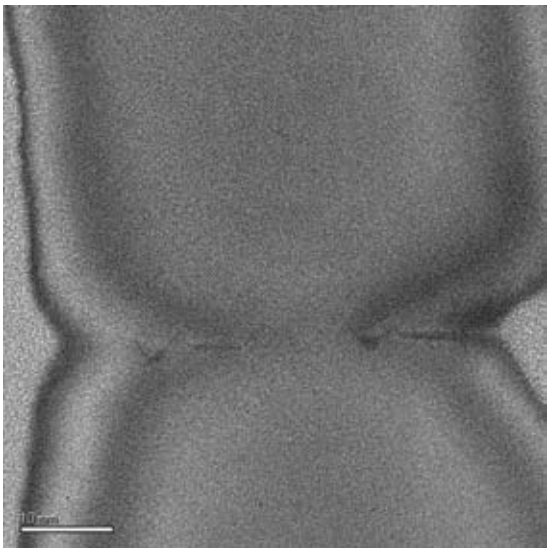

Figure 1: High-resolution transmission electron microscope (TEM) image of the neck region in the silicon feature.

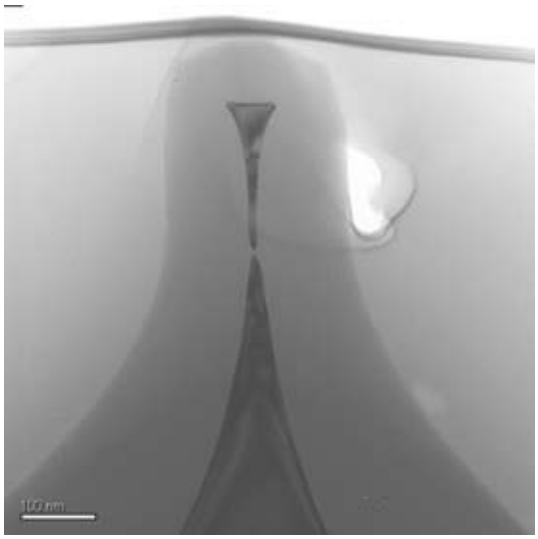

Figure 2: TEM image of the silicon neck region. Silicon was consumed to form a very sharp tip.

Magnetic and Magnetooptical Films Made by Pulsed Laser Deposition

V. Sivakumar, A. Rajamani, C.A. Ross
Sponsorship: Pirelli, Ferry Fund, MicroPhotonics Center Consortium, ISN

We have established a thin film laboratory that includes a pulsed laser deposition (PLD) system, and a ultrahigh vacuum sputter/analysis system. In PLD, a high energy excimer laser is used to ablate a target, releasing a plume of material that deposits on a substrate to form a thin film. PLD is particularly useful for making complex materials such as oxides because it preserves the stoichiometry of the target material.

We have been using PLD to deposit a variety of oxide films for magnetooptical devices such as isolators. These materials include iron oxide, which can adopt one of four different ferrimagnetic or antiferromagnetic structures depending on deposition conditions, and bismuth iron garnet (BIG, $Bi_3Fe_5O_{12}$), which is useful for magnetooptical isolators in photonic devices. The ideal material for an isolator combines high Faraday rotation with high optical transparency. Garnets have excellent properties, but do not grow well on silicon substrates, making it difficult to integrate these materials. In contrast, iron oxide (maghemite) grows very well on MgO or Si, with high Faraday rotation, but its optical absorption is high. Recently we have examined magnetic perovskites such as Fe-doped barium titanate (Figure 1). These materials show weak magnetic properties, but absorption is low, and the films grow with good quality onto MgO substrates. The magnetization versus temperature behavior for these materials is shown in Figure 2. In another set of experiments, we have started to examine how the magnetization of oxide films can be influenced electrochemically, making a chemically-switchable material. Thin films of iron oxide (maghemite and magnetite) are grown on conducting substrates like copper and are subjected to lithium insertion by electrochemical discharge in a coin cell. It is observed that the magnetization of the film decreases upon electrochemical discharge accompanying the insertion of lithium into the interstices in the inverse spinel structure.

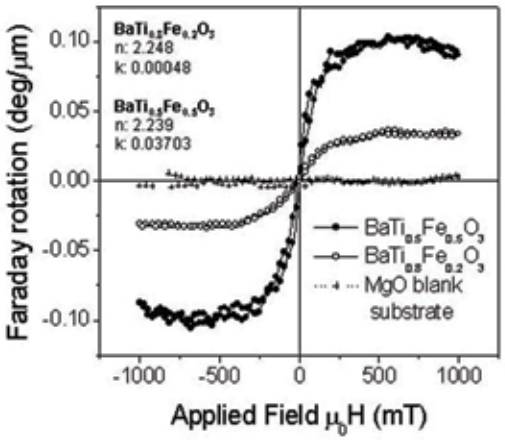

Figure 1: Faraday rotation vs. applied field for 750 nm-thick $BaTi_{0.5}Fe_{0.5}O_3$ and $BaTi_{0.8}Fe_{0.2}O_3$ films on MgO substrates, with the field perpendicular to the film. Inset: optical properties of the two films at 1.55 μm wavelength.

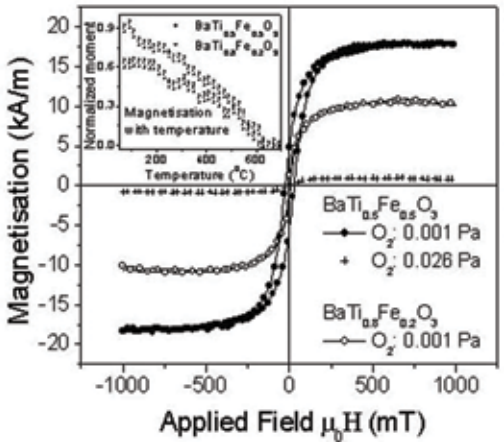

Figure 2: VSM results measured in plane for 750 nm-thick $BaTi_{0.5}Fe_{0.5}O3$ and $BaTi_{0.8}Fe_{0.2}O_3$ films on MgO substrates. Inset: their magnetization vs. temperature behavior.

Modeling of Pattern Dependencies in the Fabrication of Multilevel Copper Metallization

H. Cai, D. Boning

Sponsorship: NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing, MagnaChip

This research is to understand, model, and optimize the interaction between copper electroplating and chemical mechanical polishing (CMP) processes. Currently, this research focuses on the coupling that exists due to pattern-dependent topography, which propagates from the electroplated surface into CMP dishing and erosion. A semi-physics plating model is proposed to deal with random layout in real ICs with better predictive accuracy. Compared to the previous electroplating model developed in our group, the new model has much improved root-mean-square (RMS) error (less than 300 Å). It predicts the topography more realistically and with higher resolution. In particular, the submicron structures clearly show corner and edge effects in the specially designed high-resolution profiler scans. Furthermore, the successful electroplating model is extended to the second-level metallization case by considering the underlying uneven topography form of the first-level metallization. Figures 1 and 2 show the prediction results for the second-level electroplating with grid size 10×10 μm. An improved and coherent chip-scale model framework for copper bulk polishing, copper over-polishing, and barrier layer polishing is developed. The integration of contact wear and density-step-height models is more seamlessly implemented and addresses inherent shortcomings of the previous model. In the new model, a local density instead of the effective density computed by using a planarization length is used, and only a contact wear coefficient is used to characterize the long-range planarization capability. Results obtained with the new model show a significant improvement in the modeling accuracy to less than 100 Å of root-mean square error. Furthermore, the new model framework can be adapted for the modeling of multi-level metallization processes when combined with the electroplating pattern dependence model.

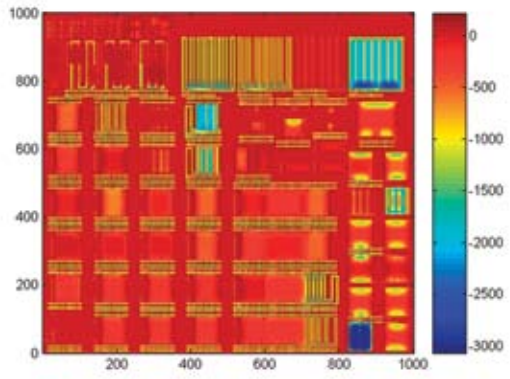

Figure 1: Pre-electroplating envelope map for the second-level metallization (unit: Å).

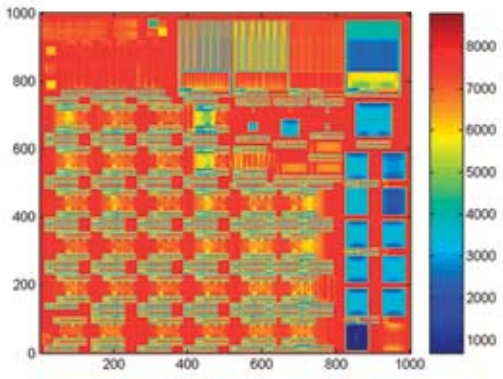

Figure 2: Post-electroplating envelope map for the second-level metallization (unit: Å).

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PFC Alternatives

A. Somani, R. Reif

Sponsorship: NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing, Applied Materials

The goal of this project is to identify possible alternatives for perfluorocompound chemistries for wafer patterning that do not pose long-term environmental problems and that can also sustain ever increasing demands from the process viewpoint. The etch viability of a variety of alternatives has been determined, and so far the most promising candidates according to experiments conducted, chemistry A, was compared with the new chemistry B. This series of experiments can be considered as a preliminary evaluation for the new gas. These novel chemistries were tested on conventional silicon dioxide films. The effluents of these processes will be identified with Fourier Transform Infrared Spectroscopy (FTIR), optical emission spectroscopy (OES), and Residual Gas Analyzer (RGA) at both the chamber and exhaust levels.

This work was carried out at Applied Materials, Santa Clara. An Applied Materials 8" etch system, Enabler, has been used for all experiments. In Figure 1, the experimental set up for this work is depicted. Low pressure RGA was employed at the chamber level for *in-situ* measurements of neutral species. The low pressure RGA was an Inficon Transpector II with a 300 mass range operating at about 1e-6 torr. An Inficon Transpector CIS 2 gas system has the capability to measure a minimum detectable composition change of 200 ppb. The ionizer energy for all measurements were fixed to 70 eV electron beam, and the electron multiplier gain value was 1300. The Fourier Transform Infrared Spectrometer was a Nicolet model 470 with a 6.5 meter CIC Photonics gas cell. It was connected to look for stable species in exhaust. There is also an MKS high pressure RGA connected to the exhaust. Figure 2 summarizes the preliminary FTIR results for blanket oxide etching with all high potential global warming gases that were observed in the exhaust.

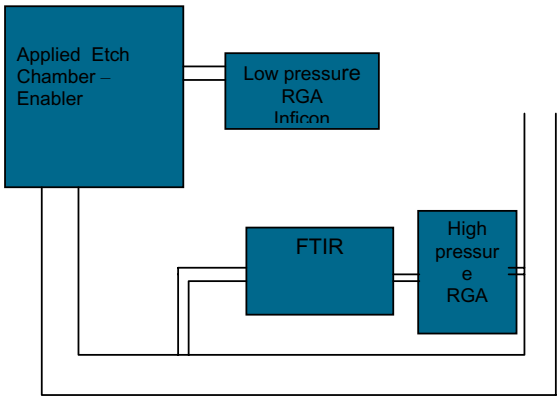

Figure 1: Experimental Set up

Etch recipe	Data presented in standard cubic centimeter						
Gases ratio	C2F6	CO	CHF3	HF	COF2	A	B
Chemistry A/O2 (65/60)	30.57	125.67	0.72	0.75	20.75	1.45	0.00
Chemistry A/O2 (75/60)	46.84	135.33	1.17	1.14	20.65	1.74	0.00
Chemistry B/O2 (65/60)	3.20	169.17	3.92	44.70	38.20	0.00	7.40
Chemistry B/O2 (75/60)	5.92	174.00	3.75	45.02	41.30	0.00	7.96

Figure 2: Amount of gases in exhaust for each blanket oxide etch experiment

Characterization and Modeling of Plasma Etch Nonuniformities

K.O. Abrokwah, D. Boning
Sponsorship: Texas Instruments, Praesagus, Inc., SRC Masters Scholarship

We present work characterizing spatial variations in Integrated Circuits (IC) etching. Our work modeling non-uniformities in IC metallization encompasses plasma etching of trenches in an oxide film stack. We study non-uniformity induced by features that are being etched. These non-uniformities manifest themselves in the form of microloading and aspect ratio dependent etching.

Microloading causes spatial non-uniformity at the chip or die scale and results from design-dependent diffusion of reactant species across the wafer surface. This design-dependent diffusion describes the effect of loading on the overall concentration of reactant species. The loading is greatest in the area of high pattern density because that is where there are the most exposed surface and thus the highest loading of reagents. We characterize etch variations by etching a wafer with dies containing structures of different pattern density (i.e. structures with differing amounts of unmasked oxide). A pattern density model is fitted to the etch depth data, and the model can then predict etch variation for arbitrary amounts of exposed oxide. The model accounts for the decrease in reactant concentration in areas of high loading caused by high pattern density (Figure 1).

Aspect ratio dependent etching occurs at the length scale of individual features and structures. At this length scale, the transport of etchant species from the top of the wafer surface down to the bottom of the trench or hole being etched determines the overall etch rate of the feature. Knudsen transport, a model of how reactants traverse the etched feature, assumes a probability of transmission of reagents that depends on the aspect ratio of the feature. Neutral and ion shadowing model the line of sight transport of reactant species from the plasma down to the bottom of a feature. The Knudsen transport kinetics has been used by Coburn and Winters in their model. We have augmented the Coburn and Winters model to include a sidewall sticking coefficient and compared our experimental depth data to simulated data from the augmented model (Figure 2).

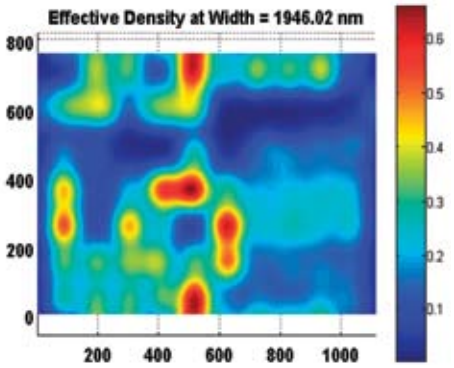

Figure 1: The figure shows the effective pattern density for the test chip containing structures with varying density (loading). The effective pattern density models the effect of neighboring densities.

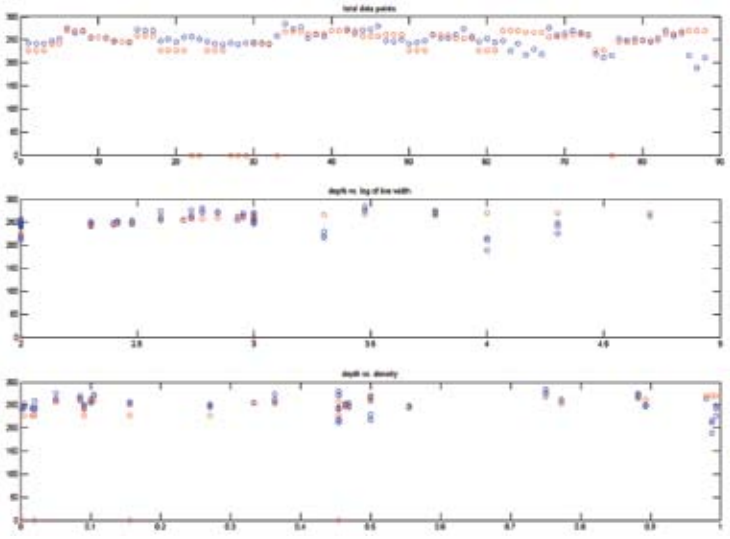

Figure 2: The figure compares the empirical (blue) depth and the simulated depth versus individual features (top), versus linewidth, and versus density.

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[1] Hill, T.F., H. Sun, H.K. Taylor, M.A. Schmidt, D.S. Boning, "Pattern Density Based Predication for Deep Reactive Ion Etch (DRIE)," Solid-State Sensor, Actuator and Microsystems Workshop, Hilton Head, SC, June 2004.

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Three-Dimensional Integration: Analysis and Technology Development

K.N. Chen, C.S. Tan, A. Fan, R. Reif
Sponsorship: DARPA, MARCO IFC

The main objective of this research project is to demonstrate functional three-dimensional (3-D) integrated circuits based on the stacking of silicon active layers. The bulk of the work focuses on process technology development for silicon active layers stacking using low temperature wafer bonding and wafer thinning. Two types of low temperature wafer bonding are investigated; one is the thermo-compression Cu wafer bonding and the other is direct oxide wafer bonding. Cu wafer bonding is used as a permanent bond between active device layers, while oxide wafer bonding is used as a temporary bond between donor wafers and handle wafers. Two types of stacking orientation are explored; either face-to-face or back-to-face. Bi-layer and four-layer stacks are demonstrated on blanket wafers.

A novel test structure for contact resistance measurement of bonded Cu interconnects in three-dimensional integration technology is proposed and fabricated. This test structure requires a simple fabrication process and eliminates the possibility of measurement errors due to misalignment during bonding. Specific contact resistances of bonding interfaces with different interconnect sizes of approximately 10^{-8} Ω-cm^2 are measured. A reduction in specific contact resistance is obtained by a longer anneal time. The specific contact resistance of bonded interconnects with a longer anneal time does not change with interconnect sizes [1].

The morphology and bond strength of copper-bonded wafer pairs prepared under different bonding/annealing temperatures and durations are presented. The interfacial morphology was examined while the bond strength was examined from a dicing test. Physical mechanisms explaining the different roles of post-bonding anneals at temperatures above and below 300°C are discussed. A map summarizing these results provides a useful reference for process conditions suitable for actual microelectronics fabrication and three-dimensional integrated circuits based on Cu wafer bonding [2].

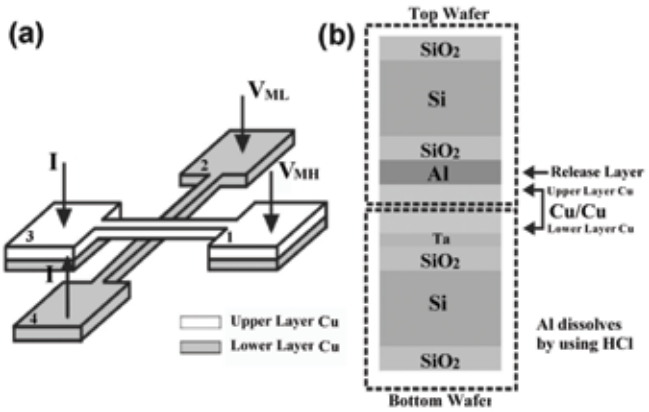

Figure 1: Schematic diagram of the contact resistance test structure [1].

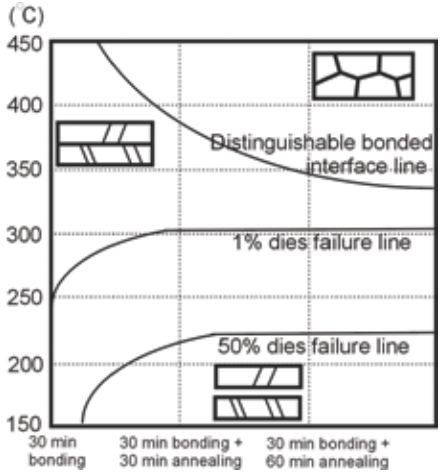

Figure 2: Morphology and strength map for copper wafer bonding under different bonding temperatures and conditions [2].

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[1] Chen, K.N., A. Fan, C.S. Tan, R. Reif, "Contact Resistance Measurement of Bonded Copper Interconnects for Three-Dimensional Integration Technology," *IEEE Electron Devices Letters,* vol. 25, pp. 10-12, 2004.

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Interfacial Electromigration in Cu-Based IC Metallization

Z.S. Choi, F. Wei, C.C. Wai, C.L. Gan, K.L. Pey, W.K. Choi, C.V. Thompson
Sponsorship: SRC, SMA

Electromigration, the diffusion of atoms caused by a momentum transfer from conducting electrons, is one of the main causes of failures in interconnects [1]. It has been shown that the dominant diffusion path in copper interconnect technology is along the interface between dielectric capping layers and copper [2]. It is critical to minimize the diffusion at this interface in order to increase the reliability of copper interconnects. We are carrying out two sets of experiments to investigate interface and surface electromigration in copper interconnects.

In the first set of experiments, the fabrication of test structures is terminated after chemical mechanical polishing of the second metallization layer, which means that the Si_3N_4 capping layer is not deposited on top of second metallization, therefore the top copper surface of the second metallization is exposed (Figure 1). Samples are heated in reducing gas to remove copper oxide, and then tested at pressures of less than 10^{-6} torr, both in specially designed test systems in which the ambient can be used to modify the structure and chemistry of the Cu surface, and for *in-situ* testing in an SEM (Figure 2).

Through these experiments, we are obtaining fundamental constants such as surface diffusivity, drift velocity, and activation energy for diffusion.

In a second set of experiments, the copper surface is treated using various techniques before deposition of an Si_3N_4 dielectric capping layer. Various surface treatments will provide information on the effects of both the surface treatments and the mechanical constraints due to capping layers. Treatments that improve the lifetime of the interconnect test structure will be investigated to understand the mechanism that leads to the improvement.

Data from these basic studies are used in models and simulations. Models and simulations are utilized to predict the reliability of more complex interconnect structures. Simulations are compared with tests on complex structures manufactured at Sematech in the US and the Institute for Microelectronics in Singapore.

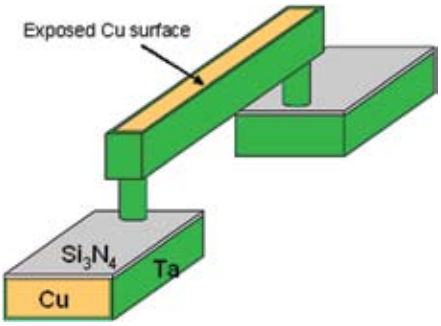

Figure 1: A test structure for which fabrication was terminated before deposition of a dielectric capping layer on top of the test segment in the second level of metallization (lead lines are in the first level).

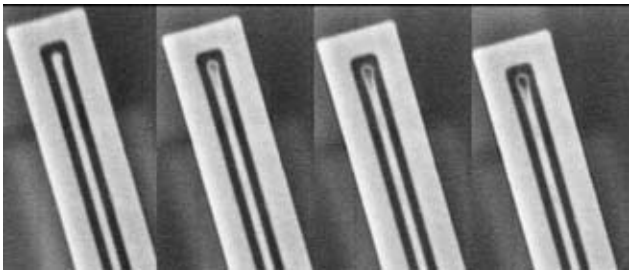

Figure 2: *In-situ* SEM images of the cathode of a test structure, showing surface electromigration damage. The test line is surrounded by a Cu extrusion monitor.

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[1] Blech, I.A., C. Herring, *Appl. Phys. Lett.* 29, p131 (1976).
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Effects of Mechanical Properties on the Reliability of Cu/Low-K Metallization Systems

F.L. Wei, Z-S. Choi, C.C. Wai, C.L. Gan, K.L. Pey, W.K. Choi, C.V. Thompson
Sponsorship: SRC

Electromigration-induced failure remains a critical concern for evolving Cu/low-k metallization technologies. Low elastic moduli, characteristic of low-k dielectrics, and decreasing liner/diffusion barrier thicknesses, with decreased elastic stiffness, lead to significant reliability degradation [1,2]. Thus, achieving future reliability requirements, as current densities increase and interconnect dimensions decrease, will become increasingly challenging. We have undertaken a comprehensive study involving both the experimental characterization of metallization materials and reliability testing of fully processed test structures, as well as simulation and analyses of mechanical responses and electromigration-induced stress evolution.

Electromigration is current-induced atomic diffusion that leads to an evolution in the stress state within interconnect segments. As Cu atoms are forced toward a via, where the liner at the base blocks atomic diffusion, a compressive stress develops and can eventually lead to the mechanical failure of the surrounding material system, and to extrusions of Cu.

The compressive stress that results from electromigration depends on the effective elastic modulus, B, of the interconnect system: the liner, interlevel dielectric (ILD), and cap/etch-stop layers (Figure 1). In order to accurately characterize the mechanical properties of low-k ILD materials, some of which are extremely sensitive to environmental effects, we have employed a suite of experimental techniques, including nanoindentation, cantilever deflection, pressured membrane deflection for characterization of materials deformation, and 4-point bending and double-cantilever pull structures for adhesion measurements. Experimentally measured mechanical properties of individual materials can be used to calculate B, using finite element modeling (FEM) analyses for complex geometries and stress states.

Comparisons between model expectations and lifetime testing are being carried out using test structures manufactured by Sematech.

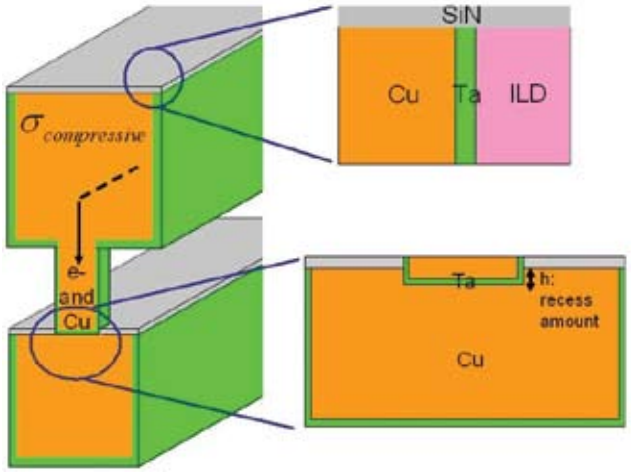

Figure 1: Schematic view of the Cu/low-k interconnect system under compressive stress due to electromigration of Cu atoms.

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Cu Bonding Technology for Three-Dimensional Integrated Circuits

R. Tadepalli, H.L. Leong, C.L. Gan, K.L. Pey, D.E. Troxel, C.V. Thompson
Sponsorship: DARPA (3D Integrated Circuits), SMA, IME

The characterization of Cu wafer bonding is critical to the successful implementation of a three-dimensional (3D) integrated circuit (IC) technology (Figure 1). Previously, we have studied the toughness of bonded Cu interconnects using a mixed-mode fracture test [1]. We have shown that high toughness Cu bonds can be created at a bonding temperature of 300°C using the EV501 bonding tool in MTL [1].

Our present work investigates Cu bond toughness under Mode I (tensile) loading. A novel test methodology has been developed to analyze the toughness of wafer/die-level thermocompression Cu bonds. The effect of lift-off patterned Cu pad size/density on the bond toughness will be studied. Additionally, Mode I bond toughness values are useful metrics for the characterization of Cu-sealed microchannels for heatsinking (Figure 1). A theoretical study of the microchannel *heat removal-bond strength* trade-off has been performed to obtain optimum channel dimensions.

The fundamental limit of the toughness of a Cu bond will be probed using an UHV-AFM/deposition system. Pristine Cu films will be deposited on a substrate and a cantilever tip, and the tip-substrate adhesion will be measured, under UHV conditions, thereby maintaining oxide-free Cu surfaces. Such measurements cannot be performed on a wafer-scale due to the lack of a commercial UHV-bonding tool.

We are also investigating the quality of bonded ECP damascene-patterned Cu interconnects (NTU, Singapore). The bond toughness is evaluated using a four-point bend test. The effects of Cu film texture, Cu pattern density, and the CMP (chemical mechanical polishing) process on the bond quality are being studied. Under thermo-compression, the wafers overcome the effects of polishing non-uniformity and the dishing effect, to bond with varying degrees of success. Moreover, we have designed novel test structures to assess the reliability of bonded Cu interconnect structures.

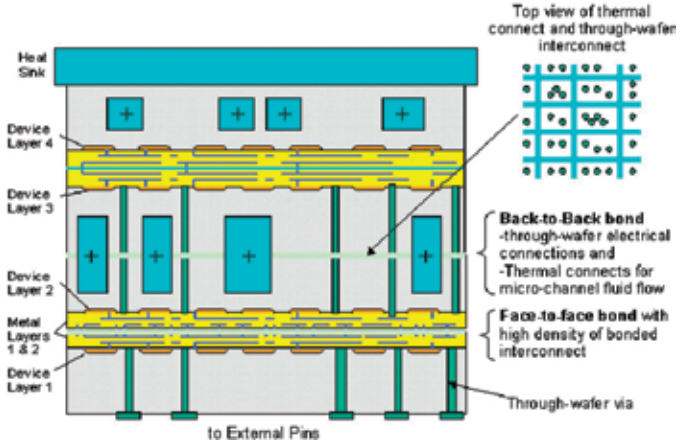

Figure 1: 3D IC technology with thermal management. Wafers are stacked using alternate face-to-face and back-to-back bonds.

REFERENCES:

[1] Tadepalli, R., C.V. Thompson, "Quantitative Characterization and Process Optimization of Low-Temperature Bonded Copper Interconnects for 3-D Integrated Circuits," in *Proc. IITC*, 2003, pp 36-38.

Numerical Techniques in Biomolecule Design and Systems Biology

D. Vasilyev, J. Bardhan, M. Altman, S. Kuo, P. Ramirez, P. Barton, B. Tidor, J. White
Sponsorship: NIH, SMA, NSF

To design an effective drug or a biochemically-based sensor, it is necessary to develop ligand molecules that bind readily and selectively to receptors of interest. Electrostatic forces play an important role in the design of ligands, but the complicated three-dimensional geometry of the problem makes it difficult to assess the electrostatic fields and then optimize the ligand. We have been developing fast methods for electrostatic analysis, and have been focussed on three aspects.

First, we have developed a fast analysis program based on using discretized integral equation formulations plus sparsification-accelerated iterative techniques. Second, we have coupled electrostatic analysis with the ligand charge optimization problem using a Hession-implicit approach [1]. Finally, we have been developing improved discretizations of the molecular surface geometry using curved panels, and have developed approaches for computing integrals over curved panels [2].

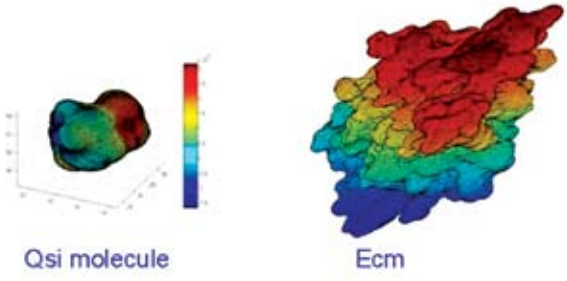

Figure 1: Electrostatic design problem

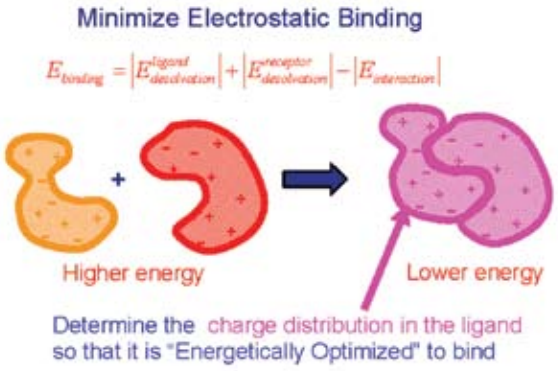

Figure 2: Molecular Surfaces for two proteins

REFERENCES:

[1] Bardhan, J.P., J.H. Lee, M.D. Altman, S. Leyffer, S. Benson, B. Tidor, J.K. White, "Biomolecule Electrostatic Optimization with an Implicit Hessian," *Proc. of Modeling and Simulation of Microsystems,* March, 2004

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Field Emission from Organic Materials

I. Kymissis, A.I. Akinwande
Sponsorship: NSF

Field emission devices have shown tremendous potential in a wide variety of applications. Displays, high intensity lighting, RF amplifiers, chemical analysis systems, and space propulsion schemes have all been proposed using field emitters. Field emission displays (FEDs) are perhaps one of the most interesting potential applications because of the high energy efficiency of cathodoluminescence, demonstrated long lifetime of available phosphors, wide color gamut, and angle-independent viewing characteristics.

Despite this promise, FEDs have failed to penetrate the consumer market and many companies have abandoned FED development. The manufacturing processes pursued so far have capital and production costs that are too high for commercialization. In this work, we have developed a new field emission architecture that allows the use of low cost materials while simultaneously offering the possibility of a uniform, low-noise display controlled with low voltages. These goals are achieved by integrating an organic field effect transistor (OFET) with an organic field emitter (OFED). In our demonstration device, both the OFED and OFET are created at room temperature using a non-lithographic process. By moving the barrier that controls emission from the field emitter surface to the transistor source-channel junction and eliminating the need for a micromachined gate, high performance and uniformity can be achieved in a potentially low cost process. We have demonstrated a reduction in current noise, immunity to residual gas exposure, and low voltage control of the electron flux control using this FED architecture.

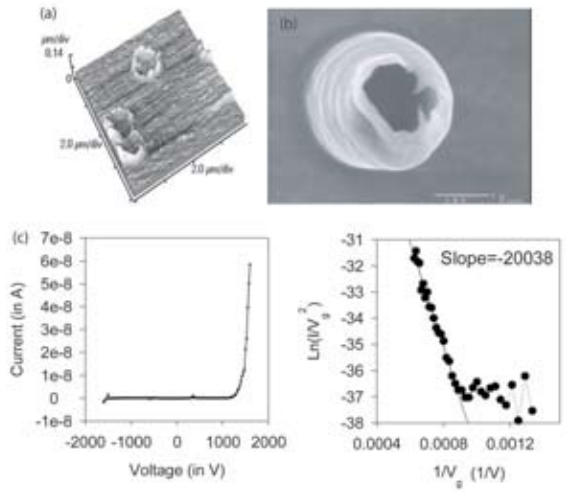

Figure 1: Figure (a) shows an atomic force micrograph of the organic field emitter, (b) shows a scanning electron micrograph, and (c) shows typical emission characteristics for the devices.

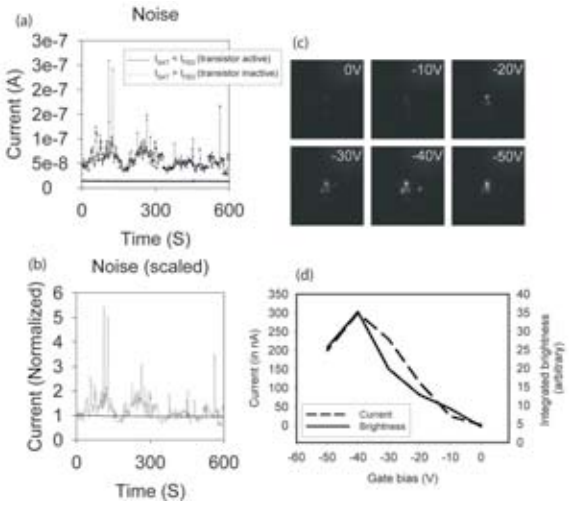

Figure 2: Figures (a) and (b) show the reduction in current noise achieved by the control technique developed; –(c) and (d) demonstrate that over 100:1 brightness switching can be achieved with 30V applied to the transistor (controlling a 1100V electrons).

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[3] Kymissis, I., A.I. Akinwande, "Organic Field Emission Device Integrated with Organic Transistor," Accepted, *IEEE Transactions on Electron Devices.*

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Integrated Organic Electronics

I. Kymissis, K. Ryu, A.I. Akinwande, C.G. Sodini, V. Bulovic
Sponsorship: MARCO MSD, NSF

Organic electronics hold promise for a wide range of applications. Using organic materials it is possible to fabricate transistors, organic light-emitting devices (OLEDs), and photodetector elements; all at low process temperatures (<90º C). While many of these individual devices have been extensively studied and optimized, technologies that are able to produce a large number of devices as well as different types of devices together in integrated circuits are not well developed.

The goal of this project is to make a fully lithographic modular platform for organic electronics that is capable of supporting organic field effect transistors (OFETs) or other related amorphous thin film transistors together with organic photodetectors and OLEDs. Because these systems can be fabricated at low temperatures, they are compatible with a wide range of substrates, including flexible polymeric foils.

To date, the project has achieved several milestones, including: the development of a fully lithographic OFET backplane process, a self-aligned OFET process (Figure 1), and the demonstration of an active matrix organic integrated photodetector array (Figure 2). Work continues on the refinement of these modular elements and their integration with organic light-emitting devices (OLEDs) to create a full-feedback controlled OLED display system that compensates for degradation in OLED devices as well as nonlinearities in the driving circuitry.

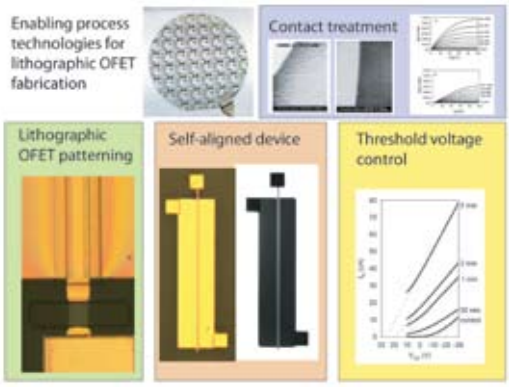

Figure 1: A summary of the technologies that we have developed to enable the lithographic fabrication of OFET backplanes and control their characteristics. The wafer shown is a typical 100mm wafer processed using our lithographic process.

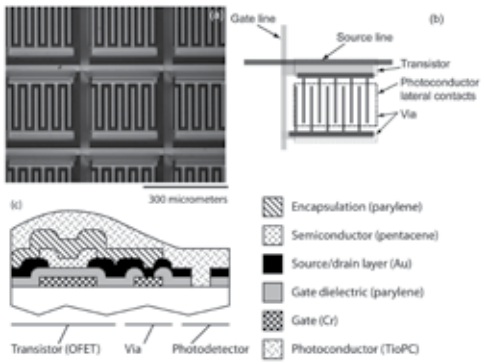

Figure 2: (a) Shows a micrograph of the low temperature active matrix photodetector presented in [1] (b) details the structure of the photodetector, and (c) schematically shows the device cross section. The transistor backplane is fabricated first; it is isolated using a layer of parylene, and a vias cut into parylene allow the photoconductor access to the interdigitated electrode structure.

REFERENCES:

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Charge Trapping in Layered Nanostructured Films

J. Yu, C. Madigan, S.H. Kang, I. Kymissis, V. Bulovic
Sponsorship: MARCO MSD, MIT, NSF, MRSEC

Structural disorder in amorphous organic thin films can result in localized electronic states that trap and store charges in equilibrium. These trapped charges can dominate the current-voltage (I-V) characteristics of organic devices due to the relatively low charge carrier density in organic solids.

Our recent experiments on organic devices with deliberately-inserted metal or organic traps demonstrated that charge trapping can significantly alter I-V characteristics of an operating device [1]. Predictions of energy band structure indicate that an ITO anode / 50 nm Alq3/ 10 nm trap / 50 nm Alq3 / 50 nm Mg:Ag / 50 nm Ag cathode structure with a trap layer of organic DCM2 or silver metal can be effective at trapping charge. This monopolar device transports only electrons. When a forward bias is applied on the device, electrons begin to fill the trap layer (Figure 1). With increased trap filling, the number of traps decreases, resulting in an increase in the effective charge mobility. Additionally, as the deep metal traps are filled, the effective trap level within the charged metal nanoclusters decreases. With decreasing trap depth, the probability of finding a trapped electron outside the trap boundaries increases, and the trapped carrier density can exceed the intrinsic carrier density in the vicinity of the trap (Figure 2). The trapped charges effectively dope the surrounding organic semiconductor which is manifested as an increased conduction through the device and results in a sharp conductance turn-on in the device I-V characteristics. Applying reverse bias on the device depletes the trap layer of electrons and eventually, switches the device to a low conduction state. The device demonstrates on/off current ratio of fifty for the DCM2 trap and ten million for a silver trap. Metals have higher trap density and deeper trap energy, and therefore, have a larger impact on the on/off current ratio.

We are presently modeling the charge trapping mechanism in these structures in order to generate a generalized description of the process. Space charge limited conduction for a uniform trap density and spatially non-uniform charge traps are both considered in our model.

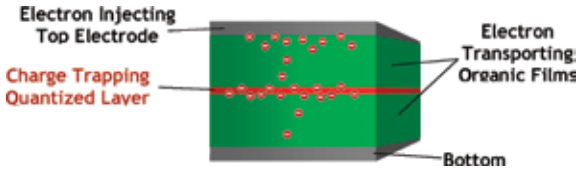

Figure 1: Charge Trapping in a trap layer embedded inside a layered semiconducting structure.

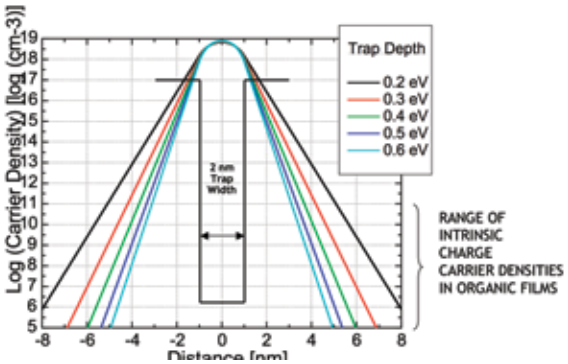

Figure 2: Due to the extent of the wavefunction, spreading charge carrier trapped in a potential well is not confined to the trap. The plot shows the charge carrier density as a function of distance away from the trap for several different trap depths. The magnitude of the trapped carrier density in the vicinity of the trap can greatly exceed the intrinsic charge carrier density in an organic film.

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Threshold Voltage Modification of Organic Thin-Film Transistors

A. Wang, I. Kymissis, V. Bulovic, A.I. Akinwande
Sponsorship: U.S. Army Natick Center, MARCO MSD

Threshold voltage control of organic field effect transistors (OFETs) is critical to the further development of integrated circuits containing OFETs [1,2]. We report results from a process-level method for modifying the threshold voltage, V_T, of pentacene FETs with parylene, an organic polymer, as the gate dielectric. In this approach, treatment of the parylene surface with oxygen plasma or UV-ozone prior to pentacene deposition introduces fixed charged states at the semiconductor-dielectric interface. These states shift the flatband voltage, V_{FB}, and, consequently, shift the V_T.

Typical I-V characteristics for control and O_2 plasma-treated FETs are shown in Figure 1. We can model the effects of trap-introduced charges on I_D in the FET linear region as (a) fixed charges, Q_{fixed}, that shift the threshold voltage and (b) mobile charges, Q_{mobile}, that increase parasitic bulk conductivity. Q_{mobile}, determined from the I-V characteristics, in the O_2 plasma-treated FETs is on the same order of magnitude as ΔQ_{fixed} (2.0×10^{-6} C/cm^2) and is an order of magnitude larger than in the control.

Since the 15-second O_2 plasma treatment resulted in V_{FB} and V_T shifts greater than +100V, UV ozone treatment was performed instead as a more controllable method of adjusting V_T. Quasistatic capacitance-voltage measurements and current-voltage characteristics demonstrate that the flatband and threshold voltages can be shifted gradually with increasing lengths of UV-ozone exposure. Figure 2a and 2b show the monotonic increase in V_{FB} and V_T with ozone exposure time. These results confirm that careful control of interface state densities at the semiconductor-dielectric interface is essential to threshold voltage control in organic FETs.

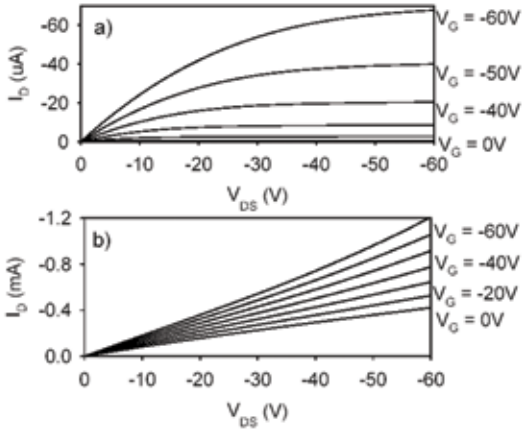

Figure 1: I-V characteristics for (a) control and (b) O_2 plasma-treated FETs. The O_2-treated device shows much higher drain current, which can be attributed to a more positive threshold voltage and increased bulk conductivity.

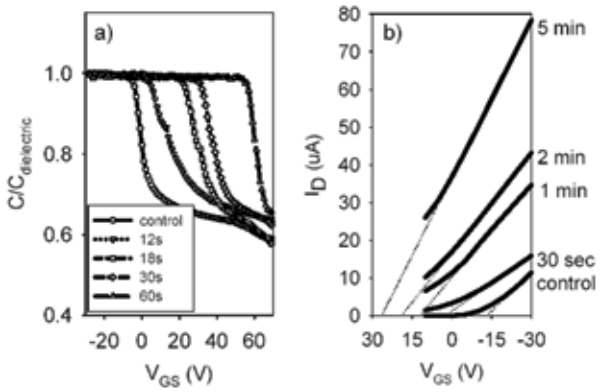

Figure 2: (a) Quasi-static C-V measurement of control and UV-ozone-treated devices. (b) V_{GS} sweep and V_T extrapolation for UV-ozone-treated devices in the FET linear region, V_{DS} = -4V. Both flatband and threshold voltages increase monotonically with ozone exposure time.

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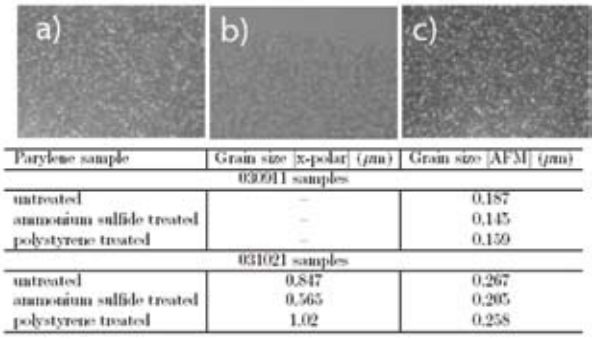
Effect of Surface Treatments on Pentacene Organic Thin-Film Transistor Performance

A. Wang, I. Kymissis, A.I. Akinwande
Sponsorship: U.S. Army Natick Center

Pentacene TFT performance is strongly dependent on the morphology of the pentacene semiconductor. Larger grain sizes and hence, fewer grain boundaries, have been linked to improved mobility and on/off ratios [1,2]. By modifying the condition of the pentacene growth surface, i.e. the surface of the gate dielectric, pentacene crystallinity and TFT performance may be improved. A more hydrophobic surface is expected to result in better packing of pentacene molecules; Yasuda, et al. reported improved mobility and on/off ratios in pentacene TFTs using more hydrophobic dielectrics [3]. In our work, pentacene TFTs were fabricated using parylene, an organic polymer, as gate dielectric. We examined the effects of an ammonium sulfide treatment and a spin-on polystyrene treatment of the parylene prior to pentacene deposition, and compared the performance of TFTs using (a) untreated parylene, (b) ammonium sulfide-treated parylene, and (c) polystyrene-treated parylene.

Contact angle measurements confirmed an increase in surface hydrophobicity after both treatments. Atomic force microscopy (AFM) and optical microscopy using crossed polarizers showed comparable pentacene grain sizes in the untreated and polystyrene-treated samples. Because of increased average surface roughness, pentacene grain size in the ammonium sulfide-treated sample was smallest (Figure 1). Electrical characterization confirms the trend seen in the physical characterization. Field effect mobility, calculated from conventional saturation region FET equations at $V_{GS} = V_{DS} = -100V$, is significantly poorer in the ammonium-treated device and comparable in the polystyrene and untreated devices (Figure 2). After gate voltage was scaled (to account for different dielectric thicknesses) to obtain the same electric field in each device, the polystyrene-treated device shows the highest mobility. These physical and electrical characterization results demonstrate the importance of the quality of the pentacene growth surface.



Parylene sample	Grain size [x-polar] (μm)	Grain size [AFM] (μm)
030911 samples		
untreated	–	0.187
ammonium sulfide treated	–	0.145
polystyrene treated	–	0.159
031021 samples		
untreated	0.847	0.267
ammonium sulfide treated	0.565	0.205
polystyrene treated	1.02	0.258

Figure 1: Optical micrographs using crossed-polarizers of pentacene on (a) untreated, (b) ammonium sulfide-treated, and (c) polystyrene-treated parylene. Each image covers a 36.6μm x 25.6μm area. Measured grain sizes are summarized in the table.

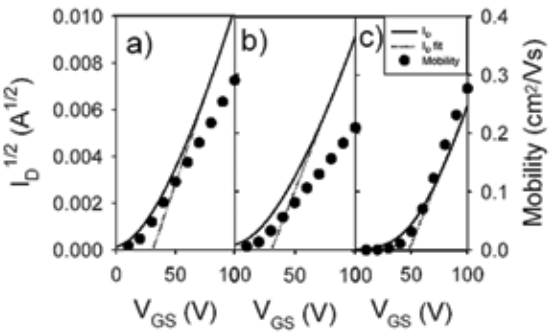


Figure 2: I-V characteristics for (a) control, (b) ammonium sulfide- treated, and (c) polystyrene-treated transistors. The circles plot mobility vs. gate voltage (right axis). The lines show the extraction of threshold voltage from the saturation region, VDS = -100V (left axis).

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Logic Gates on Fiber: Building Blocks for Electronic Textiles

Y.W. Choi, A.I. Akinwande
Sponsorship: DARPA

Electrotextiles denote the class of fabric structures that integrate electronic elements with textiles. One of the outstanding features of electrotextiles is the ability to personalize. Each system can be tailored by choosing the type of fibers that are included in the design. Another outstanding feature is that electronics can be distributed and made invisible in electrotextiles. It makes the technology invisible, embedded in our natural surroundings, present wherever we need it, enabled by simple and effortless interactions, attuned to all our senses, adaptive to users and context, and autonomously acting [1]. Research on the integration of electronic devices on fibers, which are woven into fabric is being conducted by various groups [2,3]. Thin film transistors were fabricated on polyimide sheets and cut into fibers. The transistors on the fibers were interconnected using conductor fibers, by weaving the fibers using spacer fibers, and a woven inverter circuit has been demonstrated [2]. The amorphous Si thin film transistors (TFTs) were fabricated at 150 °C on polymer substrates [3].

Our approach fabricates logic gates instead of the individual transistors on fibers. In this approach, the "fabric primitives" are fibers consisting of rows or columns of logic gates. There are several advantages to our approach. The first advantage is that fiber-to-fiber signal transmission is digital. This increases noise immunity and improves fault tolerance. The second major advantage of this approach is that systems are configured using an FPGA (Field-Programmable Gate Array) paradigm. The fibers are in essence arrays of logic gates that are personalized through programmable contact vias / interconnects. The third major advantage is that each system could be personalized by choosing the type of "fiber" that is included in the design. For example, if there were a desire for a self-powered system, then we could add a solar cell or battery "fiber." If there were a desire for a large area micro-electro-mechanical system (MEMS), we need to add a piezoelectric-actuated "fiber" for example. We fabricated logic gates, such as inverter, NAND and NOR, using low-temperature (<150 °C) a-Si TFTs technology on polyimide sheets, which were cut into fibers and woven into fabric. These logic gates on fiber may be essential building blocks for electrotextiles.

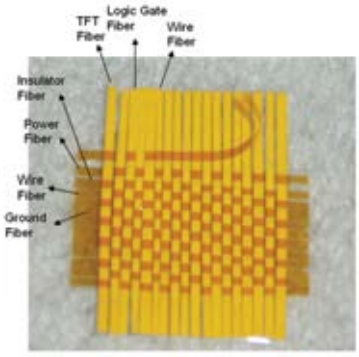

Figure 1: Photograph of the schematic electrotextiles woven polyimide fibers, which can have active devices such as inverters, NAND, and NOR.

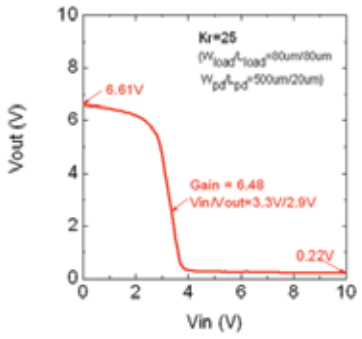

Figure 2: Transfer characteristics of the inverter fabricated with the a-Si TFTs.

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Low-Voltage Organic Thin Film Transistors with High-K $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ Pyrochlore Gate Insulator

Y.W. Choi, I.-D. Kim, H.L. Tuller, A.I. Akinwande
Sponsorship: DARPA

Thin film transistor circuits using organic semiconductors (oTFT) have received intense interest for applications requiring structural flexibility, large area coverage, low temperature processing, and low-cost [1]. Pentacene TFTs have demonstrated the highest performance among TFTs with an organic semiconductor channel. A major limitation, however, has been unusually high operating voltages (20~100 V), a concern for portable, battery-powered device applications [2]. The high-operating voltage stems from poor capacitive coupling between the gate electrode and channel region. A combination of higher permittivity gate dielectric and reduced dielectric thickness leads to lower voltage operation. Recently, M. Hallk et al. reported low-voltage pentacene OTFTs with very thin (2.5 nm) amorphous molecular gate dielectric [3]. Flexible polymer substrates, characterized by rough surfaces, benefit from the use of high K dielectrics given the ability to accommodate thicker films without the need to increase operating voltage, which leads to the suppression of pinholes and minimizes problems associated with step coverage.

We successfully fabricated low voltage (< 3V) organic transistors using a 200 nm thick pyrochlore gate dielectric, $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ (BZN), with the highest reported dielectric constant (3_r =50) prepared at a room temperature. The introduction of an extremely thin parylene film between the BZN dielectric and the pentacene semiconductor markedly shifted the threshold voltage, making it possible to fabricate both enhancement (E) and depletion (D) TFTs. Positive threshold voltage and the threshold voltage change caused by parylene may be due to dangling bonds at the BZN surface and the passivation of the dangling bonds. The inverters with depletion load were operated at less than 4V and had an excellent noise margin. The inverter and its performance were the best among the inverters made with OTFTs, with similar gate dielectric thicknesses reported previously in the literature.

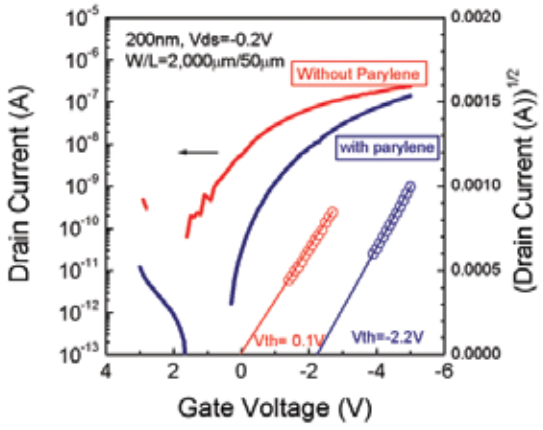

Figure 1: Transfer characteristics of pentacene OTFs with high-k BZN gate dielectric. The OTFTs with parylene and without parylene operated at enhancement and depletion modes, respectively.

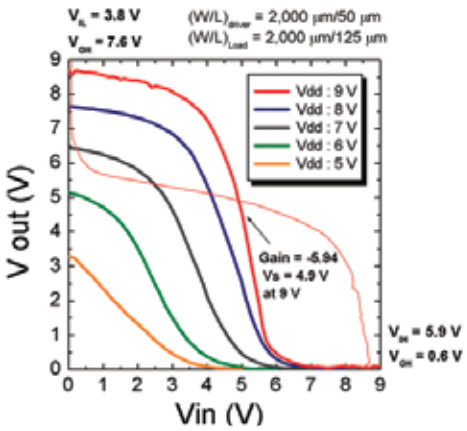

Figure 2: Transfer characteristics of the fabricated inverter with depletion load at various operating voltages.

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Hybrid Nanocomposite Architectures Using CNTs

E.J. Garcia, D.-J. Shim, B.L. Wardle, in collaboration with S.-G. Kim
Sponsorship: La Caixa Foundation

The world has been promised the widespread use of advanced composite materials for decades. Extremely stiff and strong fibers in a matrix binder (*e.g.,* graphite fibers in an epoxy matrix like that used on the Stealth bomber) provide higher performance relative to metals, and their use is widespread in the military/defense sector, with penetration into other sectors. However, advanced composites have relatively poor performance when loaded in directions off the fiber axis. The objective of the current work is to explore hybrid architectures combining both traditional composite materials and carbon nanotubes (CNTs). Several architectures have been identified for property improvement of traditional composites, and a second theme being considered is to create tough junctures between MEMS devices and macro-scale composite structures.

Key to realizing the hybrid architectures are the nanopelleting technologies and processes developed at MIT by Prof. Sang-Gook Kim [1,2]. The unique nanopelleting process allows single- or multi-wall carbon nanotubes (S/MWNTs) to be grown in a pelletized form suitable for arrangement in various architectures to realize various mechanical, electrical, and other property improvements. Volume fraction of CNTs in the pellets is very high relative to those achieved by other groups. A SEM image of a released aligned CNT pellet is given in Figure 1.

Current work focuses on a specific architecture to create ultra-tough composites [3]. The released CNT pellets (see Figure 1) serve as the starting point for the creation of this architecture. Toughening improvements for a typical composite system have been predicted showing a nanoscale effect on toughness (Figure 2). The manufacture and testing of hybrid composites is ongoing.

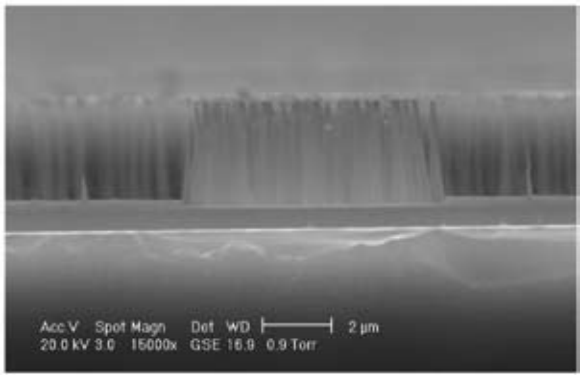

Figure 1: SEM of aligned CNT pellet (courtesy of Prof. Sang-Gook Kim, MIT ME).

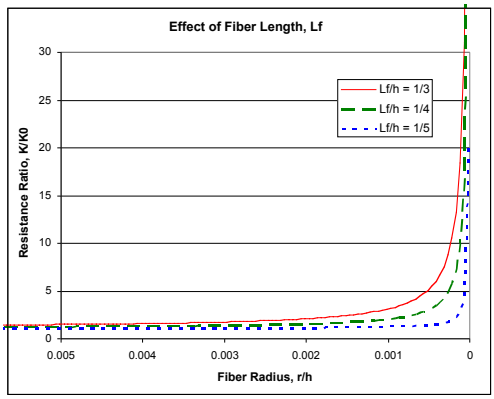

Figure 2: Relative toughness scaling results. E is the composite effective in-plane modulus and K_0 is 1.6 MPa$\sqrt{m}$.

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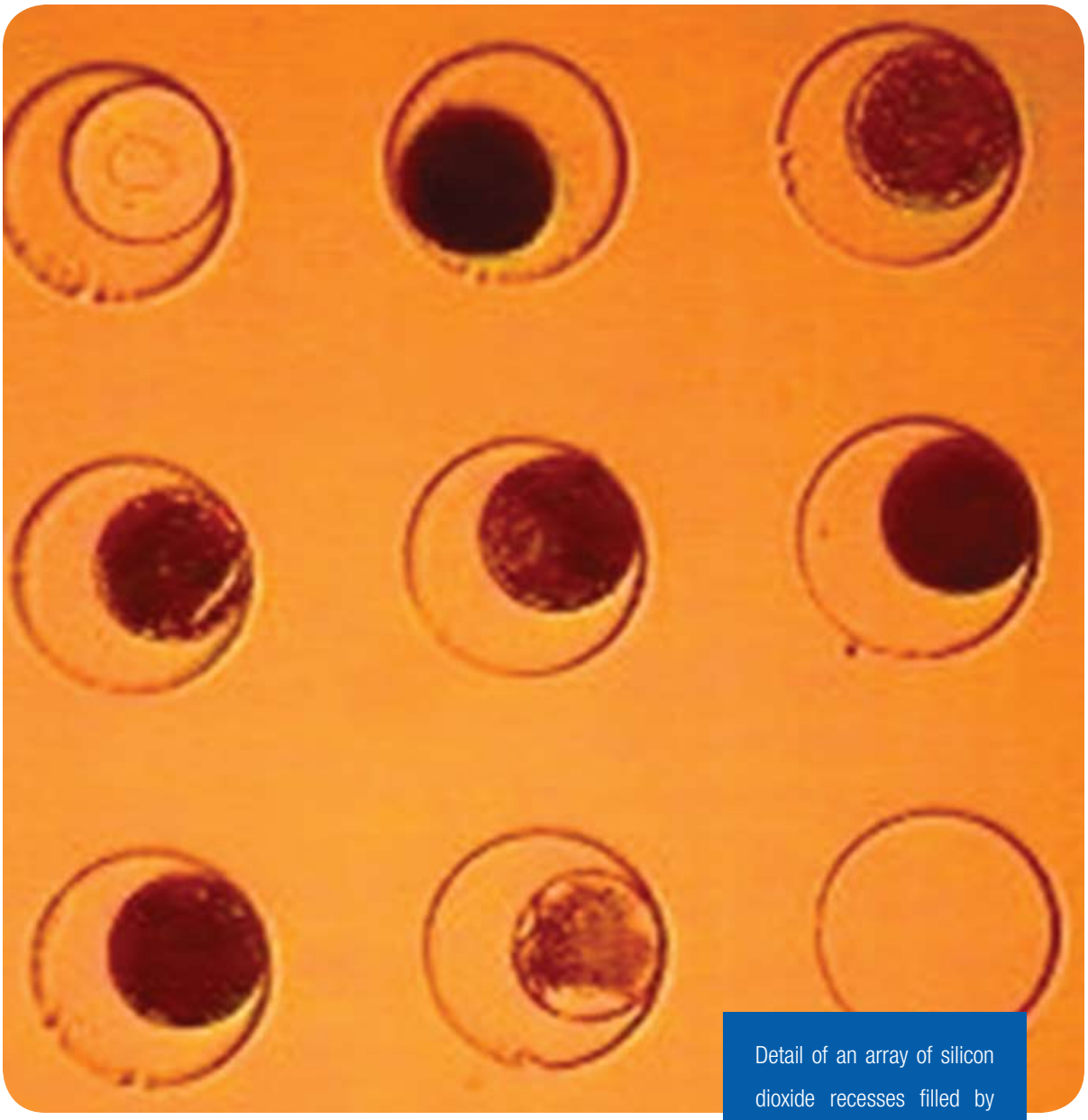

Detail of an array of silicon dioxide recesses filled by GaAs devices. Image by Fonstad group.

PHOTONICS

TABLE OF CONTENTS

Excitons in Organic Optoelectronic Devices

C. Madigan, V. Bulovic
Sponsorship: NSF Career Grant, NDSEG

Most of the published physical studies on disordered molecular organic materials investigate charge conduction mechanisms, specifically the microscopic and macroscopic behavior of polarons. While consensus remains elusive, in part because of the continuing uncertainty over the role of interfaces as compared to the bulk in determining device performance, there has been considerable progress. By comparison, very few studies have been published on exciton dynamics in organic optoelectronic devices (where excitons are the dominant optical excitations in amorphous organic materials). Exciton modeling studies are often qualitative, reduced to parameters such as the exciton diffusion length and exciton lifetime, leaving significant questions unanswered about the detailed microscopic processes and how to develop models capable of yielding quantitative device properties on the macro-scale.

In this project, we aim to develop detailed exciton dynamics models to enable and implement device-level simulations. Three considerations motivate this work. First, as has long been recognized in the inorganic semiconductor industry, designing a device on paper and simulating it using a computer is far more efficient than designing, fabricating and testing a device. Second, good models of both polarons and excitons are necessary to accurately simulate optoelectronic device behavior, but at this stage, comparatively little attention has been given to excitons. Finally, since few studies simultaneously consider polaron and exciton simulations to treat the behavior of these devices, it is significant to determine the specific ways to efficiently and accurately combine existing models of polarons with improved models of excitons in a combined simulation.

To date, we demonstrated that exciton energy levels are altered through interaction with neighboring molecules by the mechanism of solid-state solvation. We continue to investigate other electric-field-induced, excitonic energy-level shifts. We have also demonstrated that ultra-fast, time-resolved, fluorescence spectroscopy can be used to probe exciton diffusion in our materials, as previously demonstrated for polymer films. We have developed a complete Monte Carlo simulation of exciton diffusion in disordered molecular solids by treating spatial and energetic disorder and diffusion by either Dexter or Forster energy transfer. This simulation models homogenous, continuous solids as well as doped and structured materials, as required for treating devices. Existing analytical models for treating the general excitation diffusion in disordered media have been evaluated and found to be generally inapplicable to this project. Current work develops additional experimental methods for monitoring exciton diffusion, namely site-selective fluorescence and fluorescence-polarization anisotropy, and modifyies the exciton Monte Carlo simulation to incorporate polarons.

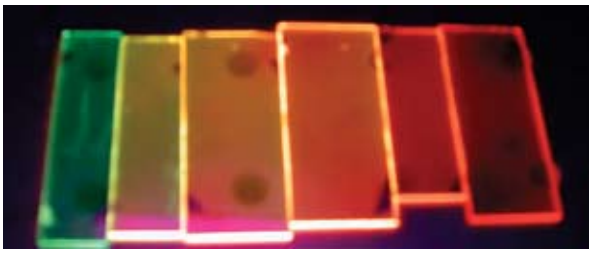

Figure 1: Series of DCM2:AlQ3 fluorescing films showing DCM2 excitonic energy shifts (i.e., different colors) due to intermolecular interactions. The leftmost film shows AlQ3 PL, and the remaining films show DCM2 PL for different DCM2 dopings.

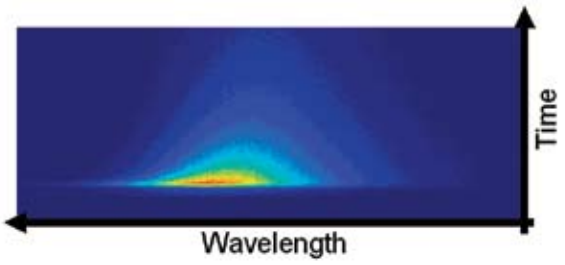

Figure 2: Example of ultra-fast, time-resolved, fluorescence data. The vertical axis denotes wavelength; the horizontal axis, time. In this example, DCM2 is the photo-luminescing material, doped into an AlQ3 host.

Layer-by-Layer, J-aggregate Thin Films with an Absorption Constant of 10^6 cm^{-1} in Optoelectronic Applications

J.R. Tischler, M.S. Bradley, V. Bulovic
Sponsorship: DARPA Optocenter, NDSEG, NSF-MRSEC

Thin films of J-aggregate cyanine dyes deposited by layer-by-layer (LBL) assembly exhibit exciton-polariton dynamics when incorporated in an optical microcavity. Such LBL, J-aggregate thin films can be precisely deposited in a specific location in an optical microcavity, enabling the development of previously unachievable optoelectronic devices, as for example, the recently demonstrated resonant-cavity exciton-polariton organic light-emitting device [1].

To gain insight into the physical properties of these films, we investigate the optical and morphological properties of 5,6-dichloro-2-[3-[5,6-dichloro-1-ethyl-3-(3-sulfopropyl)-2(3H)-benzimidazolidene]-1-propenyl]-1-ethyl-3-(3-sulfopropyl) benzimidazolium hydroxide, inner salt, sodium salt (TDBC) J-aggregates, alternately adsorbed with poly-(diallyldimethylammonium chloride) (PDAC) on glass substrates. Atomic force microscopy (AFM) shows that the first few sequential immersions in cationic and anionic solutions (SICAS) form layered structures, which give way to Stransky-Krastanov-type growth in subsequent SICAS. We combine thickness measurements from AFM and spectroscopic data to determine the optical constants of the films and find that at the peak absorption wavelength of 596 nm, the films possess an absorption coefficient of $\alpha = 1.05 \pm 0.1 \times 10^6$ cm^{-1}, among the highest ever measured for a neat thin film. The optical constants were calculated by fitting spectroscopic data for films in the layered growth regime to a model based on propagation and matching matrices (Figure 1).

The presented method is a general approach to generating thin films with very large absorption constant, an enabling step in the fabrication of novel devices that utilize strong coupling of light and matter, such as light emitting devices (Figure 2) and polariton lasers.

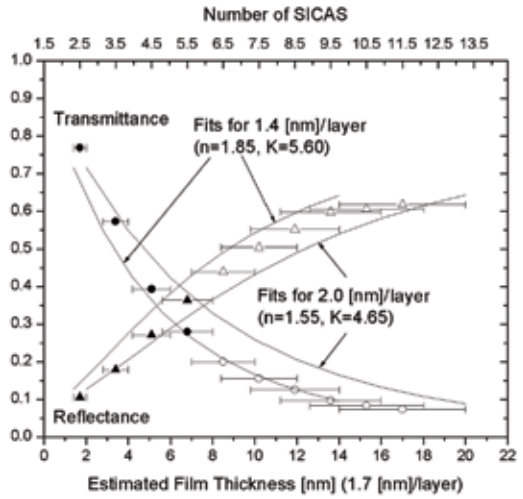

Figure 1: Optical data plotted with a least-squared-error fit for the optical constants at λ=596 nm using a model of propagation and matching matrices. The filled versus outlined points are for samples where layered versus Stransky-Krastanov growth dominate, respectively. The filled points were used for the least-squared-error fit.

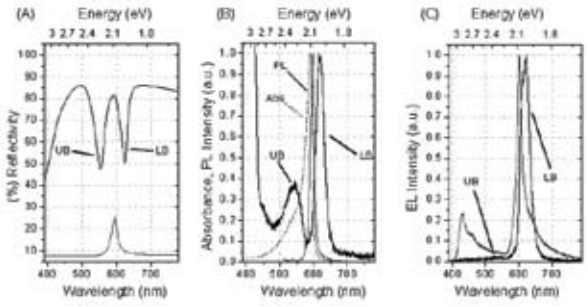

Figure 2: Reflectivity, photoluminescence, and electroluminescence of a single polariton, resonant-cavity, organic light-emitting device with microcavity closely tuned to the J-aggregate resonance.

REFERENCES:

[1] Tischler, J.R., M.S. Bradley, V. Bulovic, J.H. Song, A. Nurmikko, "Strong Coupling in a Microcavity LED", *Phys. Rev. Lett.* (2005).

Patterned Quantum Dot Monolayers in QD-LEDs

S. Coe-Sullivan, L. Kim, J. Steckel, R. Tabone, M.G. Bawendi, V. Bulovic
Sponsorship: Presidential Early Career Award for Scientists and Engineers, ISN, NSF-MRSEC, Deshpande Center

Hybrid organic/inorganic quantum dot light-emitting devices (QD-LEDs) contain luminescent nanocrystal quantum dots (QDs) imbedded in an organic thin film structure. The QDs are nanometer-size particles of inorganic semiconductors that exhibit efficient luminescence; their emission colors can be tuned by changing the size of the nanocrystals. For example, the luminescence of QDs of CdSe is tuned from blue to red by changing the QD diameter from 2nm to 12nm. By further changing the material system, saturated color emission can be tuned from the UV, through the visible, and into the IR. The inorganic emissive component provides potential for a long operating lifetime of QD-LEDs. The room temperature fabrication method ensures compatibility of the QD-LED technology with the established all-organic LEDs (OLEDs).

The optimized QD-LED device structure contains a single monolayer of QDs embedded within the layered, organic thin-film structure. The technology is enabled by the self-assembly of the QDs as a densely packed monolayer on top of a conjugated organic film. The QD film is positioned with nanometer precision in the recombination zone of the device [1]. Most recently, by using a microcontact printing (stamping) process, we demonstrated that neat layers of QDs can be placed independently of the organic layers and in-plane patterned, allowing for the pixel formation necessary for display technology (Figure 1). To date, we demonstrated QD-LED color emission across the visible part of the spectrum and from 1.3μm to 1.6μm in the near infra-red (Figure 2).

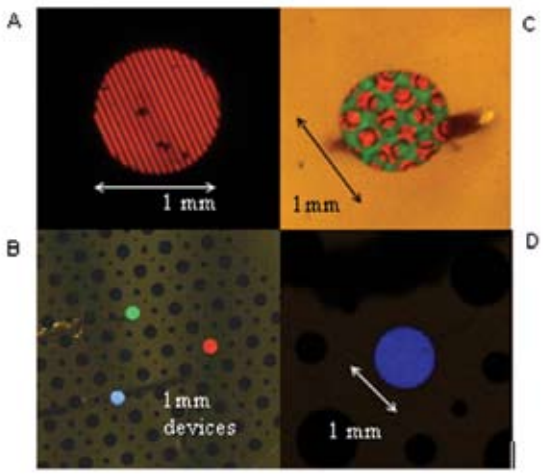

Figure 1: (A) A 25-um-wide, lined, red QD-LED, patterned by microcontact printing (stamping). (B) Stamped red QD-LED, stamped green QD-LED, and blue organic LED. (C) Stamped, patterned, green/red QD-LED. (D) Stamped blue QD-LED.

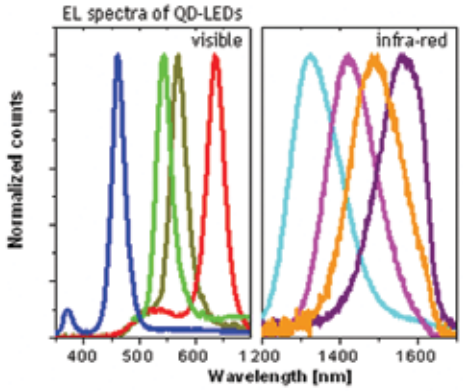

Figure 2: Electroluminescence spectra of QD-LEDs in visible and infra-red.

REFERENCES:

[1] Coe-Sullivan, S., W. Woo, J. Steckel, M.G. Bawendi, V. Bulovic, "Tuning the Performance of Hybrid Organic/Inorganic Quantum Dot Light-Emitting Devices," *Organic Electronics* 4, 123 (2003).

Quantum Dot Light-Emitting Devices

S. Coe-Sullivan, P. Anikeeva, J. Steckel, M. Bawendi, V. Bulovic
Sponsorship: Presidential Early Career Award for Scientists and Engineers, ISN, NSF-MRSEC, Deshpande Center

Hybrid organic/inorganic light-emitting devices (QD-LEDs) combine stability and color clarity of semiconductor nanoparticles and low-cost processing procedures of organic materials with the aim to generate a flat-panel-display technology. Semiconductor quantum dots (QDs) are nanocrystals that are of smaller diameter than the Bohr exciton in a bulk crystal of the same material. By reducing the size of the nanocrystal, quantum confinement effects lead to an increase in the band-edge, exciton energy. Changing QD sizes and materials can produce luminescence wavelength from UV, trough visible spectrum, and near-IR.

A typical QD-LED consists of a transparent inorganic anode deposited on a glass substrate followed by organic electron (ETL) and hole transport layers (HTL) with a QD monolayer in between. A metal cathode is deposited on top of the structure as Figures 1 and 2 (left) show. We are presently investigating physical mechanisms that govern light generation in QD-LEDs. Time-resolved optical methods allow us to study charge and exciton transport in organic films and at organic/QD interfaces, as in Figure 2 (right). Physical insights lead to an optimized design and improved performance of QD-LEDs.

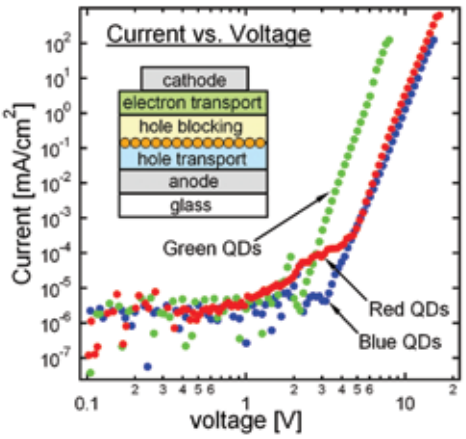

Figure 1: Current-Voltage (IV) characteristics of QD-LEDs with monolayers of red, green, and blue QDs as the recombination layers. Top left corner:structure of the device.

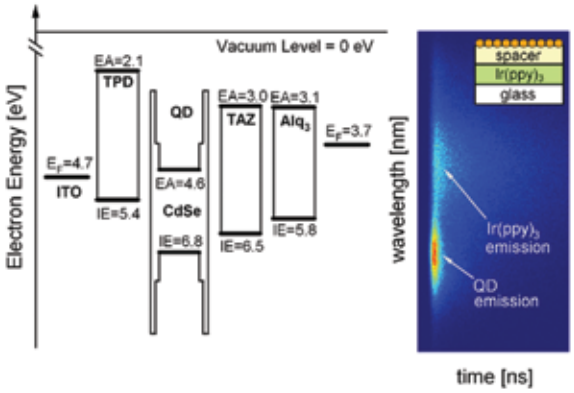

Figure 2: On the left: level diagram of a typical QD-LED. On the right: time-resolved photoluminescence measurement of the structure on the top right corner.

Development of Terahertz Quantum-Cascade Lasers

B. Williams, H. Callebaut, S. Kumar, S. Kohen, Q. Hu, in collaboration with Dr. J. Reno (Sandia National Lab)
Sponsorship: NSF, NASA, AFOSR, DOD NDSEG Fellowship

The terahertz frequency range (1-10 THz) has long remained undeveloped, mainly due to the lack of compact, coherent radiation sources. Transitions between subbands in semiconductor quantum wells were suggested as a method to generate long-wavelength radiation at customizable frequencies. However, because of difficulties in achieving population inversion between narrowly separated sub-bands and mode confinement at long wavelengths, THz lasers based on intersubband transitions were developed only very recently. Taking a completely novel approach, we have developed THz quantum-cascade lasers based on resonant-phonon-assisted depopulation and using metal-metal waveguides for mode confinement. The schematics of both features are illustrated in Figure 1. Combining these two unique features, we have developed many THz QCLs with record performance, including a maximum-pulsed-operating temperature at 164 K (Figure 2), a maximum-cw-operating temperature at 117 K (Figure 3), and the longest wavelength (~141μm) QCL to date without the assistance of magnetic fields (Figure 4).

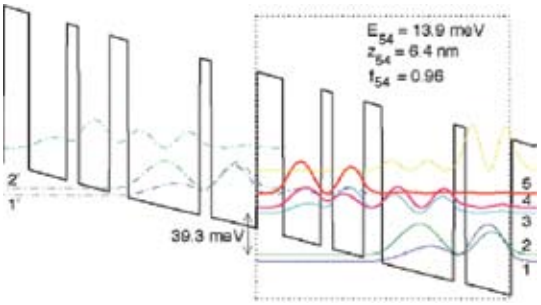

Figure 1

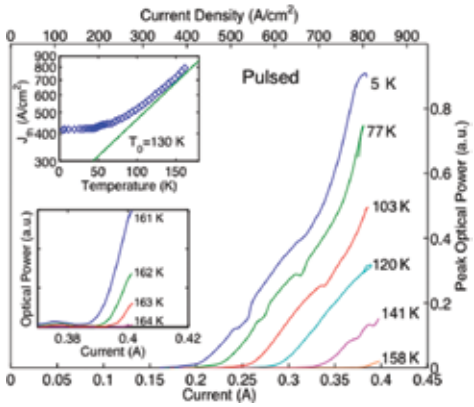

Figure 2

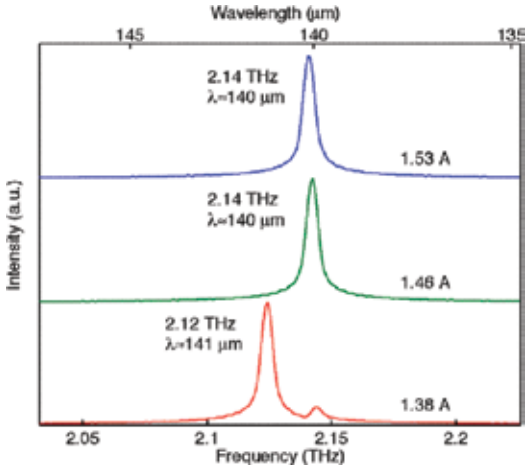

Figure 3

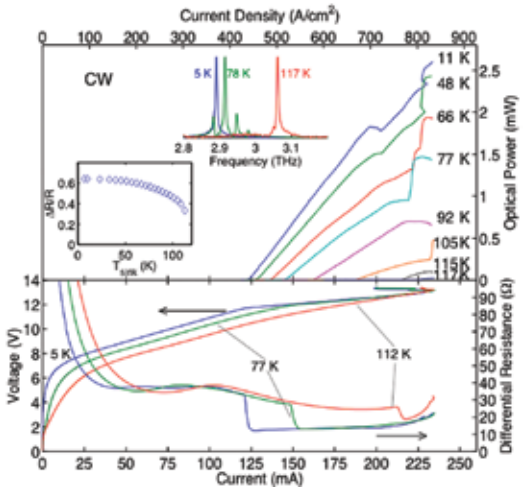

Figure 4

Broadband, Saturable, Bragg Reflectors for Mode-locking, Ultrafast Lasers

S. Tandon, J. Gopinath, H. Shen, G. Petrich, F. Kaertner, E. Ippen, L. Kolodziejski
Sponsorship: ONR MURI

Broadband Saturable Bragg Reflectors (SBR) consisting of monolithically integrated absorbers onto GaAs-based Bragg-mirrors have been used in a variety of ultra-short pulse lasers. The absorber, high-index layers and layer thicknesses are selected based on the laser's wavelength. In contrast, the low-index layer is always Al_xO_y that was created by the wet oxidation of AlAs layers. Reflectivity measurements of a variety of fabricated SBRs are shown in Figure 1.

Infrared SBRs are composed of AlGaAs/Al_xO_y mirrors with InGaAs-based absorbers which strain the structure and, depending on the absorber thickness, may lead to delamination during the AlAs oxidation process. Figure 2(a) shows a plan view of a fully oxidized 500μm diameter SBR that is designed for operation at λ=1230nm. The cross-sectional view (Figure 2(b)) shows the delaminated absorber consisting of the highly strained 80nm thick InGaAs quantum well with GaAs cladding layers and a 7-pair $Al_{0.3}Ga_{0.7}As/Al_xO_y$ mirror stack. For oxidation temperatures between 410°C and 435°C, delamination occurs between the absorber and mirror layers. More severe delamination occurs at higher oxidation temperatures. In an alternate SBR design, the additional strain introduced by the InP cladding layers generally increases the observed amount of delamination. A controlled temperature ramp before and after oxidation has greatly reduced the delamination of the SBR structures despite the presence of strain.

The same AlAs oxidation technique also enables the fabrication of visible SBRs. Using $In_{0.5}Ga_{0.15}Al_{0.35}P$ as the high-index layer and Al_xO_y, Bragg mirrors are created for operation below 800 nm. Along with a GaAs absorber layer, these visible SBRs are nominally unstrained and may mode-lock a variety of lasers including Ti:Sapphire, Cr:LiSAF, Cr:LiCAF, and Cr:LiSGaF. Figures 2(c) and 2(d) show a plan view and a cross-sectional view of one such SBR.

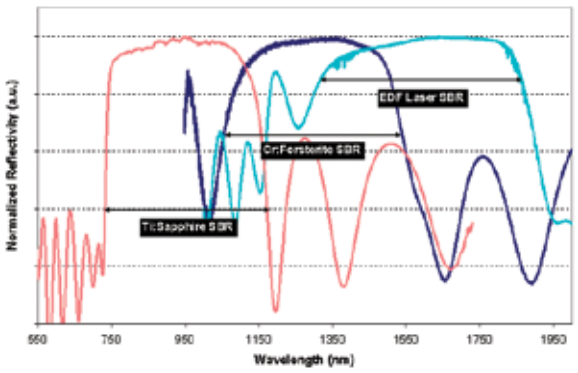

Figure 1: Reflectivity measurements of SBR structures fabricated for three different laser systems: Ti:Sapphire, Cr:Forsterite, and Er-doped fiber (EDF) laser. The Ti:Sapphire SBR was measured with a microspectrophotometer (courtesy of Filmetrics, Inc.). SBRs for the Cr:Forsterite and EDF lasers were measured using Fourier Transform Infrared Spectroscopy.

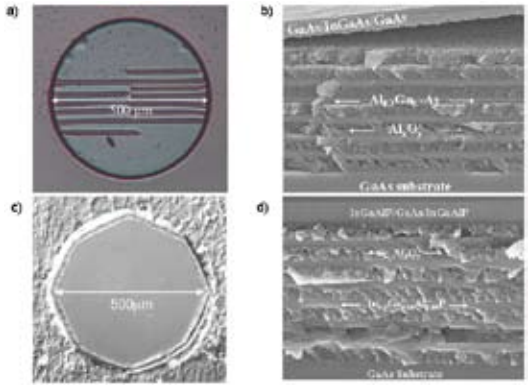

Figure 2: a) Differential Interference Contrast (DIC) image of a fully-oxidized infrared SBR. b) Cross-sectional SEM image showing delamination of the absorber layers from the mirror stack. c) DIC image of fully-oxidized visible SBR. d) Cross-sectional SEM image showing the GaAs-based absorber with a 7 pair InGaAlP/Al_xO_y mirror stack.

Approaching the InP-Lattice Constant on GaAs

N.J. Quitoriano, E.A. Fitzgerald
Sponsorship: Walsin Lihwa

Integrating different materials onto the Si platform brings new functionality to silicon. Using InP on silicon could allow the integration of optical and electronic (e.g., CMOS) devices. By growing high-quality GaAs on silicon, our group has been able to demonstrate a GaAs laser on silicon. Our research goal is to expand the lattice constant beyond GaAs and grow high-quality InP on GaAs. Having explored many materials systems and methods (e.g., InGaAs, InGaP, and InGaAlAs), to date, we have grown low-dislocation-density $In_{(0.43)}Al_{(0.57)}As$ on GaAs with a dislocation density of 1.4E6/cm^2, more than an order-of-magnitude fewer dislocations than in typical commercial metamorphic buffers. After achieving high-quality InP on GaAs, we will work to grow InP on Si. Bringing low-defect density InP onto Si may bring high-speed, InP-based devices into new markets because the processing and material-cost, for a given area will be drastically reduced and allow for high-frequency and/or low-power operation.

Figure 1: Plan-view TEM of $In_{(0.43)}Al_{(0.57)}As$ on GaAs with a dislocation density of 1.4E6/cm^2.

Figure 2: Cross-section of $In_{(0.43)}Al_{(0.57)}As$ on GaAs.

Growth and Characterization of High Quality Metamorphic Quantum Well Structure on GaAs

H.K.H. Choy, C.G. Fonstad, Jr
Sponsorship: Charles Stark Draper Laboratory, NSF

A potentially useful technique to extend the emission wavelength of quantum well (QW) lasers on GaAs substrates is to fabricate the laser structures metamorphically on compositionally graded InGaAs buffers. In such buffers, the indium fraction is increased gradually as growth proceeds. This results in steady elongation of the existing dislocations along the growth surface, releasing the additional strain, and the density of threading dislocations can be minimized. Mismatched metamorphic materials have been grown with the use of graded buffers for over 30 years and the most notable successes are mainly in electronic applications, such as InGaAs HEMTs on GaAs, and strained Si or SiGe high mobility MOSFETs on Si. The adaptation of graded buffers to optoelectronic devices, on the contrary, has been much slower, and we have been working to change this situation.

We have recently demonstrated that the use of *ex-situ* thermal annealing can yield a 30-fold improvement in the photoluminescence (PL) of aluminum-containing single QW structures grown on top of compositionally graded InGaAs buffers [1]. By analyzing the variations of low temperature PL from both the barriers and from the QW as functions of the annealing temperatures, as shown in Figure 1, we have concluded that two processes are involved in the annealing process: a faster one in the barriers and a much slower one in the QW region. By annealing diode structures on the graded buffers, we also observed a large increase in the reverse-biased breakdown voltage from ≈ 0V, due to tunneling through the mid-gap states, to 23V: the avalanche breakdown voltage of the diodes, as Figure 2 shows. Additional QW PL enhancement is found by annealing the samples at a much lower temperature, 700°C, for an extended duration of 20 minutes. With enough carrier confinement in the QWs and with the proper annealing scheme, we obtain emission from metamorphically grown QWs as strong as, and sometimes even stronger than, that from similar single QW structures pseudomorphically grown on GaAs.

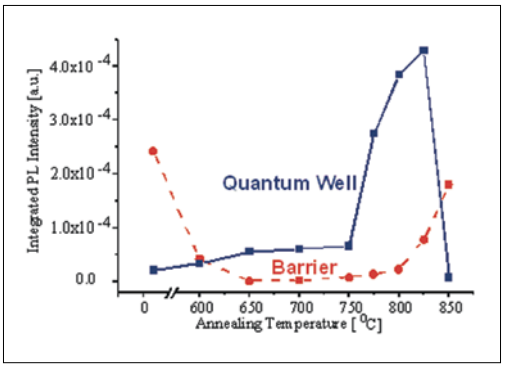

Figure 1: Integrated low temperature (19K) PL intensities from the QWs and the barriers as a function of the annealing temperature.

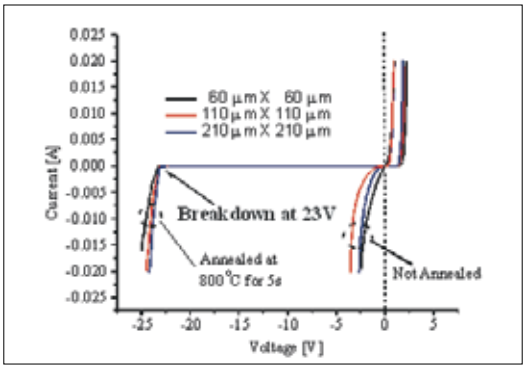

Figure 2: I-V characteristics of the diodes before and after 5 s rapid thermal annealing at 800 °C..

REFERENCES:

[1] Choy, H.K.H., "Quantum Wells on Indium Gallium Arsenide Compositionally Graded Buffers Realized by Molecular Beam Epitaxy," Ph.D. Thesis, EECS, MIT, January 2005

[2} Choy, H.K.H., C.G. Fonstad, Jr., "Enhanced Room Temperature PL from Metamorphic InGaAs/ InGaAlAs Quantum Wells on InGaAs Graded Buffers after Thermal Annealing," submitted for publication, in review.

Strain-Induced Photoluminescence Degradation in Metamorphically Grown InGaAs Quantum Wells

H.K.H. Choy, C.G. Fonstad, Jr
Sponsorship: Charles Stark Draper Laboratory, SMA, NSF

We have recently demonstrated that room-temperature PL of both tensilely and compressively strained quantum wells (QWs) grown metamorphically on graded buffers is strongly degraded relative to that of unstrained wells grown metamorphically on the same substrates [1]. For compressively strained QWs, it was found that the strain also brings about a strong temperature dependence of the PL. The integrated room-temperature and low temperature (19K) PL intensities are plotted against the indium compositions in the QWs in Figures 1 and 2, respectively. The degradation can be partially suppressed by reducing the grading rate of the buffer, by using a superlattice after the growth of the buffer, or by inserting a single 5-nm, tensile-strained GaAs layer and a 30-s growth interruption immediately before the growth of the QW. The PL can also be significantly improved if the substrate temperature during the growth of the graded buffers is reduced when the indium content in the graded buffer is high.

Our observations lead us to conclude that the degradation we observe, which has not been observed previously, is unrelated to the Matthews-Blakeslee process. We, instead, believe that the degradation is most likely related to the surface morphology introduced by the graded buffers, and that the surface roughness, which develops during growth of graded buffer layers plays the key role in the reduction. We also propose that one may eliminate the degradation by smoothing the linearly graded buffer layer using chemical-mechanical polishing (CMP) prior to growing a metamorphic QW structure on it. Such a sequence, if successful, offers another pathway to producing long-wavelength opto-electronic devices on GaAs substrates.

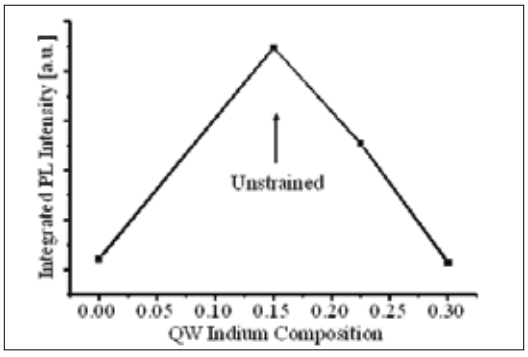

Figure 1: The integrated room temperature-PL intensities plotted against the indium compositions in the QWs.

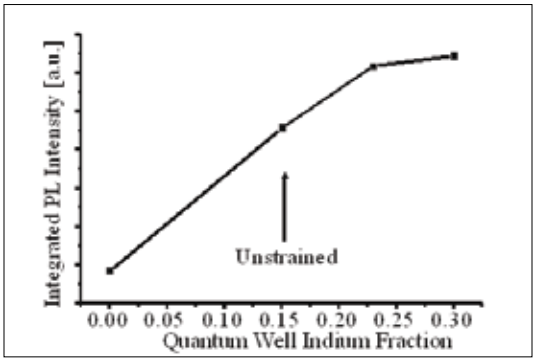

Figure 2: The integrated low temperature (19K) PL intensities of the same set of samples as in Figure 1.

REFERENCES:

[1] Choy, H.K.H., "Quantum Wells on Indium Gallium Arsenide Compositionally Graded Buffers Realized by Molecular-beam Epitaxy," Ph.D Thesis, EECS, MIT, Cambridge (MA): 2005. See also by same authors: "Strain-induced Photoluminescence Degradation of InGaAs/ InGaAlAs Quantum Wells Grown Metamorphically on InGaAs Graded Buffers," submitted for publication, in review.

Monolithic Integration of InAlGaP-based Yellow-green Light Sources on Silicon

M.J. Mori, J.W. Wu, L. McGill, E.A. Fitzgerald
Sponsorship: MARCO MSD, ARO, NSF-GOALI

Unlike those of the III-Nitrides, the lattice parameters of the InAlGaP system are amenable to integration on silicon. The wide, direct bandgap of InAlGaP makes the material an excellent candidate for green-light emission, for which the human eye is the most sensitive. We are working to optimize and integrate yellow-green-emitting devices monolithically on silicon via compositionally graded buffers. With integration, high-efficiency micro-displays with lithographically defined pixels as well as CMOS-driver electronics are possible. Additionally, since absorption length is a strong function of photon energy in silicon, yellow-green wavelengths (where $\alpha_{Si} \sim 10^4\ cm^{-1}$) are optimal for high-speed, low-cost Si photodetectors. With a bright light source, this visible wavelength may be the best choice for chip-to-chip optical interconnects. Our current work focuses on InAlGaP materials with lattice parameters near that of GaAs and we have already demonstrated a yellow-green epitaxial-transparant-substrate light-emitting diode (LED) in [1]. These LEDs will be directly ported to silicon substrates with our optimized, compositionally graded buffer technologies (such as InGaP/GaP or SiGe/Si), which enable high-quality lattice-mismatched epitaxy of InAlGaP. The LEDs consist of an undoped, compressively strained quantum well (QW) grown on an $In_{0.22}(Al_{0.2}Ga_{0.8})_{0.78}P/\nabla_x[In_x(Al_{0.2}Ga_{0.8})_{1-x}P]$/GaP virtual substrate. Theoretical modeling of the structure predicts an accessible wavelength range of approximately 540nm to 590nm (green to amber). Peak emission at 570nm was observed by cathodoluminescence studies of undoped structures with a QW composition of $In_{0.35}Ga_{0.65}P$. The QW-LEDs emit with a primary peak at 590nm and a secondary peak at 560nm. The highest LED power of 0.18μW per facet at 20mA was observed for a QW composition of $In_{0.32}Ga_{0.68}P$ and a bulk threading dislocation density on the order of $7x10^6\ cm^{-2}$. Based upon superspots present in electron diffraction from the quantum well region, we believe that the observed spectrum is the result of emission from ordered and disordered domains in the active region.

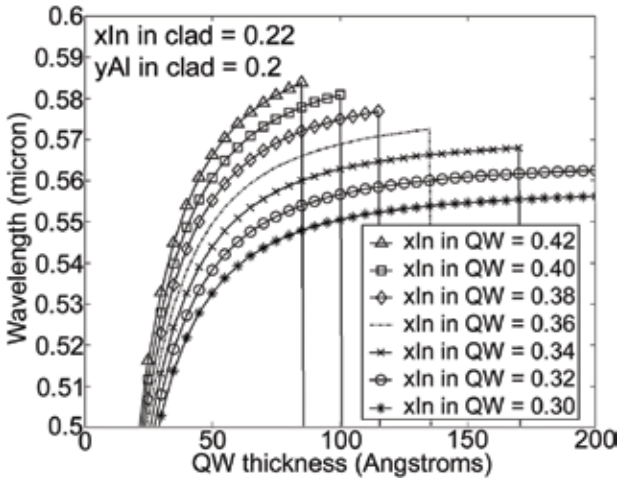

Figure 1: Predicted emission for subcritical-thickness quantum-well devices with $In_{0.22}(Al_{0.2}Ga_{0.8})_{0.78}P$ cladding and an $In_xGa_{1-x}P$ strained quantum well. Vertical lines represent the critical-thickness cutoff.

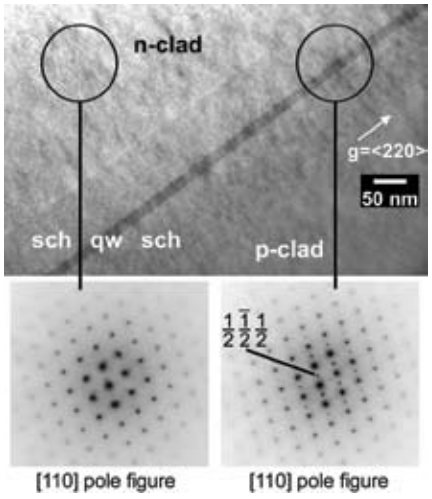

Figure 2: Cross-section transmission electron micrograph of a device with an $In_{0.32}Ga_{0.68}P$ quantum well. Electron diffraction of the quantum well shows ordering superspots, while the clad does not.

REFERENCES:

[1] McGill, L., J. W. Wu, E.A. Fitzgerald, "Yellow-green Strained-InGaP Quantum-well Epitaxial-transparent-substrate Light-emitting Diodes," *Journal of Applied Physics*, vol. 95, pp. 7561-7566, June 2004.

Mid-10^5 cm^{-2} Threading Dislocation Density in Optimized High-Ge Content Relaxed Graded SiGe for III-V Integration with Si

D.M. Isaacson, A.J. Pitera, C.L. Dohrman, S. Gupta, E.A. Fitzgerald
Sponsorship: MARCO MSD

The relaxed graded SiGe platform ($\nabla_x[Si_{1-x}Ge_x]/Si$) has been enormously successful for fabricating high-mobility strained-Si and strained-Ge devices, as well as for the $Ge/\nabla_x[Si_{1-x}Ge_x]/Si$ platform for the subsequent growth of III-V devices, such as: lasers, waveguides, and high-efficiency solar cells. The key feature of the relaxed graded SiGe buffer approach is its effectiveness at minimizing threading dislocation densities, thereby allowing for fabrication of scaleable $Ge/\nabla_x[Si_{1-x}Ge_x]/Si$ structures with TDD values on the order of 10^6 cm^{-2}.

Despite these successes, two key factors have room for improvement with respect to III-V integration on SiGe buffer: a further reduction in the threading dislocation density as well as a reduction in the high thermal mismatch portion of the SiGe buffer. This work presents a framework for achieving these goals. By avoiding dislocation nucleation in $Si_{1-x}Ge_x$ layers of $x>0.96$, we have achieved a relaxed $Si_{0.04}Ge_{0.96}$ platform on Si(001) offcut 2° that has a threading dislocation density of 7.4×10^5 cm^{-2}, with no fundamental limitation to obtaining lower values. This 2° offcut orientation was determined to be the minimum necessary for growth of GaAs without anti-phase boundaries (APBs). Furthermore, we found that we could compositionally grade the Ge content in the high-Ge portion of the buffer at up to 17%Ge μm^{-1} with no penalty to the threading dislocation density. The reduction in both threading dislocation density and buffer thickness exhibited by our method is an especially significant development for relatively thick III-V based minority-carrier devices, such as multi-junction solar cells and vertical cavity surface emitting lasers.

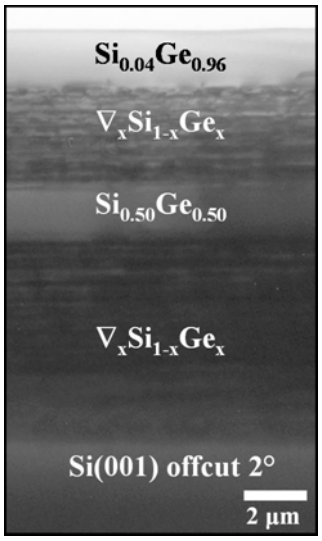

Figure 1: Cross-sectional transmission electron microscopy image of the optimized $Si_{0.04}Ge_{0.96}/\nabla_x[Si_{1-x}Ge_x]/Si$ platform.

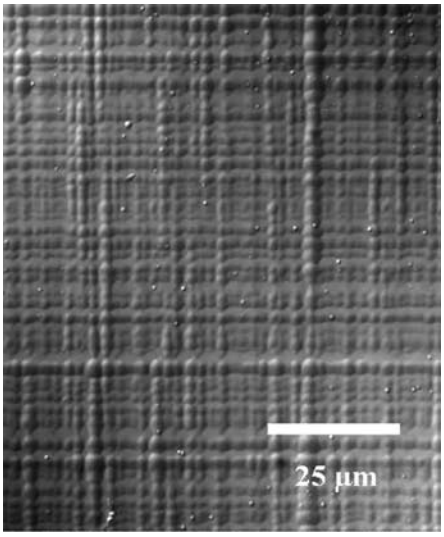

Figure 2: Nomarski etch-pit density image of the optimized $Si_{0.04}Ge_{0.96}/\nabla_x[Si_{1-x}Ge_x]/Si$ platform.

A Bonding Apparatus for OptoPill Assembly

M.S. Teo, C.G. Fonstad, Jr.
Sponsorship: MARCO IFC, NSF

The central objective of our heterogeneous integration effort is to integrate III-V functionality, such as laser emission, with Si-CMOS circuitry in a manner that retains all of the advantages of multi-wafer, batch processing that have propelled Si ICs along the Moore's Law performance timeline for so long. To this end, we have developed Recess Mounting with Monolithic Integration, RM^3, in which we place III-V heterostructure pills, or OptoPills, in recesses 5 to 6 microns deep and 50 microns in diameter that are formed in the inter-metal dielectric layers covering a processed Si IC, and then interconnect them monolithically with the underlying circuitry.

Once the hetero-structure device pills have been placed in their recesses, whether using micro-scale pick-and-place or fluidic self-assembly (both described in other abstracts), they must be securely fastened in place. Making a good electrical contact to the bottom of the pill is often desired at the same time. Two different solders have been found particularly suitable for this purpose: a Au-Sn eutectic to solder gold-coated pills into the recesses and a Pd-Sn-Pd stack to bond bare pills into the recesses. In both cases it is necessary to supply pressure between the pill and substrate to reliably achieve successful bonding or soldering. To apply the required pressure to these micro-scale pills, particularly when they are in recesses, we have developed a bonding system, shown in Figure 1, in which a vacuum-bagging film and a pressure differential are used to apply a controlled, reproducible, and uniform pressure simultaneously to all the pills on a wafer. A photograph of the unit, with the outer chamber removed so the film is visible, appears in Figure 2. Typical bonding conditions apply a pressure of approximately 50 psi and a temperature of approximately 300°C.

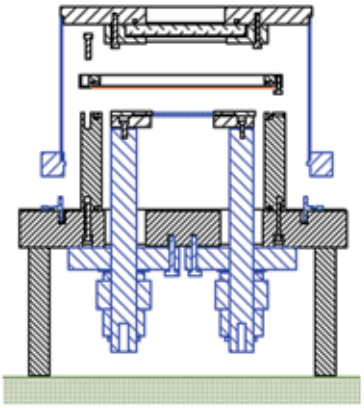

Figure 1: Cross-sectional drawing of the bonding chamber showing the base plate with heater strip, the inner bonding-ambient chamber, the film holder plate, and the outer pressurized chamber.

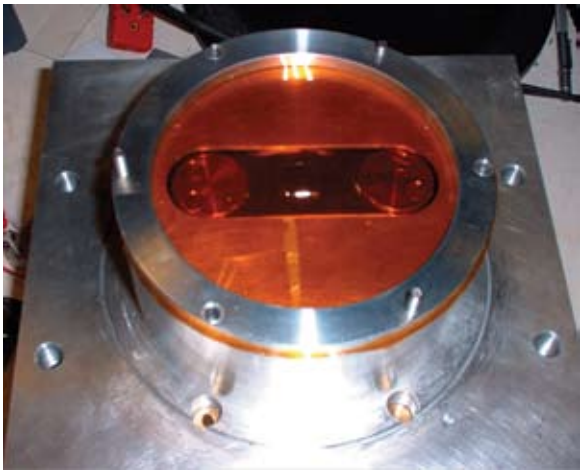

Figure 2: The film-pressure bonding system shown with the outer, pressurized chamber removed to show the film and heater strip.

REFERENCES:

[1] Teo, M.S., "Development of Pick-and-Place Techniques for Monolithic OptoPill Integration," S.M. Thesis, Department of Electrical Engineering and Computer Science, MIT, January, 2005, unpublished.

Micro-scale Pick-and-Place Integration of III-V Devices on Silicon

M.S. Teo, D. Chang, C.G. Fonstad, Jr.
Sponsorship: MARCO IFC, NSF

We are developing micro-scale assembly techniques for integrating III-V optoelectronic devices on silicon integrated circuits that blur the practical distinction between hybrid and monolithic integration. Our general approach, which we term Recess Mounting with Monolithic Integration, or RM^3, involves forming recesses 5 to 6 microns deep and 50 microns in diameter in the inter-metal dielectric layers covering a processed Si IC. After all of the standard silicon processing is completed, the Si IC wafers for RM^3 integration undergo further back-end processing, first to create the recesses, and then to place and bond III-V device structures in them. Wafer-level processing is continued to complete any remaining III-V device processing and to interconnect those devices with the underlying electronic circuitry. One approach we have taken to placing the III-V devices in recesses has been to form discrete heterostructure pills the size of the recesses, and to place them individually into the recesses using micro-scale pick-and-place assembly, as illustrated in Figure 1.

The dimensions of the device pills we are assembling are much smaller than the device die normally used in pick-and-place applications, and thus conventionally available vacuum pick-up tools are unsuitable. We have found, however, that quartz micropipettes of the type used by microbiologists to study cells can be fabricated with the right dimensions and geometry for this application. In particular, we use micropipettes pulled from 1-mm-diameter, 0.25-mm-wall quartz tubing and tapered down over 7 mm to a tip diameter of 30 microns. The tip is beveled at 45° to complete the pick-up tool. A photomicrograph of a tool mounted in its holder is shown in Figure 2. With this tool, pills can be picked up, placed in a recess, and released without damage [1].

Our current effort is directed at using micro-scale pick-and-place assembly to do heterogeneous integration and further developing and refining the technique.

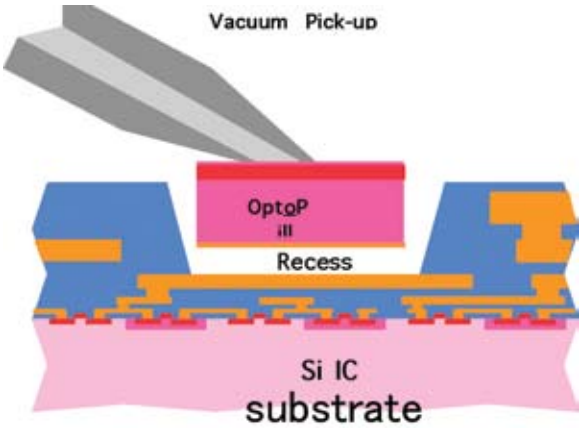

Figure 1: A cartoon illustrating the micro-scale pick-and-place process for locating a heterostructure device pill in a recess on a Si IC wafer surface.

Figure 2: A quartz micropipette pick-up tool mounted on its holder.

REFERENCES:

[1] Teo, M.S. "Development of Pick-and-Place Techniques for Monolithic OptoPill Integration," S.M. Thesis, Department of Electrical Engineering and Computer Science, MIT, January 2005, unpublished.

Magnetically Assisted Statistical Assembly of III-V Devices on CMOS

J. Rumpler, J.M. Perkins, C.G. Fonstad, Jr.
Sponsorship: SRC, MARCO IFC, NSF, SMA

We are researching an efficient process for integrating III-V devices on silicon CMOS using fluidic self-assembly and a unique magnetic retention mechanism. Specifically, III-V devices and silicon ICs will first be processed separately. Dielectric recesses 5 to 6 microns deep and 50 to 60 microns in diameter will then be formed on the IC wafer surface, and permanent ferromagnetic films will be deposited and patterned at the bottoms of these recesses. The III-V devices will be etched into similarly sized pillars that will then be embedded in a polymer, and the substrate will be removed. A permeable ferromagnetic film will next be patterned on the back side of the devices, and they will be released from the polymer. The resulting pills will be cascaded over the CMOS wafer in a fluid, where they will fall into the recesses and be retained by short-range magnetic forces. They will finally be bonded in place and interconnected with the underlying electronic circuitry, using techniques developed in our earlier integration research.

We have demonstrated experimentally that the proposed magnetic retention works and that pills formed, as just described are attracted to and held by patterned magnetized films [1]. We have also conducted fluidic assembly experiments in which thousands of 45 μ diameter, 6 micron thick III-V pills are flowed over a target substrate containing hundreds of correspondingly sized dielectric recesses in the apparatus shown in Figure 1. Initial fluidic assembly experiments without magnetic retention show that a large number of pills can be successfully assembled, as shown in Figure 2, but it is also found that the pills readily come out of the recesses when, for example, the substrate is removed from the fluid. This clearly demonstrates that a short-range retention force is essential to a practical self-assembly process, and in the near future, we hope to demonstrate high yield assembly and retention using magnetic attraction.

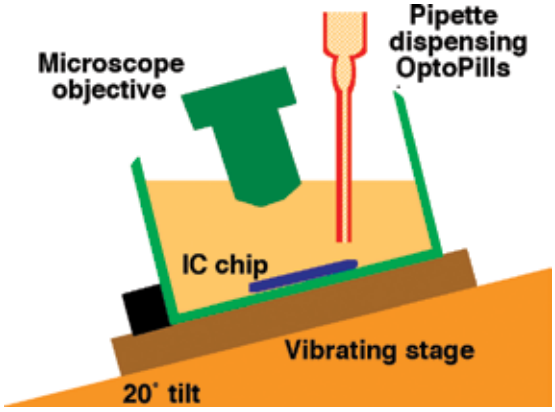

Figure 1: Assembly setup.

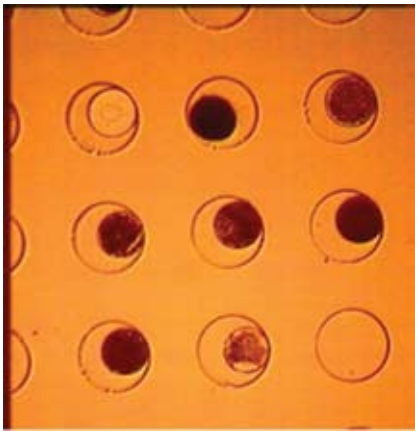

Figure 2: An array of silicon dioxide recesses filled by GaAs devices.

REFERENCES:

[1] Rumper, J.J., J.A. Perkins, C.G. Fonstad, Jr., "Use of Patterned Magnetic Films to Retain Devices During Fluidic Self-Assembly," to be submitted for publication.

Integration of 1.5-µm P-i-N Diodes on Si ICs for Optical Clocking and Interconnects

Y.-S. V. Lei, C.G. Fonstad, Jr. in collaboration with D. Boning
Sponsorship: MARCO IFC

An important issue faced by designers of high performance microprocessors is distributing the clocking signals uniformly across an integrated circuit chip. While transistor dimensions are successfully being aggressively scaled down to meet the insatiable demand for higher processor speeds, the accompanying shrinkage of metal interconnect dimensions has led to increased signal propagation delays, and to severe clock distribution problems. Distributing clock signals optically, rather than electrically, may offer a solution to this problem because doing so eliminates many of the problems associated with electrical interconnect lines. To explore this option, we are applying our optoelectronic integration techniques to integrate of III-V semiconductor P-i-N photodiodes on a variation-robust Si-CMOS optical clock receiver circuit (which is shown in Figure 1) that has been designed by Prof. Boning and his group at MIT. The integration technique employed is referred to as recess-mounting with monolithic metallization, or RM^3 integration for short. The integration process involves several major steps: a) recess formation, b) assembly and bonding of the photonic device heterostructures [1], c) ohmic contact formation, d) device active area definition, e) planarization and passivation, f) via opening, and g) top metallization [2].

Our recent focus has been on the fourth step in this sequence, in particular on refinement of the dry etching technique process for defining the photodiode active region. A process employing BCl_3/He chemistry has shown particularly promising results. The next step will be to fabricate discrete InGaAs/InP photodiodes in order to study and characterize their electrical and optical behaviors independently from the Si-CMOS circuits. Then we will use the processes and technology we have developed to integrated similar photodiodes on the Si-CMOS circuit chip shown in Figure 1.

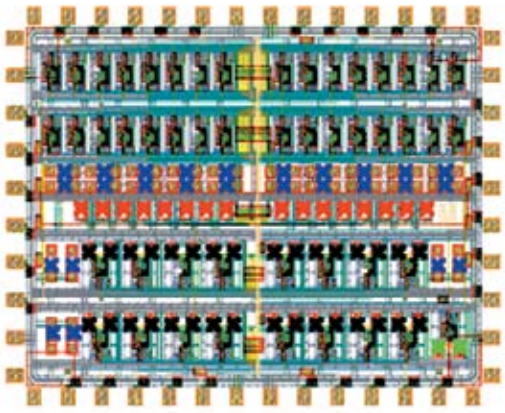

Figure 1: The layout of a Si-CMOS optical clock distribution chip designed by Professor Boning's group at MIT. The 60-x 60-µm recesses (marked with "X"s) are areas where the photo-diode will be placed. The die is 2.7mm x 2.1mm.

REFERENCES:

[1] Teo, M.S., "Development of Pick-and-Place Techniques for Monolithic OptoPill Integration," S.M. Thesis, Department of Electrical Engineering and Computer Science, MIT, January, 2005, unpublished.

[2] Lei, Y.V., "Post-Assembly-Process Development for Monolithic OptoPill Integration on Silicon CMOS" Ph.D. Thesis, EECS, MIT, June 2004.

Integration of III-V In-Plane SOAs and Laser Diodes with Dielectric Waveguides on Silicon

E.R. Barkley, J.J. Rumpler, S. Famini, C.G. Fonstad, Jr.
Sponsorship: DARPA through ARL

The successful implementation of optical interconnects on silicon requires the ability both to integrate III-V optoelectronic devices on silicon substrates with dielectric waveguides and to achieve low-loss optical coupling between the devices and the waveguides. Building on the success of ongoing research in recessed mounting with monolithic metallization (RM^3) of III-V device pills on silicon [1], this project ultimately seeks to demonstrate optical amplification of an on-chip signal through an RM^3 integrated InP/InGaAsP semiconductor optical amplifiers (SOA) and low-loss end-fire coupling from an integrated, edge-emitting laser diode to a dielectric waveguide. A schematic of a III-V SOA integrated with a silicon oxynitride waveguide is shown in Figure 1.

At this stage of the project, the focus falls on developing a process and design that enable low loss coupling between the waveguide and the III-V device. Achieving low loss coupling requires careful processing to ensure smooth sidewalls and facets and attention to the optical mode characteristics of the waveguiding components. Silicon oxynitride waveguides have been fabricated and are currently undergoing testing; Figure 2 shows a cross-sectional SEM photograph of a representative guide. Finite difference time domain (FDTD) simulations have been run to quantify the anticipated coupling loss as a function of the waveguide-to-SOA separation. Based on previous device placement and mounting results, an estimated 2-μm separation is achievable, corresponding to a 4dB/facet loss, as obtained from FDTD simulations.

As a supplement to the ongoing RM^3 research, a micro-cleave technique is being explored as a way of obtaining cleaved facets on small (100 μm x 50 μm) III-V devices. This technique will enable laser length definition with micron-level precision. Future work will involve exploring additional ways of decreasing the waveguide to device coupling losses using, for example, anti-reflection coated devices and tapered waveguides.

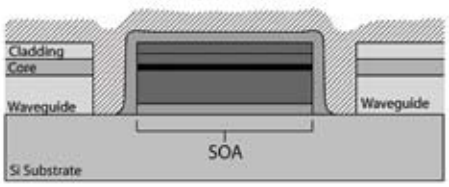

Figure 1: Schematic of an SOA integrated with a dielectric waveguide.

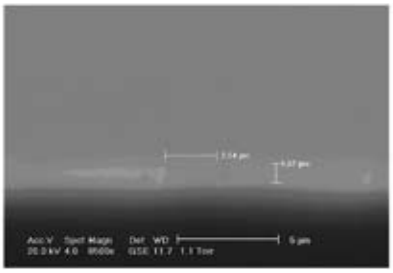

Figure 2: SEM of the waveguide cross-section.

REFERENCES:

[1] See companion abstracts in this document for more information on the RM^3 integration process: A) "Microscale Pick-and-Place Integration of III-V Devices on Silicon" Teo, Chang, Fonstad. B) "Magnetically Assisted Statistical Assembly of III-V Devices on CMOS," Rumpler, Perkins, Fonstad

Integration of VCSELs on Si ICs for Free-Space Optical Neural Network Signal Processing

J.M. Perkins, C.G. Fonstad, Jr., in collaboration with T. Simpkins, C. Warde
Sponsorship: NSF, SRC

This research aims to integrate AlGaAs vertical-cavity, surface-emitting lasers (VCSELs) onto silicon integrated circuits, using integration techniques developed and refined by Professor Fonstad's group. In these techniques, such as Micro-scale Pick-and-Place (MPAP) and Magnetically Assisted Statistical Assembly (MASA) [1], device pills are bonded in recesses on a silicon wafer surface and connected monolithically to the underlying silicon circuitry. In this study the pills will be small cylindrical III-V disks around 75 microns in diameter and 7 microns in height. Each pill will contain one partially processed VCSELs fabricated on campus from a commercially grown AlGaAs epi-wafer. The necessary heterostructure design has been completed and the epi-wafers have been ordered. A processes flow for the fabrication of the VCSEL devices has also been designed and is currently under development. The structure will utilize an oxide current-confinement layer. Once the mask design has been finalized for the semiconductor etching and the metallization steps, the processing of VCSEL devices will begin. These devices will first be measured on their native substrate to test their basic functionality. The VCSEL devices can then be freed from their substrate and bonded onto a Si IC substrate. New technology must be developed to release pills with an InGaP etch-stop layer, and to deposit and pattern metal on the backs of the released pills.

The specific application this work pursues is a free-space, optical neural network array signal processor [2], which will use a 3x3 array of VCSELs in each pixel, shown in Figure 1, and holographic elements between pixel planes, shown in Figure 2, to allow communication between each pixel in one array, to any of nine different pixels in the following pixel array. For this reason, the VCSELs in this study will emit at 850nm, a wavelength compatible with silicon detectors. Professor Cardinal Warde and his MIT students are responsible for the array and optics parts of the effort.

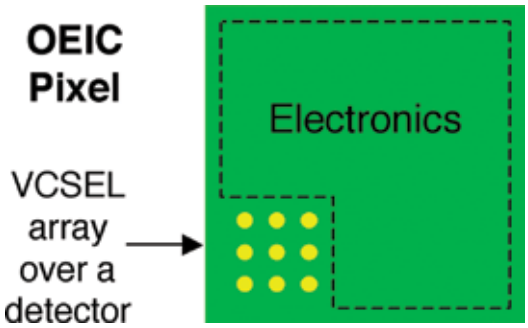

Figure 1: A schematic illustration of a typical pixel in the arrays on each level of the free-space, optical neura network array signal processor under development. The 3x3 VCSEL array will allow communication to any of nine pixels in the next level of the multi-level system.

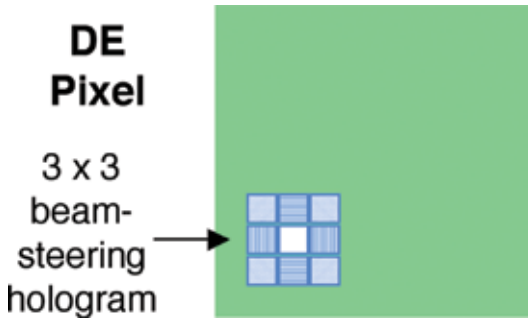

Figure 2: A schematic illustration of a typical pixel in the dielectric element arrays between the OEIC pixel arrays described in Figure 1. The beam-steering hologram directs the output of each of the nine VCSELs in a pixel to the detectors associated with each of nine different pixels on the next plane of OEIC pixels.

REFERENCES:

[1] Fonstad, C.G. Jr., "Magnetically Assisted Statistical Assembly - A New Heterogeneous Integration Technique," Singapore-MIT Alliance Symposium, Jan 2002, unpublished; M. S. Teo. "`Development of Pick-and-Place Assembly Techniques for Monolithic OptoPill Integration," S. M. Thesis, MIT Department of Electrical Engineering and Computer Science. January 2005, unpublished.

[2] Warde, C, C.G. Fonstad, Jr., "Compact Optoelectronic Neural Co-processor Project," in Proceedings of the International Conference on Opto-electronics and Laser Applications, ICOLA '02, October 2-3, 2002, Jakarta, Indonesia, pp. B07-B11.

Germanium Photodetectors for Silicon Microphotonics

J. Liu, D. Ahn, D.T. Danielson, D. Pan, W. Giziewicz, C.-Y. Hong, K. Wada, J. Michel, L.C. Kimerling
Sponsorship: Pirelli Lab, S.P.A., Analog Devices

Silicon microphotonics is emerging as a promising technology for optical communications and on-chip interconnects. One of the critical devices required is a high-performance photodetector compatible with standard silicon complimentary metal-oxide-semiconductor (CMOS) technology. We have demonstrated an epitaxial Ge photodetector on Si as a promising candidate in previous reports. Here we report a higher-performance and broader spectrum Ge photodetector by utilizing tensile strain introduced by the thermal annealing process.

Smooth Ge epitaxial layers with a root-mean-square roughness of ~0.7 nm were selectively grown directly on Si in windows opened through a SiO_2 layer. Due to the thermal expansion mismatch between the Ge epitaxial layer and the Si substrate, 0.20% in-plane tensile strain was introduced into the Ge layer, reducing the direct band-gap of Ge from 0.801 to 0.773 eV and extending the effective photodetection range to 1605 nm. The tensile strain can be further enhanced by the backside silicidation process. The device shows a high responsivity over a broad detection spectrum from 650 to 1605 nm (Figure 1), and a 3 dB bandwidth of 8.5 GHz at a low reverse bias of 1 V (Figure 2), having promising applications in both telecommunications and integrated optical interconnects.

One other important component in optical circuitry is the integration of photodetectors and waveguides. Integration benefits detector performance by circumventing the usual trade-off problem between responsivity and bandwidth. In contrast to the more common III-V materials case in which both waveguide and photodetector are lattice-matched semiconductor materials and are grown in one-step epitaxial process, we adopted SiON/Si_3N_4 dielectric materials for waveguides and group IV Si/Ge materials for photodetectors, for monolithic integration with a Si CMOS chip. This design requires a novel coupling structure. We have investigated coupling behavior for Group IV integrated photodetectors. We fabricated a photodetector mesa structure with enough cladding height to optically isolate the waveguide from substrate. We employed a CMP planarization step to form a platform on which the waveguide can be deposited. To achieve efficient and uniform optical coupling between waveguide and photodetectors, the effects of design variations are measured and compared with theoretical studies based on analytic modeling and BPM (Beam Propagation Method) optical simulation.

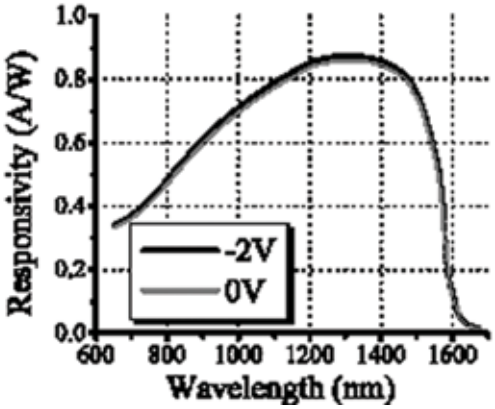

Figure 1: The DC responsivity at 0V and 2V reverse bias in the wavelength range of 650-1650nm without antireflection coating.

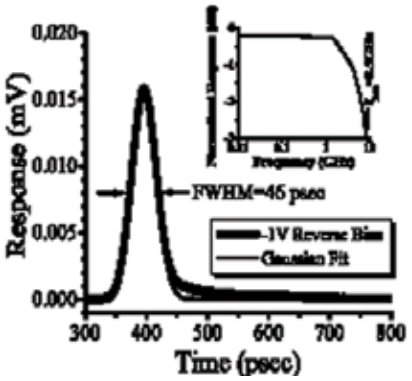

Figure 2: Temporal response of a 10×70μm Ge/Si photodetecter at a reverse bias of 1V to ~1 ps-long pulses generated by a mode-locked Yb-fiber laser at 1040 nm (black line). The inset of the figure shows the Fourier transform of the pulse, which gives a 3 dB bandwidth of 8.5GHz.

Quantum Dot Photodetectors

A.C. Arango, D.C. Oertel, M.G. Bawendi, V. Bulovic
Sponsorship: MIT ISN

Solution-processable colloidal quantum-dot systems exhibit many of the special optical and electronic properties associated with epitaxially grown, quantum confined systems. Their tunable band gap and higher absorption relative to the bulk make quantum dots particularly attractive as photo-generation materials. At the same time, colloidal quantum dots offer much greater material system flexibility than epitaxial quantum dots because deposition on any substrate is possible.

Efficient photoconductivity has previously been observed in lateral device structures consisting of single thin quantum dot films [1]. Response time of this device was limited by charge transport, suggesting that a vertical photdetector structure could decrease the response time and support higher currents due to the larger contact cross-sections. That motivates our present project, in which we study the photo-response of quantum dot thin films in a vertical sandwich structure. We engineer a multilayer thin film device with a colloidal quantum dot film inserted into the middle of a wide bandgap structure forming a double heterojunction device that functions as a rectified diode (Figure 1). The rectifying behavior ensures suppression of the shunt current in the reverse-biased structure that can arise from the mechanical imperfections in the quantum dot film. Additionally, the photo-generative quantum dot film can be positioned in the peak of the optical field, increasing the device efficacy. Changing the size and material properties of the quantum dots tunes the response spectrum of the device across visible and near infra-red spectra.

With current-voltage measurements (not shown), we have achieved low dark current and have identified high internal resistance of the cadmiun selenide (CdSe) quantum-dot film as a major limitation to the device performance. The quantum efficiency (number of generated electrons per incident photon) is shown in Figure 2. At present we focus on improving the device performance and optimizing the photodetection response in the 1um-to-2um wavelength region by using lead selenide quantum-dot films.

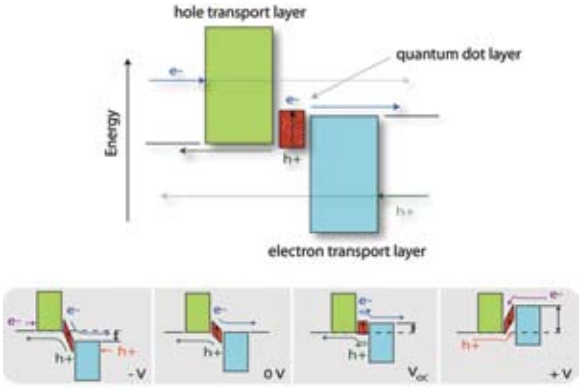

Figure 1: Alignment of energy bands in a conceptual tri-layered p-i-n-like quantum dot hetero-junction photo-detector. The contact layers (indicated in green and blue) serve to transport charge out of the device, block charge from entering the device, and transmit light to the absorbing quantum dot layer. Under applied bias, the proposed device exhibits rectification because charge is blocked at both electrodes under reverse bias yet allowed to enter under forward bias.

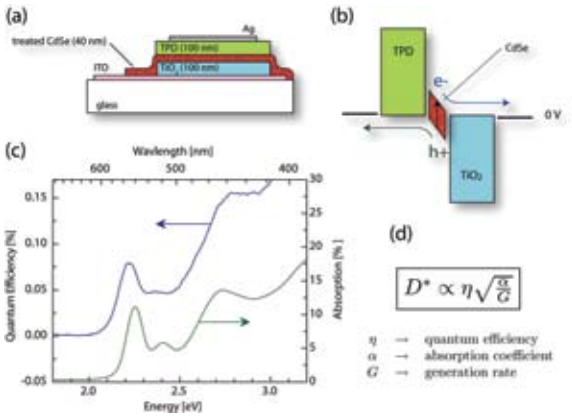

Figure 2: The photo-detector device structure (a) consists of a solution-deposited, colloidal CdSe, quantum-dot layer sandwiched between n-type TiO_2 and a p-type organic semiconductor TPD. At zero bias and under illumination (b), an excited electron can exit the device via the TiO_2 layer, while the corresponding hole can exit via the TPD. The resulting quantum efficiency spectrum at zero bias (c) tracks the shape of the CdSe absorption. An important metric for photo-detectors (especially infrared detectors) is the detectivity D* (d), a measure of a device sensitivity to background noise.

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[1] Jarosz, M.V., V.J. Porter, B.R. Fisher, M.A. Kastner, and M.G. Bawendi, "Photoconductivity Studies of Treated CdSe Quantum Dot Films Exhibiting Increased Exciton Ionization Efficiency," *Phys. Rev. B*, vol. 70, no. 19, art. 195327, November 2004.

Integrated Emitter/Detector/Electronics Arrays for Diffuse Optical Tomography

C.G. Fonstad, Jr., W.P. Giziewicz, in collaboration with C. Saunders, D. Brooks, S. Prasad, R. Gagnon (Northeastern University)
Sponsorship: NSF

Biomedical imaging and sensing may benefit greatly from development of integrated probes because they promise improvements in signal-to-noise ratio, as well as, reduced size and cost. We are working to apply the optoelectronic integration technologies we are developing to create an integrated circuit implementation of a probe for diffuse optical tomography (DOT), in which emitters, detectors, and driver, receiver, and signal-processing circuitry, fabricated in a standard analog CMOS process, are integrated together on a single chip.

The first lot of DOT chips was received from MOSIS in late 2003. Testing indicated that the stand-alone detectors functioned well and as anticipated. Specifically, Gagnon and Giziewicz show that the detectors have the high sensitivity at low light levels, large dynamic range, and low dark currents needed for the targeted DOT applications [1]. The associated detector circuitry, however, did not function properly. Extensive testing led ultimately to the discovery of several layout errors and circuitry errors. These were corrected and another chip design, including most of the original components as well as additional cells and circuitry, was prepared by Giziewicz and submitted to MOSIS in early 2004. Chips were received in June 2004.

Northeastern University S.M. student Christopher Saunders is completing the characterization and testing of the latest chip, and will perform simulated DOT sensing with the chip using external fiber sources. Simultaneously, work is proceeding in another program on the integration of VCSELs on Si CMOS chips; if that work proceeds as planned, emitters will be integrated on the DOT chip as well, and Saunders will test the fully integrated DOT chips before he completes his S.M. thesis research (and the NEU program terminates) at the end of August 2005.

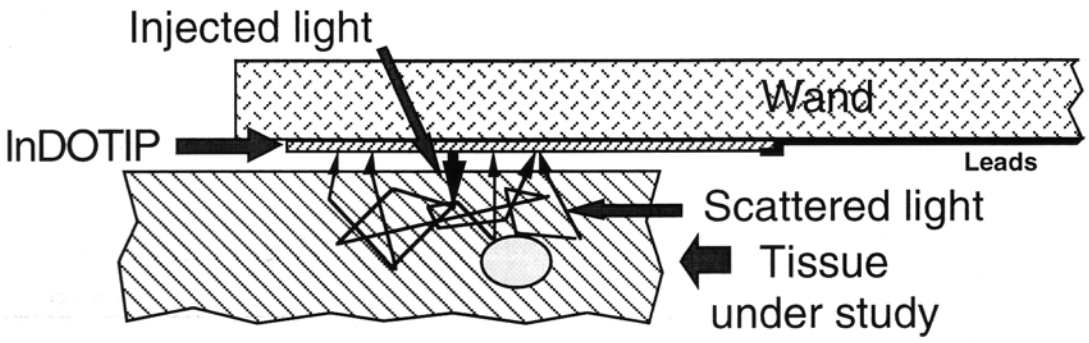

Figure 1: An illustration of one way that the DOT OEIC die might be mounted on the end of a wand and used for DOT subsurface imaging of soft body tissue. In use, each VCSEL is illuminated in turn (the figure shows one turned on) and the pattern of scattered light seen by the detector array is recorded. With this information, an image of the sub-surface structure can be constructed.

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[1] Giziewicz, W.P., R. Gagnon, S. Prasad, D. Brooks, C.G. Fonstad, Jr., "Initial Development of an Integrated Optoelectronic Probe for Biomedical Imaging," Proceedings of the 26th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, EMBC 2004, San Francisco, CA, Vol.3, pp. 2094-2097, 2004.

Fabrication of Superconducting Nanowire, Single-Photon Detectors

J.K.W. Yang, R. Hadfield, G. Gol'tsman, B. Voronov, K.K. Berggren
Sponsorship: MIT Lincoln Laboratory

Several novel applications that rely on high-speed single-photon detectors (SPDs), for example quantum cryptography, have recently emerged. The nanowire SPD consists of a 4-nm-thick, ~ 100-nm-wide, superconducting NbN wire operating at 4.2 K or below. It reportedly detects single photons at 1550-nm wavelength with a detection efficiency (DE) of ~ 5%, which is too low to be of use for most applications. Its proposed GHz-counting rate is several orders of magnitudes faster than has been demonstrated by other types of SPDs to date [1]. The aim of our research is to improve the detection efficiency (DE) of the nanowire SPDs and to make devices capable of GHz-counting rates. Figure 1 shows a scanning electron micrograph (SEM) of a nanowire SPD that consists of closely spaced nanowires in a large-area meander. We are working to improve DE by: (1) using thicker and more optically absorptive NbN films, (2) defining even narrower nanowires, (3) improving the linewidth uniformity, (4) increasing the length of the nanowire (and thus the total area of the meander), and (5) identifying and minimizing sources of material damage (such as electro-static discharge, plasma-damage, and thermal damage). We have recently developed a fabrication process using electron-beam lithography and hydrogen-silsesquioxane (HSQ) resist followed by a reactive-ion etch (RIE). This process, combined with an electron-beam proximity-effect correction technique, allows us to fabricate wires 150-μm long and less than 100-nanometer wide with line-width non-uniformity of ~ 5%, covering an area of ~ 25 μm^2 [2]. Figure 2 shows an SEM image of one of the devices we have made using this process that was 25-nm-wide: the narrowest superconducting nanowire ever fabricated for this type of detector.

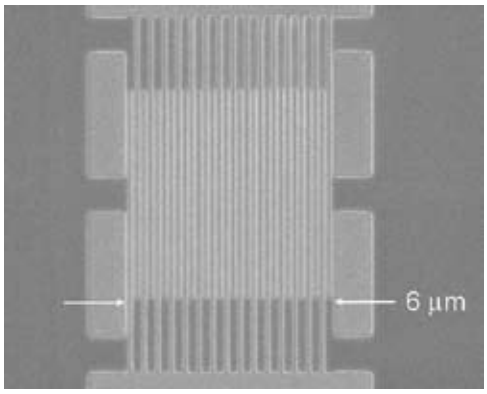

Figure 1: SEM image showing a superconducting nanowire meander structure with uniform 100-nm-wide linewidths, fabricated using electron-beam lithography.

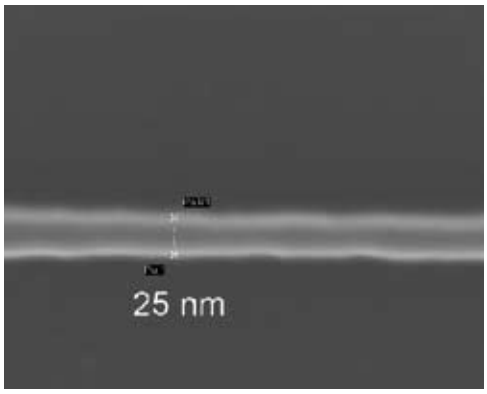

Figure 2: SEM image of the narrowest superconducting wire that we have fabricated. Narrower wires will have higher detection efficiencies.

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[2] Yang, J.K.W., E. Dauler, A. Ferri, A. Pearlman, A. Verevkin, G. Gol'tsman, B. Voronov, R. Sobolewski, W.E. Keicher, and K.K. Berggren, "Fabrication Development for Nanowire GHz-counting-rate, Single-photon Detectors," to be published in *IEEE Transactions on Applied Superconductivity*, 2005.

CMOS-compatible Photodetectors Using Ge-on-Si Films Deposited in an Applied Materials Epitaxial Reactor

O.O. Olubuyide, D.T. Danielson, L.C. Kimerling, J.L. Hoyt, in collaboration with J. Yasaitis (Analog Devices)
Sponsorship: DARPA, Analog Devices, Inc., IBM/SRC Graduate Student Fellowship

Germanium films have the required responsivity and speed to serve as photodetectors at the 1.55 micron range. Such detectors can be used in the communications field in a variety of high-speed systems, such as optical samplers. Thus, integrating Ge films grown on silicon (Ge-on-Si) substrates into a CMOS-compatible process is an attractive goal for making arrays of on-chip detectors that can be used in a range of electronic and photonic integrated circuit applications. In this project, we explore the growth properties and material quality of Ge-on-Si deposited by Low Pressure Chemical Vapor Deposition (LPCVD) in an Applied Materials Epitaxial Reactor, and the optical and electrical properties of Ge-on-Si photodiodes.

It has already been demonstrated in Ultra High Vacuum Chemical Vapor Deposition (UHVCVD) systems that depositing a low temperature Ge layer (seed layer), followed by the deposition of a high temperature layer with subsequent annealing, can create a smooth, planar Ge film on a <100> silicon substrate with threading dislocation density on the order of 10^7 cm^{-2} [1]. We have adapted this two-step deposition process to an LPCVD system. The effect of growth pressure, temperature, and seed thickness on the material quality has been explored. An optimum Ge seed layer deposition process window of 335ºC ± 15ºC and 30 T ± 10 T (Figure 1) is identified and the requirement of a seed layer thickness above 30 nm (Figure 2) is demonstrated. After annealing at 900ºC for 30 minutes, these Ge films have threading dislocation densities of ~2 x 10^7 cm^{-2}. Recently, photodiodes fabricated with these optimized Ge films have been measured to have a dark current of ~1 µA for 50 µm square diodes at – 1 volt bias and a responsivity of 400 mA/W at 1.55 µm.

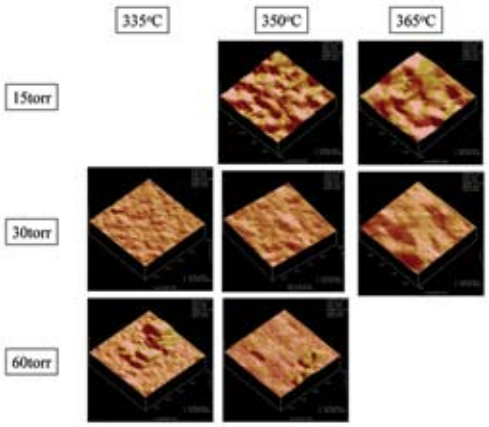

Figure 1: 1 µm x 1 µm AFM scans of Ge seed layers grown at various pressures and temperatures. As pressure increases, the growth rate increases, but gas phase nucleation (bottom panels) becomes an issue. At high temperatures, surface roughness increases due to the higher surface mobility of Ge. Optimum seed growth -conditions are 335ºC at 30 T.

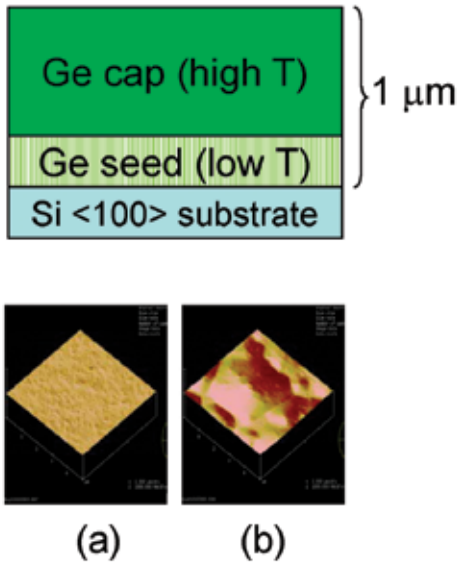

Figure 2: Ge film layer structure and 5 μm x 5 μm AFM scans of 1 μm-thick Ge films with different seed thicknesses: a) 60 nm seed, RMS of 0.9 nm and (b) 30 nm seed, RMS of 29 nm. The thicker 60 nm seed layer (a) has a higher thermal stability during the ramp to high temperatures for the thick Ge cap layer. and thus yields a significantly smoother surface morphology for the Ge film, in comparison to the thinner 30 nm seed layer (b).

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Chemo-sensing Optoelectronic Structures

J. Ho, A. Arango, T. Swager, V. Bulovic
Sponsorship: ISN, NSF-MRSEC

We are developing solid-state, organic device structures capable of efficiently converting analyte detection into an electrical signal. The main advantage to using organic materials is that they are synthetically flexible and can be tailored to respond in a distinct manner to specific analytes. Our proposed device structure is a heterostructure consisting of an optically active, chemo-sensing layer and a charge transport layer. Physically separating the sensing and transport functions in chemical sensors has two significant advantages. First, we can optimize both the sensing and the transport layers independently to maximize chemical sensitivity. Second, we can tailor materials in the sensing layer to detect specific materials, allowing us to reuse the same device structure for a variety of applications.

An integral part of this research is to demonstrate efficient, organic photo-transistors and to physically model their behavior. By building upon models developed for organic transistors, we can begin to explain the behavior or organic photo-transistors. In the photo-transistor structure, light acts as a gate pseudo-electrode by changing the conductivity in the transistor channel to modulate current. Once the photo-transistor model has been developed and the material set has been optimized, the next challenge will be to introduce chemically sensitive materials into the structure of the device to modulate the photo-detection ability of the sensing layer. In this way, we can detect the presence of any analyte. By transducing the sensing response of an analyte into the transport of charge, we can observe a bulk change in the system with only a small number of binding events; thereby increasing the sensitivity of the devices.

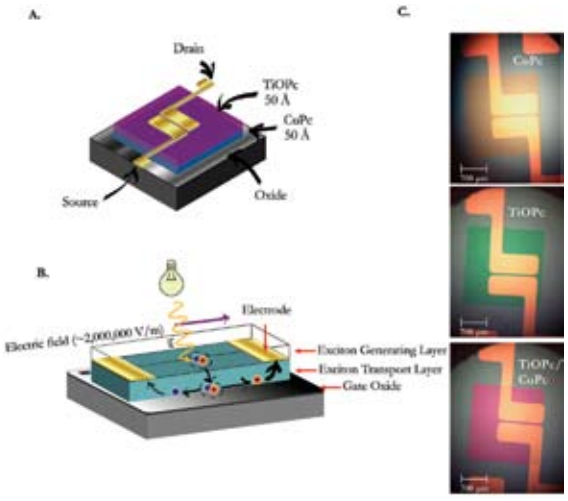

Figure 1: A) Schematic structure of a phototransistor. B) Schematic of phototransistor operation C) Microscope pictures of photoresistors under 40X magnification.

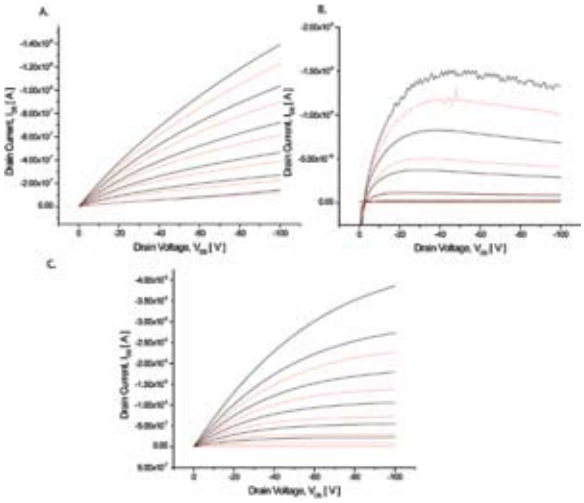

Figure 2: Linear I-V plots of A) 50 Å CuPc, B) 50 Å TiOPc, C) 50 Å CuPc, and 50 Å TiOPc. The dotted red lines represent I-V curves in the absence of light for gate voltages ranging from 0 V to -100 V in steps of -20 V. The dashed black lines represent the same curves In the presence of white illumination. Notice that the heterostructure improves the photo-transistor action.

Sensitivity Gains in Chemosensing by Lasing Action in Organic Optoelectronic Structures

A. Rose, C. Madigan, J. Ho, T. Swager, V. Bulovic
Sponsorship: NASA, ISN, NSF-MRSEC

Societal needs for greater security require dramatic improvements in the sensitivity of chemical and biological sensors for weapons detection. To meet this challenge, increased attention has been directed at materials and devices with highly non-linear characteristics. Semiconductive organic polymers (SOPs) (Figure 1) exemplify a class of amplifying materials which have also been recognized as promising lasing materials, although their susceptibility to optical damage due to photo-oxidation has thus far limited applications.

We recently demonstrated that for photostable SOPs, attenuated lasing in optically-pumped SOP thin films can exhibit more than 30-times higher sensitivity to explosive vapors than can be observed from spontaneous emission [1]. Through optical pumping, amplified stimulated emission was readily observed at sufficiently low pump power so as to prevent SOP bleaching during operation in ambient air. Ambient operation is necessary for applications involving the detection of explosives in the field. Upon exposure of the lasing SOP thin film to vapors of 2,4,6-trinitrotoluene (TNT) and 2,4-dinitrotoluene, cessation of the lasing action is observed and recorded. Associated enhancement of sensitivity is most pronounced when the films are pumped at intensities near their lasing threshold (Figure 2). The responses at low analyte-exposure levels are detectable in the lasing peak before any attenuation appears in the spontaneous emission peak. The strong binding of these nitro-aromatic analytes to electron-rich SOPs and their ease of reduction produce a selective response that is relatively immune to other airborne analytes (no response was observed upon exposure to benzene or naphthalene). Present efforts focus on incorporating SOPs into open, high-Q, optical-feedback structures that will reduce the lasing threshold as well as enhance sensitivity by using thinner active layers.

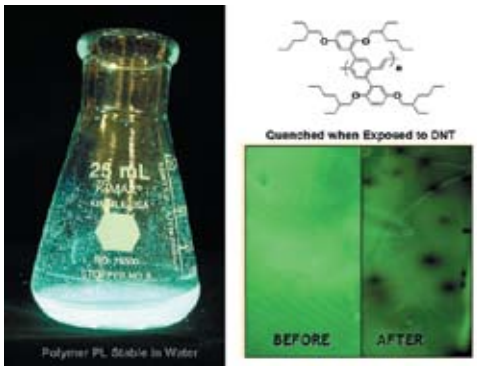

Figure 1: Fluorescence of the SOP in solution and in a thin film (before and after DNT exposure).

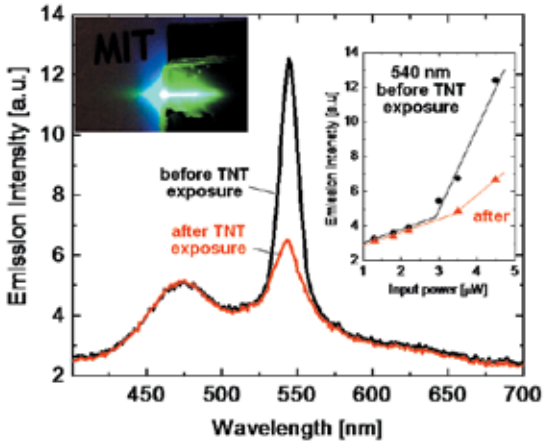

Figure 2: Spectral response of a ring-mode structure consisting of a 25-um-diameter, silica fiber dip-coated with an SOP thin film. The ASE attenuation in the absence of spontaneous emission attenuation after 1.5 min of exposure to saturated TNT vapor pressure. Right inset, plots of ASE peak-emission intensity (wavelength of 535 nm) as a function of excitation power. Left inset pictures a chemo-sensitive SOP thin-film laser.

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Photovoltaics and Thermophotovoltaics

D.T. Danielson, T.M. Montalbo, T. Lin, L. Dal Negro, Y.Yi, K. Wada, L.C. Kimerling
Sponsorship: Shin-Etsu Chemical Corp.

This research program aims to design and prototype a novel photonic microstructure, in conjunction with thin silicon solar cells in order to enhance cell efficiency. The structure should increase the optical path length of wasted photons by creating anomalous refraction effects. We have proposed three-dimensional photonic crystal backside reflectors to achieve the strong bending of the incident light. The fabrication of regular arrays of air macro-pores in silicon (Si) has been achieved by electrochemical etching using DMSO-HF solutions on p-type Si substrates, affording the design advantages of higher solar cell base minority carrier diffusion lengths relative to n-type Si. The strong advantages of our new DMSO etching process are clearly displayed in Figure 1, showing a cross-sectional SEM of our recent porous samples. A depth of 22μm with average pore diameters of approximately 1.6μm was achieved indicating an impressive aspect ratio of ~14. As expected, lateral etching appears to have been suppressed and inter-pore walls are significantly thicker with respect to the samples produced by standard HF/ethanol processes. Additionally, a vertical pore growth rate 15 times greater than that achieved with ethanol as a solvent was achieved, making this process much more amenable to a realistic production environment.

We have successfully fabricated ordered high-aspect ratio macropores in p-type Si with ~1-2μm diameters and relatively thick pore walls through electrochemical anodization. This achievement represents a critical step toward the realization of 3D photonic structures directly integrated on the backside of a p-type Si solar cell to achieve strong light trapping for high-efficiency thin-film Si solar cells.

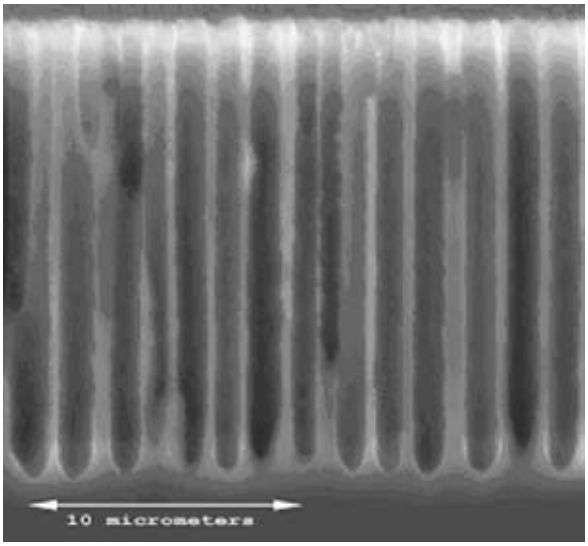

Figure 1: Cross-section SEM image of 30min, 4M HF/DMSO, 15mA/cm^2 porous Si sample

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Concepts and Devices for Micro-scale, Thermo-photovoltaic Energy Conversion

H.K.H. Choy, C.G. Fonstad, Jr., in collaboration with R. Dimatteo (Charles Stark Draper Lab)
Sponsorship: Charles Stark Draper Laboratory

The first-order proximity-enhancement of thermo-photovoltaic energy conversion that we and CSDL demonstrated for the first time several years ago [1, 2] leads to a dramatic and important increase in energy conversion rate but only a modest increase in the efficiency of the conversion process. The challenge we are addressing now is to use the micro-scale geometry (in which the hot and cold surfaces are in extreme proximity) to increase the efficiency of thermo-photovoltaic energy conversion as significantly as we have increased the conversion rate.

Our work supports the C. S. Draper Laboratory (CSDL) effort on micro-scale thermo-photovoltaic (MTPV) electrical power sources. We have provided InAs-based MTPV cells to the CSDL effort; we have analyzed the impact of the enhancement effect on TPV cell performance; and we have evaluated more sophisticated, quantum-effect-based phenomenon that can be used to enhance significantly the energy selectivity of the energy transfer, and thereby dramatically increase the efficiency of the thermal to electrical energy conversion. We have most recently also begun work on dot-junction, back-side-illuminated solar cells. In the past year we have designed an original InGaAlAs-on-InP heterostructure suitable for fabricating high performance dot-junction, back-side illuminated solar cells shown in Figure 1, and proposed an accompanying fabrication sequence. Referring to Figure 1, the uppermost n+ InGaAs layer is the n-side of the junction and a low-resistance contact layer. The InGaAlAs layers shield the minority carriers created in the wide, p-type InGaAs light-absorbing layer from surface recombination; the composition of this layer is graded to eliminate any barrier to electron flow from the absorbing layer to the n-side of the junction. The lowest p+ InGaAs layer reduces resistance as carriers flow laterally to ohmic contacts made to the p-side of the junction. The first sample of this heterostructure has been grown and CSDL researchers are doing fabrication and testing of the first set of devices.

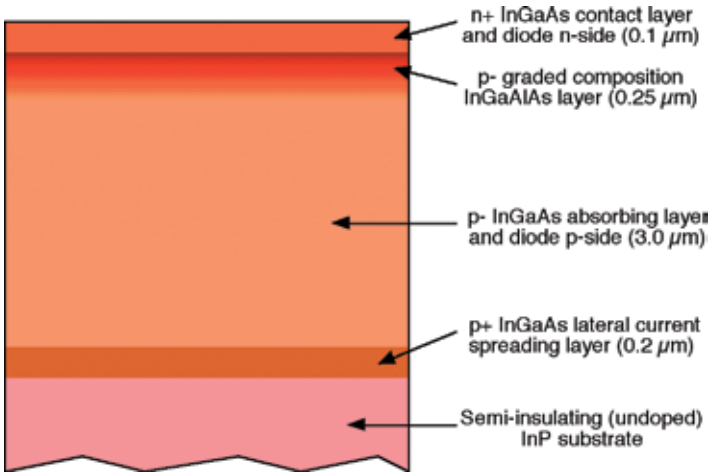

Figure 1: The layer structure for dot-junction, back-illuminated TPV and MTPV cells

REFERENCES:

[1] DiMatteo, R.S., P. Greiff, S.L. Finberg, K.A. Young-Waithe, H.K.H. Choy, M.M. Masaki, C.G. Fonstad, Jr., "Enhanced Photo-generation of Carriers in a Semiconductor via Coupling Across a Non-Isothermal Nano-scale Vacuum Gap," *App. Phys. Lett.* 79, 2001 pp. 1894-1896, 2001.

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Nanoscale, Thermal-Imaging Microscopy

P. Mayer, D. Lueerssen, J. Hudgings, R.J. Ram
Sponsorship: ONR, NSF

Thermo-reflectance microscopy is a widely used means of measuring surface temperature changes that does not require physical contact of the surface (as opposed to the use of thermocouples, for example) combined with a better spatial resolution than IR thermography. A few years ago, Grauby et al. presented a break-though idea that improved the usability of CCDs two-dimensional detection [1]. However, the literature reveals a widespread belief that the temperature resolution of thermo-reflectance is limited to the order of 1K to 0.1. This conclusion stems from the assumption that a typical 12-bit CCD can measure a reflectivity of $R \leq 2^{12}=4096$. At best, the measurable changes are equal to the quantization limit, $\Delta R=1$. Under idealized circumstances (e.g., no noise), the obvious conclusion is that the resolution of the system is $\Delta R/R=2.5 \cdot 10^{-4}$. Intuition suggests that if we include the unavoidable shot noise, the resolution of $\Delta R/R$ can only be worse, but this conclusion is wrong. The resolution is, in fact, better than in the idealized case, and we demonstrate that $\Delta R/R$ can be measured with an uncertainty better than $1 \cdot 10^{-7}$. We utilize noise-induced level-crossing to measure changes in the thermoreflectance better than the limit of quantization of the camera. Using 467-nm light on gold, we have realized 10 mK temperature resolution simultaneously with 250-nm spatial resolution [2].

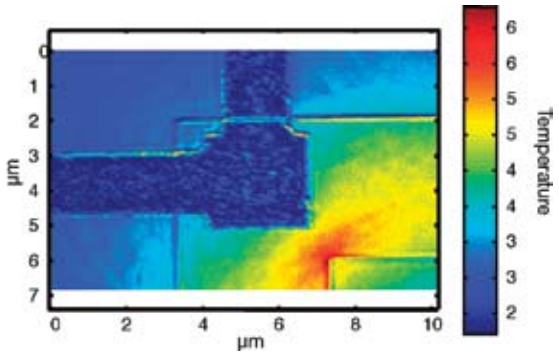

Figure 1: Thermal image of a diffused- Ssilicon resistor. The image shows the excess Joule heating in the inside corner of the resistor.

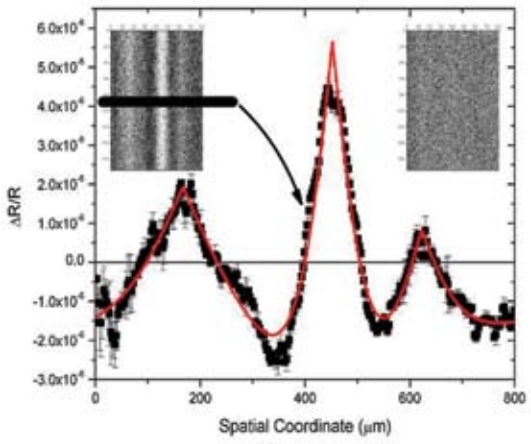

Figure 2: Heating due to non-radiative recombination at defects within a Ssilicon solar cell. The signal level is three orders of magnitude below the CCD-quantization limit.

REFERENCES:

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Digital Holographic Imaging of Microstructured and Biological Objects

J.A. Dominguez-Caballero, J.H. Milgram, G. Barbastathis
Sponsorship: MIT Sea Grant

Digital Holographic Imaging (DHI) is a powerful technique that allows three-dimensional imaging by recording the optical-wave field using a CCD array. This recording is followed by a numerical reconstruction of the image field. The DHI is being employed to characterize micro-structured and biological objects at distances relatively far from the CCD with high lateral resolution. The amplitude and phase information can be retrieved from the reconstructed field, allowing us to obtain a more complete description of the sampled object.

The digital hologram is created by capturing the interference between the wavefronts scattered by an illuminated object and a reference beam. The intensity registered at the CCD plane is given by: $I_{CCD} = |r+o|^2$

where r is the reference field and o is the Fresnel diffracted-object field. The recorded intensity is then multiplied by the digitally generated version of the reference beam (r_D) in order to recover the virtual image. The next step is to reconstruct the object in the image plane by using the diffraction integral. The reconstruction is achieved using the convolution approach:

$T_o = F^{-1}[F(I_{CCD} \cdot r_D) \cdot F(h)]$,

where T_o is the reconstructed field in the image plane; the operators F{} and F^{-1}{} are the forward and inverse Fourier Transforms, respectively, and h is the diffractive kernel. The reconstruction is optimized by using the Fast Fourier Transform algorithms.

Experiments using an in-line configuration reconstructed a USAF 1951 resolution target and a live brine shrimp. The recordings were made using a He-Ne Laser with $\lambda = 632.8$nm. The beam was expanded and split into two paths of equal length, forming a Mach-Zehnder Interferometer. The sampled object was placed in one of the paths and the other path was left clear to form the reference wave. Neutral Density Filters were used to control the relative intensity between the object and reference beams. The hologram was captured using a CCD array of 4096x4096 pixels with a pixel size of 9μm and a fill factor of 100%. Figure 1 shows the reconstruction made for the USAF 1951 resolution target located 15mm away from the CCD array. Figure 2 shows the reconstruction made for the live brine shrimp located at a distance of 167mm. The length of the brine shrimp is, approximately, 5mm.

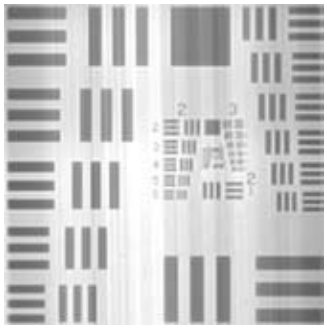

Figure 1: Reconstruction of a USAF 1951 resolution target: z = 15mm.

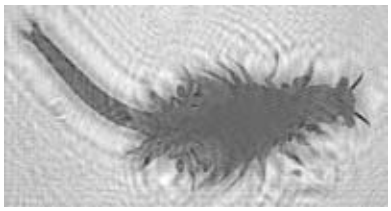

Figure 2: Reconstruction of a live brine shrimp: z = 167mm.

Super-resolution Optical Profilometry Using Maximum-likelihood Estimation

W. Sun, G. Barbastathis, in collaboration with M.A. Neifeld (University of Arizona)
Sponsorship: Montage Program, DARPA

Highly precise and accurate profile measurement is important in various kinds of precision engineering, such as precise parts manufacturing, optical element grounding and polishing, etc. Several techniques have been developed for high-resolution profilometry in different application areas. We presented a number of volume-holographic imaging (VHI) based profilometery systems recently. The VHI-based profilometer optically slices the object to be measured layer-by-layer, and then the acquired raw images from each layer are sent to a computer. The computer reconstructs the 3-D profile of the object. The plane wave reference volume-holographic imaging (PR-VHI) based system with active monochromatic illumination can achieve ≈ 2 mm depth resolution at a 50 cm working distance. For stepwise object metrology, the resolution can be improved to ≈ 50μm at the same working distance. In this report, we present Viterbi Algorithm (VA) based maximum likelihood estimation data processing method for PR-VHI profilometry with multiplexing holograms. The method can resolve object's features at 8 different depth layers with 4 times super-resolution with raw images captured at only one lateral scanning process.

The experimental demonstration of the VA-based, super-resolution VHI profilometry was applied to a plastic LEGO® model. We set the VHI profilometer at the working distance at 50cm. To demonstrate the super-resolution, we deliberately closed down the aperture to degrade the nominal depth resolution to 6.5mm. The active illumination is from a Coherent Verdi®-5 Nd:YAG laser operated at 532nm. We repeated the experiments at the laser output powers of 25mw, 15mw, and 8mw to test the super-resolution performance at different SNR levels. Two multiplexing holograms recorded in a single $LiNbO_3$ crystal were used in the experiment. These two holograms were [consistent tense for experiment] focused on two different depth layers with the spacing of 6.4mm, equivalent to four LEGO® layers. In the profilometery process, the two holograms were set to focus on the 3rd and 6th layers of the LEGO® model (with distances z_1 and z_2 from the PR-VHI system, as shown in Figure 1). With mechanical scanning only at one lateral dimension (x direction shown in Fig. 1), two raw images of the profilometry slices at the 3rd and 6th layers of the LEGO® were acquired. These two slices were then sent to the VA based, post-processing to reconstruct the object. Figure 2 shows reconstructed LEGO models with the VA-based method and cross-correlation-based method . The results show that the VA-method generates a reconstruction almost without error.

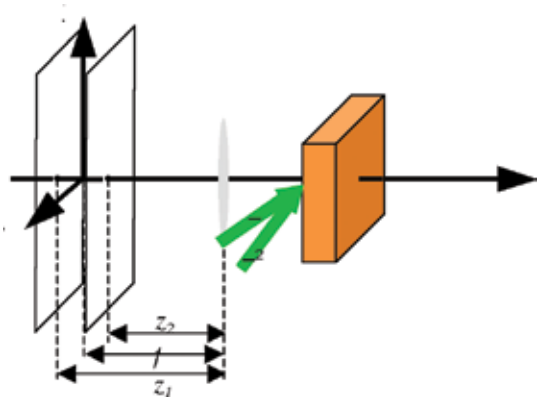

Figure 1: Schematics of the PR-VHI super-resolution experiment with multiplexing holograms.

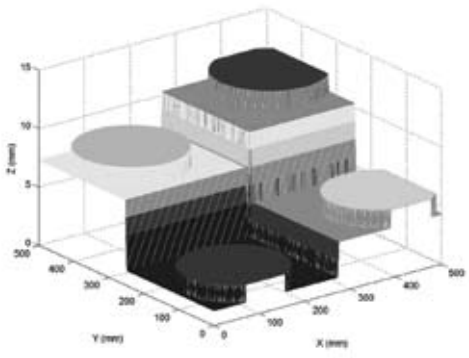

Figure 2: Reconstructed LEGO® model with VA-based post-processing method.

White-light Optical Profilometry at Long Working Distances

W. Sun, G. Barbastathis
Sponsorship: AFOSR, DARPA

We devised a real-time, optical profilometry technique with rainbow-illuminated, volume-holographic imaging (RVHI), as shown in Figure 1. A white light source is first analyzed by a diffraction grating and the object is illuminated by the decomposed rainbow. After passing through a cylindrical lens, the rainbow is focused to the focal plane of a volume holographic lens [a volume holographic lens is a specifically designed volume hologram acting as a lens but with unique optical properties]. The diffraction grating, cylindrical lens, and the objective lens are chosen in so that the rainbow projection on the focal plane satisfies the following coupled angular-wavelength shifting relation [1]:

$$\frac{\Delta\lambda}{\lambda} \approx -\frac{\Delta\theta}{\theta_s}$$

Where λ is the recording wavelengthand $\Delta\theta$ is the desired angular shift to the optical axis of a color component in the rainbow, which has a wavelength shift $\Delta\lambda$. Therefore, all the in-focus points along the *x* dimension are matched; in the *y* dimension they are also Bragg matched because of degeneracy. Thus, the entire rainbow plane is Bragg matched, resulting in a broad field of view (FOV). When shifted out of focus, each point source in the rainbow becomes Bragg mismatched due to defocus, much as a narrow-band source at the same wavelength would [2]. With wide FOV, RVHI can map the height of a reflective object across the entire lateral frame at one shot, without additional scanning. For better accuracy, images of different depth layers can be captured and mapped to different sections of the camera plane by multiplexing holograms [3].

RVHI can be set up in an inclined scheme to further improve depth resolution for profilometry of step-wised objects at a long working distance [4]. The target object (micro-turbine, see Figure 2(a)) is placed 450mm away. Figure 2(b) and (c) show two raw images of a micro-turbine acquired by RVHI at the top surface and the substrate, respectively.

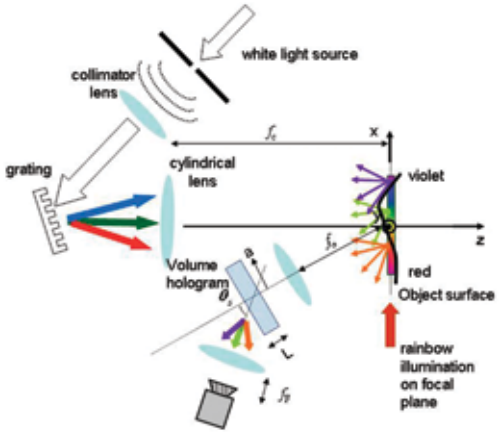

Figure 1: Illustration of rainbow volume holographic imaging system.

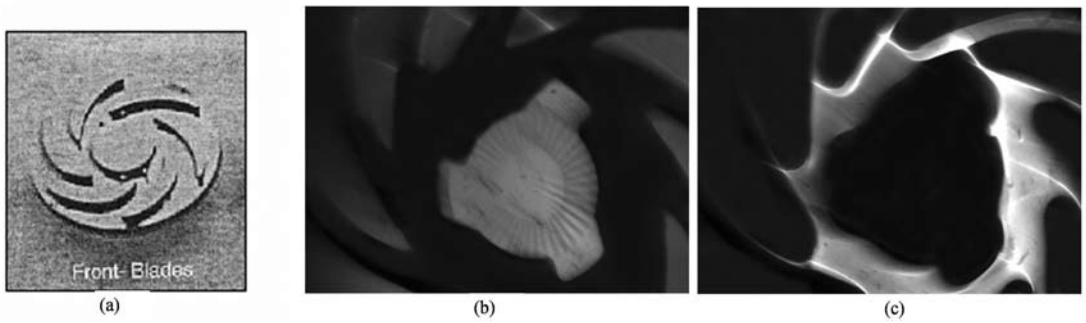

Figure 2: Image acquisition using RVHI: (a) object illuminated with rainbow; (b) and (c) raw images showing depth-selectivity across the rainbow field.

REFERENCES:

[1] Barbastathis, G. and D. Psaltis, "Shift-Multiplexed Holographic Memory Using The Two-Lambda Method," *Opt. Lett. 21*. pp. 432-434, 1996.

[2] A. Sinha, A., W. Sun, T. Shih, and G. Barbastathis, "Volume Holographic Imaging in Transmission Geometry," *App. Opt. 43,* pp. 1533-1551, 2004. [use lower-case letters in journal article as consistent with [1], [3], & [4]

[3] Liu, W., D. Psaltis, G. Barbastathis, "Real-time Spectral Imaging in Three Spatial Dimensions," *Opt. Lett., 27,* pp. 854-856, 2002.

[4] Sinha, A. and G. Barbastathis, " Volume Holographic Imaging for Surface Metrology at Long Working Distance," *Opt. Exp. 11*, pp. 3202-3209, 2003.

Optical Measurement of 3-D Deformation in Transparent Materials

K. Tian, T. Cuingnet, Z. Li, W. Liu, D. Psaltis, G. Barbastathis
Sponsorship: Montage Program

Deformation of volume holograms, such as shrinkage during processing [1], can cause deviation in the angle or wavelength for the Bragg matching condition [2], and aberrations in the reconstructed image. This problem, usually associated with the investigation of holography materials, has received much attention. The deformation models used in the literature are relatively simple, since their target is simple linear deformation. In this paper, we present a generalized theory that can deal with arbitrary deformations. We derived a general expression of the response of a volume grating to arbitrary deformation, using a perturbative approach. We constructed experiments, as shown in Figure 1, to measure the effect of the deformation due to a point-load exerted normally on the surface of a hologram on the diffracted field from both plane-wave transmission and reflection hologram. The experiment results, as Figure 2 shows, are consistent with the theory. Using this technology, we can determine the deformation itself, based on a set of observations of the field diffracted from a known (pre-deformation) volume hologram.

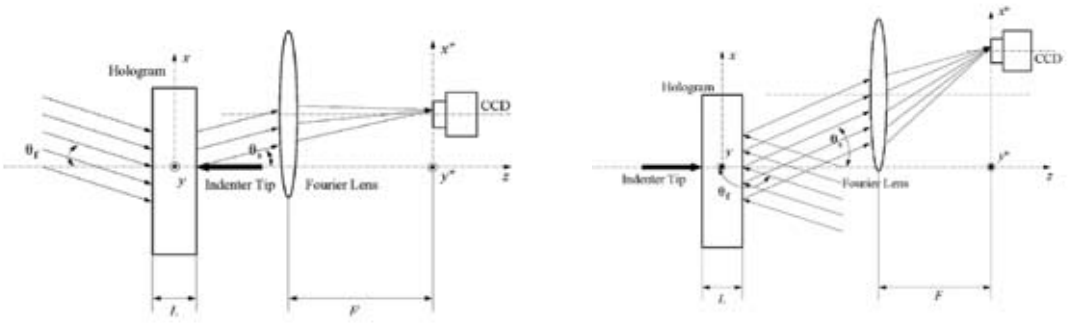

Figure 1: Experimental geometry when a point load is exerted on (a) a transmission- hologram; (b) a reflection hologram

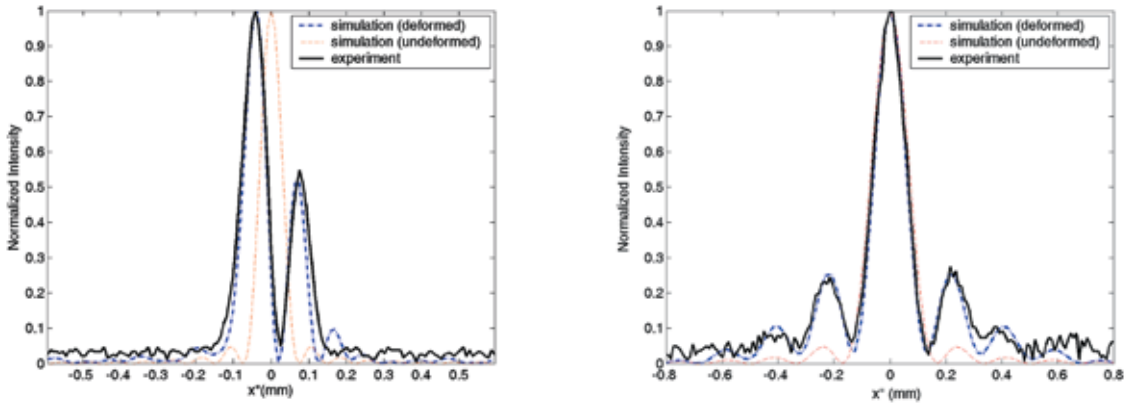

Figure 2: Experimental and simulated results when a point load is exerted on (a) a transmission type hologram and (b) a reflection type hologram

REFERENCES:

[1] Colburn, W.S. and K.A. Haines, *Appl Opt,* 10, pp.1636-1641, 1971; B.L. Booth *Appl Opt.,* 14, pp. 593-601, 1975.
[2] Hariharan, P., Optical Holography: Principles, Techniques, and Applications. Cambridge: Cambridge University Press, 1984.

Light Emitting Aperiodic Photonic Structures

L. Dal Negro, J.H. Yi, V. Nguyen, Y. Yi, J. Michel, L.C. Kimerling
Sponsorship: NSF-MRSEC

The control of light-matter interactions in complex dielectrics without translational invariance offers the ultimate potential for the creation and manipulation of light states. Unlike periodically arranged dielectrics (photonic crystals), aperiodic dielectric arrays show unique light localization and transport properties related to the lack of translational symmetry, and an unprecedented degree of structural complexity. Aperiodic dielectrics can be deterministically generated following simple mathematical rules. They offer significant advantages over randomly generated non-periodic materials in terms of reproducibility, processing, and design. Recently [1,2] we fabricated the first light-emitting silicon-rich, SiN_x/SiO_2 Thue-Morse (T-M) multilayer structures in order to investigate the generation and transmission of light in strongly aperiodic deterministic dielectrics. Photoluminescence and optical transmission data experimentally demonstrate the presence of emission-enhancement effects occurring at wavelengths corresponding to multiple T-M resonance light states. The unprecedented degree of structural flexibility of T-M systems can provide alternative routes towards the fabrication of optically active, multi-wavelength photonic devices.

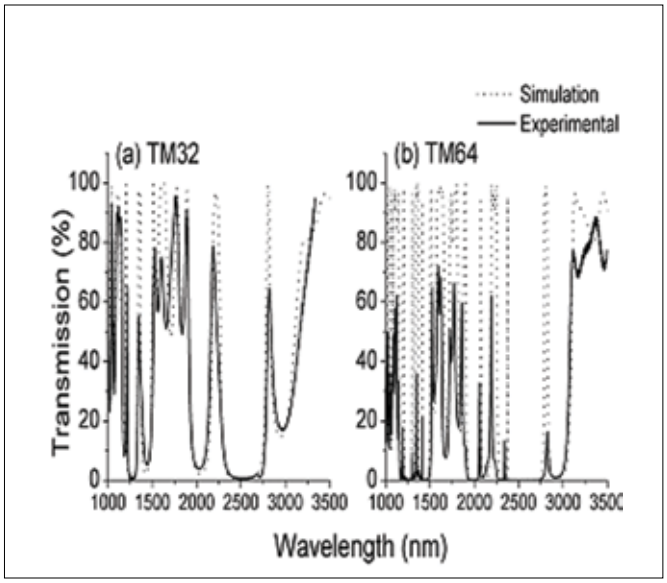

Figure 1. (a) Experimental (solid line) and calculated (dotted line) transmission for the 32-layer T-M structure (TM32); (b) Experimental (solid line) and calculated (dotted line) transmission for the 64-layer T-M structure (TM64). For all the simulations we have considered n_A=2.23 (SiN_x), n_B=1.45 (SiO_2). The thickness simulation parameters that yield the best fit with the experimental transmission data are d_A=198.9 nm and d_B=273 nm, which are approximately 6% thicker and 4% thinner than the targeted values defined by the Bragg condition at l_0 =1.65 mm.

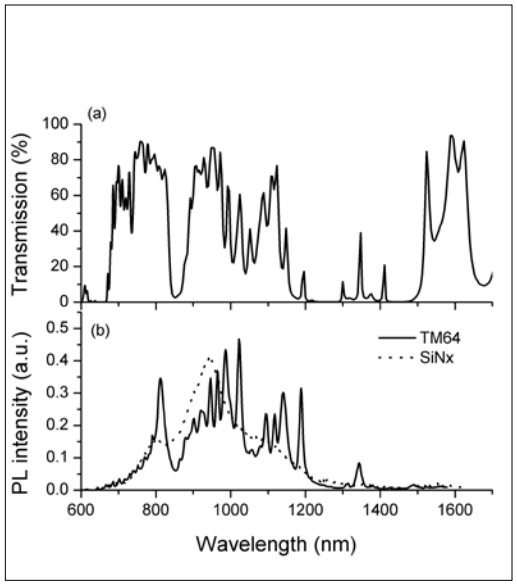

Figure 2. (a) Experimental transmission for the 64-layer T-M structure; (b) Comparison of the room-temperature TM64 emission spectrum and the homogeneous SiN_x -reference-sample emission spectrum . The pump power was 5mW.

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[1] Dal Negro, L., J.H. Yi, V. Nguyen, Y. Yi, J. Michel and L.C. Kimerling, "Light Emission in Aperiodic Thue-Morse Dielectrics," *Proceedings of MRS*, 92331, F1.3 2005.

[2] Dal Negro, L., J.H. Yi, Y. Yi, V. Nguyen, J. Michel, L.C. Kimerling, "Spectrally Enhanced Light Emission from Aperiodic Photonic Structures" accepted for publication, *Appl. Phys. Lett.*, 2005 .

Photonic Crystals

L. Zeng, Y. Yi, C.-Y. Hong, X. Duan, L.C. Kimerling
Sponsorship: National Renewable Energy Laboratory (NREL), CMSE

In order to improve thin film solar cell efficiency, it is important to enhance the optical path length by trapping light in the cell. We have successfully developed a new light-trapping scheme, which combines a reflection grating in the substrate with a distributed Bragg reflector (DBR). It can enhance optical path length by more than 10^4 times with little loss of reflection. Consequently, incident light can be almost completely absorbed. In turn, we expect the quantum efficiency of the solar cell based on our photonic structure to be improved significantly.

In the year 2004, we achieved rapid progress in several aspects:

- We have fabricated high-quality DBRs with extremely high reflectivity that agrees well with simulation. For instance, using 5 pairs of Si/Si_3N_4 gives a reflectivity of 99.6%, whereas that for Si/SiO_2 is 99.98%.
- We have successfully developed a practical fabrication process for the silicon grating DBR by the following steps: first, optical projection lithography is used to pattern the Si substrate into gratings with periods on the order of wavelength; then a plasma etch is used to accurately control etch-depth; the last step is to deposit DBR stacks using LPCVD or DCVD. Figure 1 is the SEM image of Si grating with one pair of Si_3N_4/Si.
- Our Si grating displayed strong light bending effects (Figure 2). We have set up a measurement system that has a tunable-wavelength laser source and a detector that can be rotated over 180 degrees, allowing accurate determination of the reflected light direction and intensity.

The next step is to integrate the new back-reflector with simple solar cells to verify cell-efficiency improvement.

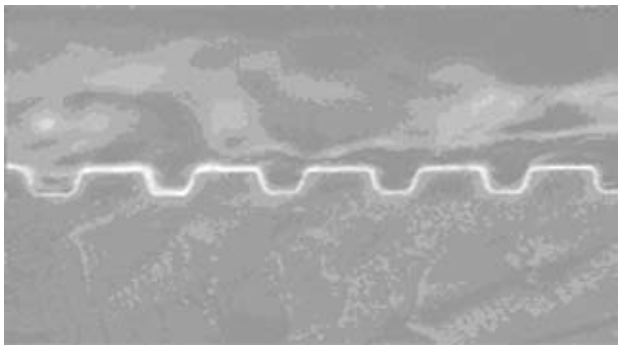

Figure 1: An SEM image of a Si grating with one pair of Si_3N_4/Si

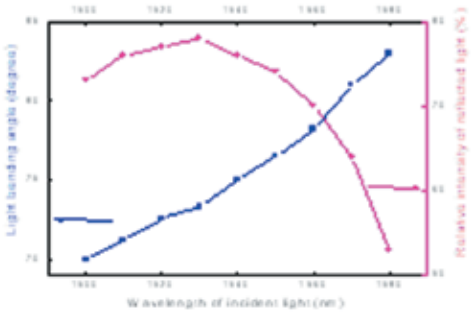

Figure 2: Optical measurement results of the Si grating.

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[1] Hamakawa, Y. (Ed.), Thin-Film Solar Cells, Next Generation Photovoltaics and its Applications, Springer, Berlin; New York , 2004.
[2] Green, M.A., Silicon Solar Cells, Advanced Principles & Practice, University of New South Wales, Sydney, Australia, 1995.

Electrically-Activated Nanocavity Laser Using One-Dimensional Photonic Crystals

E. Mattson, G.S. Petrich, L.A. Kolodziejski, S. Assefa
Sponsorship: NSF-MRSEC

In the future, optical networks may play an expanded role not only in telecommunications, but also in computers and other common electronic devices. These optical networks will require small, on-chip light sources. Using the photonic crystal's ability to strongly confine light, photonic crystal lasers are both very small and efficient, making them ideal for integration into photonic integrated circuits. The laser is very flexible in that simply by changing the active material or by changing the size and spacing of the holes that create the photonic crystal, the emission wavelength can be varied. This laser should be more efficient than current light sources from the standpoints of both the energy and chip design, and should represent a major improvement in on-chip light sources.

The laser consists of two one-dimensional photonic crystal waveguides that cross each other (Figure 1). The laser's nanocavity, which has a length of ~1 μm, is located where the defect regions of the two photonic crystal waveguides overlap. The bottom waveguide consists of an active layer containing InGaAs quantum dots, which emit at 1300nm, sandwiched between two GaAs and AlGaAs layers. Once the photons are generated in the nanocavity, the light will be confined laterally and vertically, by index of refraction changes at the materials' interfaces. However, at the two ends of the waveguide, a series of holes are etched, forming the photonic crystal, which confines the light lengthwise in the nanocavity. Some of the light will leak into the upper InGaAlP waveguide. The upper waveguide exhibits less loss than the lower waveguide and has an asymmetric number of holes etched into it around the nanocavity, allowing the direction of the emitted light to be controlled. The entire photonic crystal part of the laser is about 5 μm square.

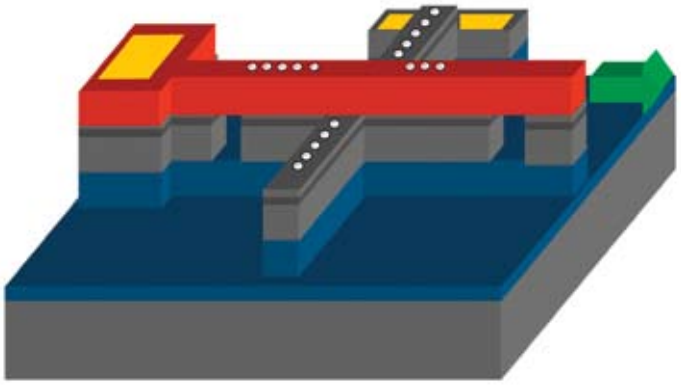

Figure 1: Depiction of the electrically-activated, photonic crystal nanocavity laser. The green arrow represents the direction and location of the emitted light.

Super-Collimation of Light within Photonic Crystal Slabs

S.N. Tandon, M. Dahlem, P. Rakich, M. Ibanescu, M. Soljacic, G.S. Petrich, J.D. Joannopoulos, E.P. Ippen, L.A. Kolodziejski

Sponsorship: NSF-MRSEC

A super-collimator is a device in which light is guided by the dispersion properties of a photonic crystal slab rather than by photonic crystal defects or waveguiding structures. Photonic crystals form the essence of the super-collimation effect. The device, schematically shown in Figure 1, consists of a two-dimensional photonic crystal composed of a square lattice of cylindrical air holes etched into a high-index material. Furthermore, the photonic crystal occupies the entire surface of the super-collimator. The cleaved edges of the super-collimator function as input or output facets. The initial design has focused on realizing super-collimation at a wavelength of 1.44 μm.

Figure 2 shows images of a fabricated super-collimator using a silicon-on-insulator (SOI) wafer. The photonic crystal holes are patterned using interference lithography and are etched into the upper Si layer via reactive ion etching. The left inset of Figure 2 shows the full 1cm x 1cm device with its cleaved input and output facets. The photonic crystal occupies the full sample area and the SEM images at the center and right inset of Figure 2 show the details of the photonic crystal cross-section. The center image also illustrates the large area nature of the photonic crystal. The right inset shows that the air holes are etched through the upper silicon layer. The photonic crystal rests on a buried SiO_2 layer to minimize the coupling to the substrate.

Testing of the super-collimator device is in progress. Preliminary results show that the super-collimation effect is wavelength dependent, with the strongest collimation occurring at a wavelength of 1495 nm. Results also suggest that super-collimation can be sustained within the photonic crystal on millimeter-length scales with very little divergence.

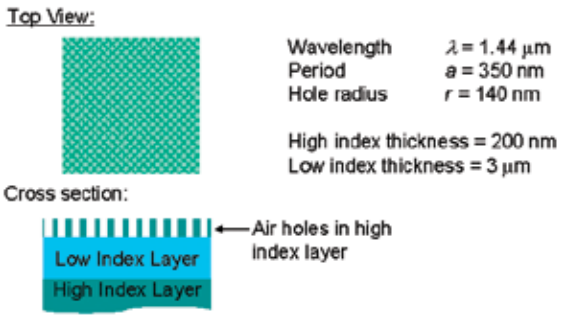

Figure 1: Super-collimator device design showing the top and side views of the device.

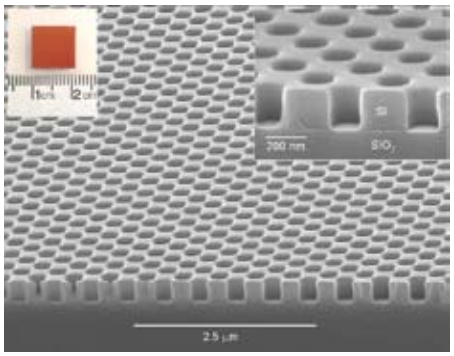

Figure 2: Images of the fabricated super-collimator device. Left inset: Digital photograph showing the full sample. Center: Scanning electron microscope (SEM) image showing the large area nature of the 2D photonic crystal. Right inset: SEM image showing a cross-sectional image of the device fabricated using a SOI wafer.

Diamond-Structured Photonic Crystals

M. Maldovan, E.L. Thomas
Sponsorship: ARO

Certain periodic dielectric structures can prohibit the propagation of light for all directions within a frequency range. These “photonic crystals” allow researchers to modify the interaction between electromagnetic fields and dielectric media, from radio to optical wavelengths. Their technological potential, such as the inhibition of spontaneous emission, enhancement of semiconductor lasers, and integration and miniaturization of optical components, makes the search for an easy-to-craft photonic crystal with a large band-gap a major field of study. This progress article surveys a collection of robust complete three-dimensional dielectric photonic-band-gap structures for the visible and near-infrared regimes, based on the diamond morphology together with their specific fabrication techniques. The basic origin of the complete photonic band-gap for the ”champion” diamond morphology is described in terms of dielectric modulations along principal directions. Progress in three-dimensional interference lithography for fabrication of near-champion diamond-based structures is also discussed.

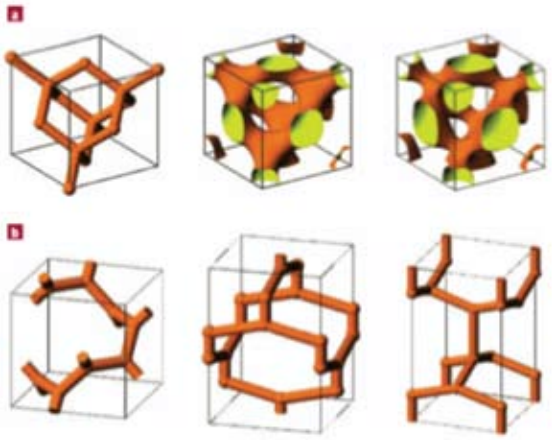

Figure 1: The level-set diamond D and three-connected diamond structures: (a, left): The rod-connected diamond. Center: The level-set diamond-D structure connects neighbor sites of the diamond lattice, producing a continuous dielectric network. This analytical representation allows the fabrication of the diamond morphology through the interference lithography technique; (right): The unbalanced diamond structure connects neighbor sites of the diamond lattice with different weights producing a continuous but unbalanced diamond network. This unique structure presents two simultaneous complete photonic band-[?]gaps for a wide range of volume fractions;(b):3-D representations of the unit cells for the three-connected diamond-like structures. The unit cell ratios are a:a:a, a:a:$\sqrt{2}$a, and a:a:$\sqrt{3}$a, respectively. The maximum gap values are 26.6%, 26.2%, and 22%.The structure on the right has both three- and four-connected nodes [40?].

REFERENCE:

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Photonic Crystals through Holographic Lithography: Simple Cubic, Diamond-like, and Gyroid-like Structures

C.K. Ullal, M. Maldovan, E.L. Thomas, G. Chen,Y.-J. Han, S. Yang
Sponsosrship: AFOSR, ARO

We show how to fabricate three basic photonic crystal structures with simple cubic, fcc, and bcc translational symmetry by interference lithography. The structures are fabricable by the interference of beams launched from the same half space. The simple cubic structure is size-scalable while the structure with fcc translational symmetry possesses two band gaps. Both these structures are experimentally realized.

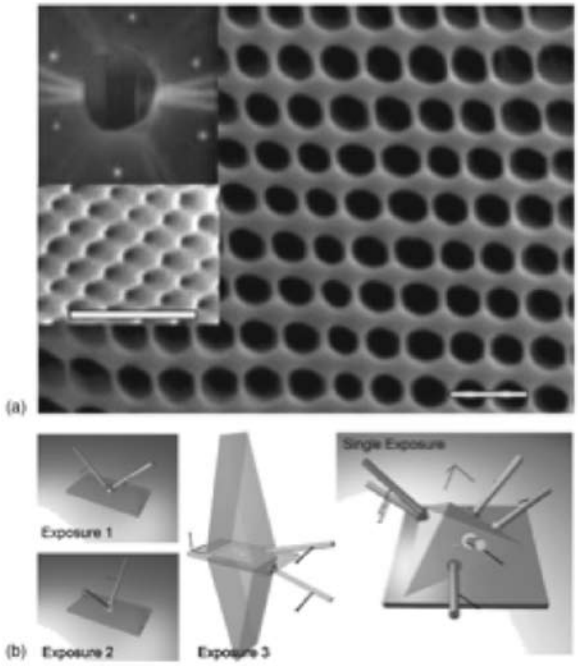

Figure 1: Surface and configuration of P-structure: (a) SEM micrograph of the (100) surface for a P-surface structure, with a periodicity of 1.1 μm. The inset shows a SEM image of a P-surface structure with a periodicity of 0.5 μm, demonstrating size scalability. The inset diffraction pattern comes from another P-surface structure showing the (111) orientation. The scale bars shown are 2 μm. (b) Two possible six-beam configurations for the fabrication of the P-structure. The polarizations are indicated as small arrows on the beams.

REFERENCE:

[1] Ullal, C.K., Maldovan, M., Chen, G., Han, Y-J, Yang, S., Thomas, E.L., "Photonic Crystals through Holographic Lithography: Simple Cubic, Diamond-like, and Gyroid-like Structures", *Applied Physics Letters*, 84, pp. 5434-5436, 2004.

Three-Dimensional Network Photonic Crystals via Cyclic Size Reduction/Infiltration of Sea-Urchin Exoskeleton

Y.-H. Ha, R.A. Vaia, W.F. Lynn, J.P. Constantino, J. Shin, A.B. Smith, P. Matsudaira, E.L. Thomas
Sponsorship: Dupont-MIT Alliance, AFOSR

Many naturally occurring solids possess periodic structures that give rise to visible photonic crystal properties, commonly termed structural colors. Some stunning examples are butterfly wings (one-dimensional, 1-D), abalone shells (1-D), sea mouse spines (two-dimensional, 2-D), and natural opals(three-dimensional, 3-D). Exploitation of other periodic natural structures is, however, limited by the inherently large size scale and the low dielectric contrast of the materials. Furthermore, these generally more complex geometries are a challenge to model correctly in order to obtain correct band diagrams. Here we report the development of a high-fidelity, cyclic, size- reduction and infiltration scheme and apply it to a sea urchin exoskeleton to successfully fabricate a high-dielectric contrast, 3-D photonic crystal exhibiting a stop band in the mid-IR range. The band structure of the exoskeleton is modeled using level set mathematics and agrees well with the experimental reflectivity exhibited by the 3-D bi-continuous tellurium network of the replicated urchin.

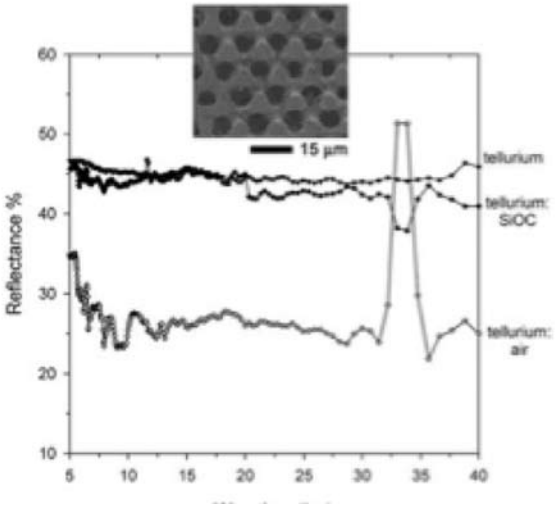

Figure 1: Reflectance spectra θ_i=20° of the bulk tellurium, tellurium: SiOC and tellurium:air replicas. The inset SEM image shows the three-fold symmetric (111) facet of the tellurium:air network after polishing and etching the tellurium:SiOC structure. The reflectivity peak from tellurium: air is centered at 34 µm.

REFERENCE:

[1] Ha, Y.-H., Vaia, R.A., Lynn, W.F., Constantino, J.P., Shin, J., Smith, A.B., Matsudaira, P.T., Thomas, E.L., "Three-Dimensional Network Photonic Crystals via Cyclic Size Reduction/Infiltration of Sea Urchin Exoskeleton", *Advanced Materials*, 16, pp. 1091-1094, 2004.

Layer-by-layer Diamond-like Woodpile Structure with a Large Photonic Band Gap

M. Maldovan, E.L. Thomas, C.Carter
Sponsorship: Singapore-MIT Alliance, U.S. Army

A layer-by-layer, periodic dielectric structure with a large photonic band gap is presented. It consists of a layer-by-layer approximation to the triply periodic bi-continuous level set D surface structure having diamond (FD3m) symmetry. The structure retains the ease of fabrication of the standard woodpile while increasing the maximum quality factor of the gap by 28%. Photonic band gap properties of this structure were calculated using the plane-wave method and its band gap optimized at a fixed index contrast of 3.6.1.

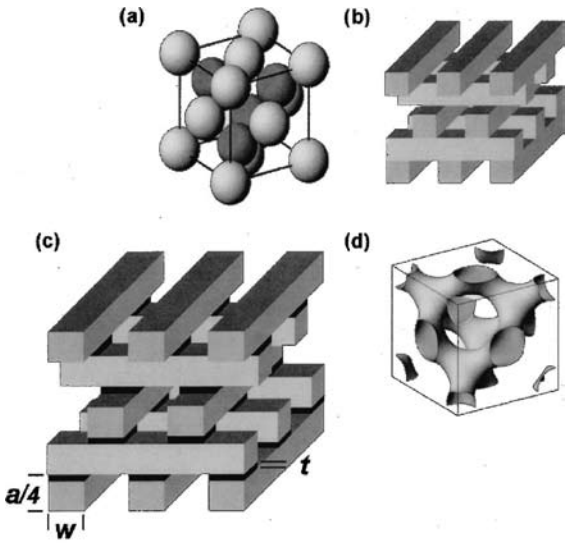

Figure 1: Schematic three-dimensional representation for (a) spheres on a diamond lattice, (b) standard woodpile, (c) diamond-woodpile, and (d) bi-continuous, diamond D level set

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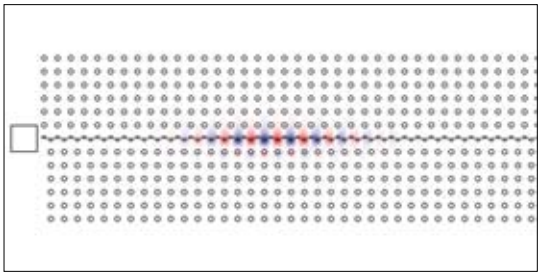
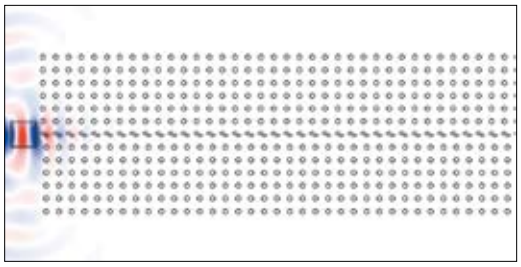
Localized, Guided Propagation Modes in Photonic Crystals with Shear Discontinuities

K. Tian, G. Barbastathis, in collaboration with J. Hong (Jet Propulsion Laboratory)
Sponsorship: Montage Program

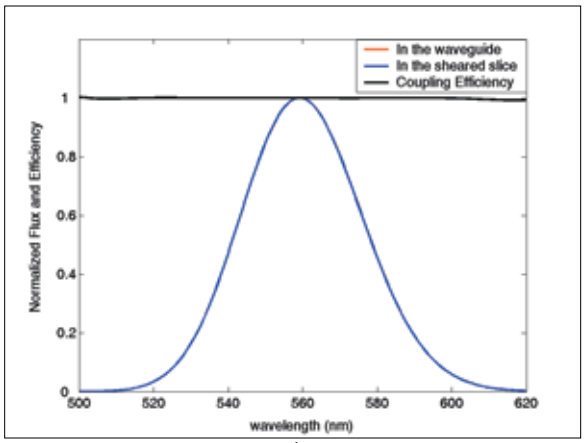
Photonic crystals consist of periodic arrays of dielectric media [1,2]. Electromagnetic waves propagate in photonic crystals as Bloch waves whose coupling gives rise to the band structure, which may include forbidden gaps where the waves cannot propagate. Certain defects can lead to the coupling of energy to confined, localized states in the vicinity of the defect. We propose a new type of defect, consisting of a shear discontinuity in a photonic crystal lattice. Figure 1(a) shows a square lattice of circular dielectric columns with a shear discontinuity in the middle row. The circular dielectric columns in the middle line are cut in half. The shear shift is exactly half the lattice constant. Using FDTD, we simulated a band-limited pulse with its spectrum inside the band gap of the (unperturbed) photonic crystal being injected by the waveguide near the tip of the sheared slice. As Figure 1(a) shows, the entire pulse is well localized to the shear plane as it propagates in the crystal. The confined propagation mode occurs over a broadband spectrum. As Figure 1(c) shows, the coupling efficiency is almost 100% over a long wavelength range, provided that the shear shift is approximately half a lattice constant.



(a)



(b)



(c)

Figure 1. The pulse propagates inside the sheared photonic crystals. The refractive index of basis media is 1.0; that of the circular dielectric columns is 3.0. The diameter of each column is 80nm and the lattice constant is 200nm. The duration of the pulse is 10fs and its center wavelength is 560nm: (a) half-lattice-constant shift; (b) quarter-lattice-constant shift (the confinement is turned off); (c) the spectrum of flux at the exit of the waveguide and in the sheared slice and the couple-in efficiency of (a)

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Nanoelectromechanical Optical Switch for 1550 nm Light

R.E. Bryant, M.L. Povinelli, S.G. Johnson, G.S. Petrich, J.D. Joannopoulos, E.P. Ippen, L.A. Kolodziejski
Sponsorship: NSF-MRSEC

One major objective of optical engineering research is to bring optical systems to the large-scale functionality of electrical systems. Striving to reach this objective, high-index-contrast, planar, evanescently coupled, Nano-Electro-Mechanical (NEM) waveguide switches using the GaAs-based material system are being developed.

The concept that is behind the NEMs switch combines two ideas: high-index-contrast waveguide optics and electromechanical actuation. High-index-contrast waveguide optics can route optical signals via waveguides with sizes of hundreds of nanometers in cross-section. Also, the evanescent method of energy transfer occurs along 100-nanometer coupling lengths and separations. The ability to exploit these length scales leads to a small device footprint, which lends itself to large-scale integrated optics. The physical dimensions of high-index-contrast evanescent coupling provide the impetus for the development of planar opto-electronic NEM systems. Furthermore, due to the size of NEM systems, it is possible to design switches with microsecond response times which would increase the number of potential applications for use by system designers that would not have been possible using the larger Micro-Electro-Mechanical-based switches.

A considerable amount of design and fabrication work has been invested in the development of the NEMS switch. Theoretically, when a voltage is applied to the switch, the two waveguides reduce their separation distance in order to achieve lateral evanescent coupling, which allows 100% of the optical energy to be transferred between the waveguides. In the initial, unbiased state, the initial separation distance prevents lateral coupling. Experimentally, GaAs-based waveguides with release lengths over 30 microns long have been achieved for waveguides that are 1-μm thick and ~300-nm wide, with excellent lateral and horizontal waveguide-to-waveguide alignment. Because the GaAs waveguides typically reside on thermally-oxidized GaAlAs layers, oxidation experiments have been performed to investigate the correlation between the resulting stresses that affect the waveguide at the point where the waveguide becomes suspended to the stoichiometry of the oxidized GaAlAs layer.

MEMS Switching for Integrated Optical Systems, Part (1): Fabrication

S. Takahashi, L. Waller, G. Barbastathis
Sponsorship: DARPA

Ring resonators are optical devices that can act as wavelength-specific add/drop filters, and they have important applications in optical add-drop multiplexers. These resonators can be switched on or off by use of a metal MEMS structure built above the ring resonator and actuated by electrostatic force, as shown in Figure 1. When the metal structure is pulled down to interfere with the evanescent field of the ring waveguides and cause loss, the device will lose its resonance, and hence, the filter will be switched "off." As the structure is freed from the electrostatic force and restored to its natural position above the evanescent field of the ring, the resonator will turn "on" and act normally as a filter. This MEMS structure is easily fabricated by a standard process (Figure 2). We are investigating the use of titanium nitride (TiN) as the material for the MEMS structure. Not only does TiN have appealing mechanical properties (e.g. high modulus-to-density ratio, high yield stress) and electrical conductivity, but a large body of knowledge also exists concerning its micro-fabrication techniques due to its wide use in CMOS fabrication, i.e., for diffusion barriers and local interconnects[1]. Therefore, TiN has high potential as a MEMS/NEMS structural material, especially for those applications that require electrostatic actuation of beams, bridges, etc.

One major problem in designing and fabricating this device is the residual stress of the MEMS structure, which could essentially deflect the beam vertically and allow the conductive structure to interfere with the evanescent field in the "on" state. Appropriately controlling the deposition parameters or annealing the material before its release from the sacrificial layer can control residual stress. Previous studies have shown that annealing of TiN by heating to 500°C and cooling back to room temperature at a rate of 2°C per minute can induce a significant reduction of stress in a TiN membrane. This MEMS switching device has a broad range of application in micro and nano-photonics, where the device can operate in the same fashion to interfere with the evanescent field of guided light, such as in photonic-crystal-based and plasmon-optics-based devices.

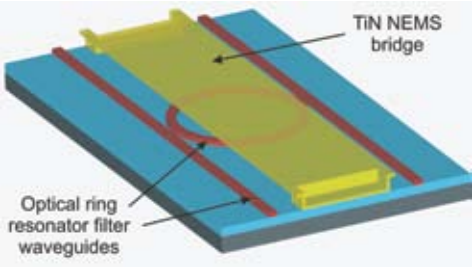

Figure 1: Schematic of the MEMS ring resonator filter switch.

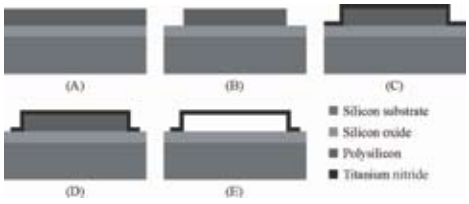

Figure 2: Fabrication process of the MEMS structure

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[1] Plummer, J.D., M. D. Deal, P. B. Griffin, *Silicon VLSI Technology*, Upper Saddle River, New Jersey: Prentice Hall, 2000.

MEMS Switching for Integrated Optical Systems, Part (2): Instrumentation and Control

L. Waller, S. Takahashi, G. Barbastathis
Sponsorship: DARPA

We have shown that wavelength-selective, integrated optical switches controlled via MEMS-actuation can be fabricated and operated. These devices have potential uses in optical networking, optical sampling, and RF- MEMS switching. However, practical application of these switches requires tuning of the dropped wavelength. To achieve this, we can use a dielectric MEMS bridge and control it in an analog fashion. If the dielectric bridge is moved vertically within the evanescent field of the ring resonator, the optical path length of the resonator, and thus the wavelength selected by the ring resonator, shift. In order to achieve tuning over one full wavelength channel of 30nm, we must control the MEMS bridge with a positional accuracy better than 0.7Å. Noise models for the device and control have been developed to predict the system noise, and a capacitive sensing feedback circuit is being designed to meet specifications (Figure 1). Capacitive sensing is a highly accurate, easily implemented feedback method that has shown to be useful in micro devices. The MEMS dielectric bridge can act as one electrode of a three-electrode capacitive sensor (Figure 1), in which a sensing signal and a control signal are applied to the outer two electrodes in order to displace the dielectric bridge to the desired height. Figure 2 also shows the response of this system to a two-pulse input. The device's performance can be measured, both temporally and spectrall,y using a lensed fiber to couple into and out of the integrated waveguides.

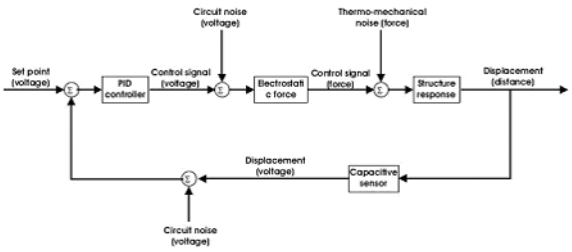

Figure 1: Flow chart for system model.

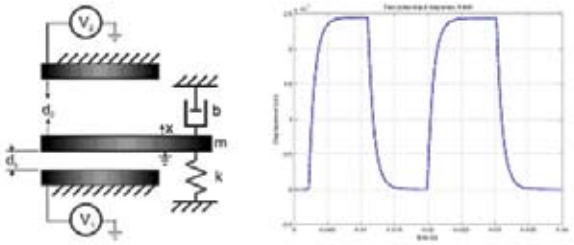

Figure 2: Three-electrode model and its [it's = it is]system response to pulses.

Techniques for Coupled Optimization and Simulation

K.C. Sou, J.H. Lee, J. Bardhan, L. Daniel, A. Megretski, Y. Avniel, S. Johnson, J. White
Sponsorship: MARCO IFC and GSRC, DARPA

The enormous advances in both interior-point-based, convex optimization and fast methods for three-dimensional simulation are making development of design tools that perform automatic structural optimization much more feasible. We are developing strategies for coupling fast simulation and interior-point optimization for applications such as: biomolecule design, nanophotonics, and optical semiconductor process inspection. Our approaches include using Hession-implicit methods in which the simulation and optimization occur in parallel [1] and strategies in which a detailed simulation model is used to generate a parameterized reduced order model [2,3,4]

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[2] Daniel, L. and J. White, "Numerical Techniques for Extracting Geometrically Parameterized Reduced Order Interconnect Models from Full-wave Electromagnetic Analysis," Proceedings of the IEEE AP-S International Symposium and USNC / URSI National Radio Science Meeting, June, 2004.

[3] Lee, J.H., D. Vasilyev, A. Vithayathil, L. Daniel, and J. White, "Accelerated Optical Topography Inspection using Parameterized Model Order Reduction," forthcoming, Proceedings of the IEEE International Microwave Symposium, June, 2005.

[4] Klemas, T., L. Daniel, and J. White, "Segregation by Primary Phase Factors: A Full-wave Algorithm for Model Orderreduction," forthcoming, Proceedings of the Design Automation Conference, Anaheim, CA, 2005.

Tools for Photonics in Integrated Circuit Design and Manufacturing

J.H. Lee, Y. Avniel, S. Johnson, J. White
Sponsorship: MARCO IFC, DARPA, NSF

Optical inspection, now the non-destructive, semiconductor process monitoring technique of choice, requires the solution of an inverse scattering problem to infer geometry from measured light. We have developed a new approach to accelerating this inverse scattering problem based on using parameterized model reduction [1]. The problem of analyzing optical effects in wavelength-sized structures also arises for developers of integrated nanophotonics, which is emerging as an important new technology. Nanophotonic designers have very few available tools, and we are beginning a project to improve the situation. We are developing approaches that can be used to extract circuit-level models of photonic devices [2,3] and are also developing new techniques for assessing the impact of roughness on the loss in photonic channels [4].

REFERENCES:

[1] Lee, J.H., D. Vasilyev, A. Vithayathil, L. Daniel, and J. White, "Accelerated Optical Topography Inspection Using Parameterizedmodel-order Reduction," forthcoming, Proceedings of the IEEE International Microwave Symposium, June, 2005.

[2] Klemas, T., L. Daniel, and J. White, "Segregation by Primary Phase Factors: A Full-wave Algorithm For Model-order Reduction" forthcoming, Proceedings of the Design Automation Conference, Anaheim, CA, 2005.

[3] Klemas, T., L. Daniel, and J. White, "A Fast Full-wave Algorithm to Generate Low-order Electromagnetic Scattering Models," forthcoming International Symposium on Antennas and Propagation and USNC/URSI National Radio Science Meeting, Washington, DC, July, 2005.

[4] Zhu, Z., A. Demir, and J. White, "A Stochastic Integral Equation Method for Modeling the Rough Surface Effect on" Proceedings of the IEEE Conference on Computer-Aided Design, San Jose, November 2004.

Photonic Integrated Circuits for Ultrafast Optical Logic

A. Markina, R.D. Williams, G.S. Petrich, R. Ram, L.A. Kolodziejski
Sponsorship: DARPA

The aim of this project is to model and to produce a modular, monolithically integrated, all-optical logic unit cell capable of performing a complete set of Boolean operations at speeds of hundreds of gigabits per second. The basic structure consists of a balanced Mach-Zehnder interferometer with an (In,Ga)(As,P)-based semiconductor optical amplifier (SOA) in each arm, as shown schematically in Figure 1.

Modeling is used to develop the design rules, to identify tradeoffs, to determine fabrication tolerances, and to estimate the effects of imperfections in semiconductor processing on the device's performance. Beam propagation method simulations are used to model passive waveguides, multimode interference couplers, and asymmetric twin-waveguide structures. Finite-difference, time-domain simulations are used to estimate the reflections between the various components. Custom MATLAB scripts are being developed to assess tradeoffs in SOA performance and to work toward design rules that specifically address the design of the SOAs for switching applications. The challenge is to optimize the performance of each component even when all of the components are monolithically integrated on a photonic integrated circuit.

Fabrication processes are being developed to create the all-optical logic unit cell. The waveguide design calls for vertical integration of the passive waveguide and active elements. This integration is achieved by employing a taper coupler to transfer the optical mode between the lower passive waveguide and the upper active waveguide of the twin-waveguide structure. In addition to the optical logic unit cell, isolated components are being fabricated and tested to confirm the device design and the computer simulation results.

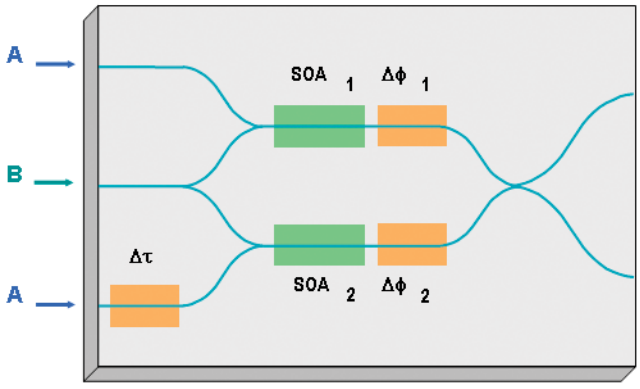

Figure 1: The optical logic unit cell. A balanced Mach-Zenhder interferometer composed of SOAs, multimode interference couplers, phase shifters and a time delay element.

Variation Analysis in Optical Interconnect

K. Balakrishnan, S. Staker, D. Boning
Sponsorship: MARCO IFC

The continual scaling of CMOS technology causes an increase in the amounts of systematic and random variation in circuits. Variation is also a concern in alternative optical interconnect approaches. In particular, both passive and active optical components can be affected by different sources of variation. In passive components such as waveguides and splitters, one source of variability tends to be of a geometric nature, causing uneven splitting ratios and overall transmission losses. For example, blurring across waveguide corners and bends can result in transmission losses. The sidewall roughness of a wave-guiding structure itself also contributes to non-negligible losses when a light source must travel a long distance from one end of a chip to another. In addition, temperature gradients within the chip as well as variation in the operating temperature of a chip can cause refractive index variations throughout these passive optical components. Current work being done in this area involves the analysis of effective-refractive-index variations on the transmission and splitting ratios of different splitter structures. These waveguide-splitter structures are as follows: High Transmission Cavity (HTC) splitter [1], Star-coupler design [2], and Uniform Bending Radius design [3]. Preliminary results have shown a sub-linear relationship between the refractive index variation and splitting losses for the HTC splitter. Figure 1 shows an example of an HTC splitter test structure, with the difference in color/shading representing the refractive index variations in the waveguide. Figure 2 illustrates results of both splitting ratio and transmission power as functions of index variation. Further work will examine other possible waveguide-splitting structures as well as analyze the effects of sidewall roughness caused by lithographic uncertainties on the robustness of wave-guiding structures.

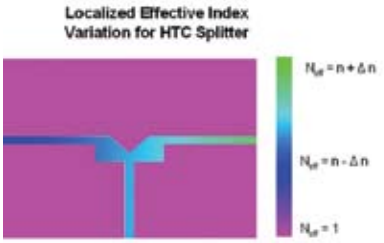

Figure 1: Example HTC splitter test structure with a horizontal refractive-index gradient.

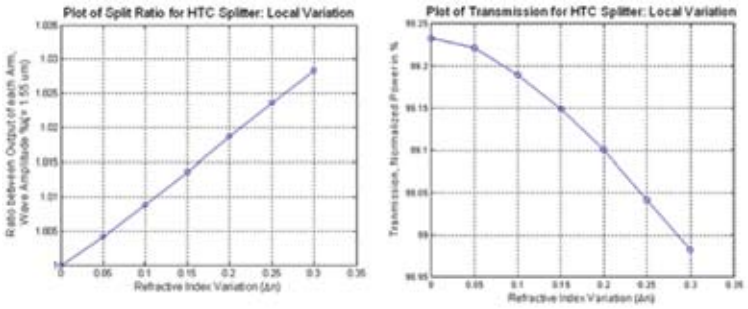

Figure 2: Simulation results of splitting ratio and transmission power versus refractive-index variation.

REFERENCES:

[1] Manolatou, C., S.G. Johnson, S. Fan, P.R. Villeneuve, H.A. Haus, J.D. Joannopoulos, "High-Density Integrated Optics," *J. Lightwave Tech.,* 17(9) September 1999.

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[3] Zheng, J.-F., F.H. Robertson, E. Mohammed, I. Young, D. Ahn, K. Wada, J. Michel, L.C. Kimerling, "On-chip Optical Clock Signal Distribution," *Optical Society of America.* 4(4), 254-258, 2003.

Trimming of Microring Resonators

D.K. Sparacin, J.P. Lock, C. Hong, K.K. Gleason, L.C. Kimerling, J. Michel
Sponsorship: NSF MRSEC, ISN

Microring resonators are basic building blocks of photonic circuits, enabling complex functionality for optical systems. However, as micro-ring resonator diameters shrink to less than 10 μm, non-deterministic pattern-transfer errors limit dimensional precision and preclude the fabrication of identical devices across an entire wafer. Thus, the ability to precisely trim microring resonators becomes increasingly important. Microring trimming is typically done by thermal methods, where a heater, integrated onto the microphotonic chip, modifies the effective index and thus the resonance condition of the ring. This architecture adds several fabrication steps, limits the density of devices to maintain thermal isolation, and requires significant power consumption to keep the rings "trimmed". Alternatively, we use an organo-silicon polymer film as a cladding material, in which the refractive index is adjusted via photo-oxidation when irradiated with ultraviolet light (Figure 1). Photo-oxidation decreases the refractive index of PECVD 6M2S by nearly 4%, from n=1.52 to n=1.46, enabling large resonance shifts that are not feasible with thermal trimming techniques. In this work, Si_3N_4 (n=2.2) waveguides, designed for single mode operation at λ = 1550 nm, were fabricated from a 0.4-μm Si_3N_4 film deposited onto a 3-μm oxide under-cladding layer on (100) Si. The Si_3N_4 was patterned using a polysilicon hard mask and 365-nm photolithography. The micro-rings have a diameter of 100μm and the Si_3N_4 waveguides have cross-sectional dimensions of 400 x 750 nm^2. Afterwards, an organo-silicon top cladding layer was deposited directly onto the ring resonator devices using a PECVD process [1]. Spectral characterization of the microrings was done at the ring's through-port in both TE and TM polarizations by a C+L band, JDS Uniphase swept wavelength system (tunable laser and broadband photodetector) used in conjunction with a Newport Auto-Align System. Resonance shifts (Figure 2) from the Si3N4 rings were as large as 12.8 nm for the TE mode and 23.5 nm for the TM mode. Experimental results were compared with shifts predicted by theory. As a quick, localized, and controllable technique to produce large and precise resonance shifts, photo-oxidation trimming provides an attractive alternative to conventional trimming techniques.

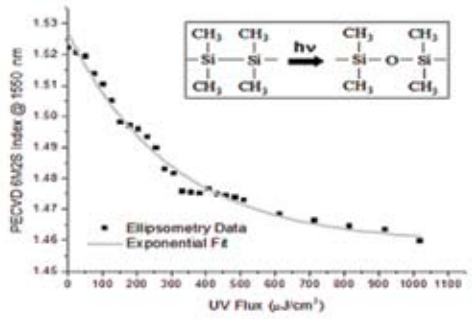

Figure 1: The refractive index of PECVD 6M2S cladding material decreases with UV irradiation as a result of photo-oxidation. The inset depicts the photo-oxidation reaction.

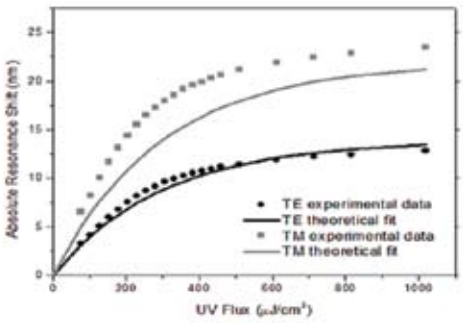

Figure 2: The experimental resonance shifts for TE and TM polarizations are compared with modeled results.

REFERENCE

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Optical Gain Media

L. Dal Negro, M. Stolfi, J. Michel, X. Duan, S. Saini, L.C. Kimerling, J. LeBlanc, J. Haavisto
Sponsorship: Charles Stark Draper Laboratories

The recent discovery of efficient energy-transfer between silicon nanocrystals (Si-nc's) and erbium (Er) ions has initiated an entirely new approach that profits from the advantages of quantum size effects and silicon (Si) rare earth doping, promising a route towards the integration of CMOS technology with 1.54-μm light sources. Despite several exciting breakthroughs, the nucleation of efficient light-emitting Si-nc generally requires annealing temperatures in excess of 1000 °C, severely limiting CMOS-compatibility. However, very recently Franzò [1] et al. demonstrated that Er-sensitization can occur at temperatures as low as 800°C, stimulating a debate on the ultimate nature of the energy transfer process.

We have recently fabricated erbium-doped, silicon-rich SiO_2 (Er:SRO) slab waveguides on Si substrates by reactive, radio-frequency (RF) magnetron-sputtering followed by thermal annealing. By studying Er emission versus Er:SRO annealing temperature, we found that the emission intensity is maximized between 600°C and 700°C for a Si content of 38% at. For samples annealed at 600°C, we are currently investigating the presence of light amplification and optical gain through variable stripe length (VSL) measurements.

These Er:SRO films can be used for the fabrication of compact waveguide optical amplifiers and integrated light sources with full CMOS-compatibility.

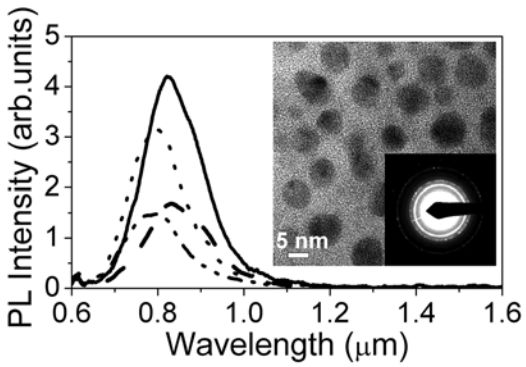

Figure 1: Room temperature PL spectra of Si-nc in SiO_2 samples without Er with different silicon content annealed at 1100 °C for 1 hour in a N_2 atmosphere. The Si contents for the samples are: 34 at% (dash-dot line), 35 at% (dotted line), 38 at% (solid line) and 43 at% (dash line). (inset) Plan-view TEM image and electron diffraction pattern for the Si-nc sample with 38 at% Si. [2]

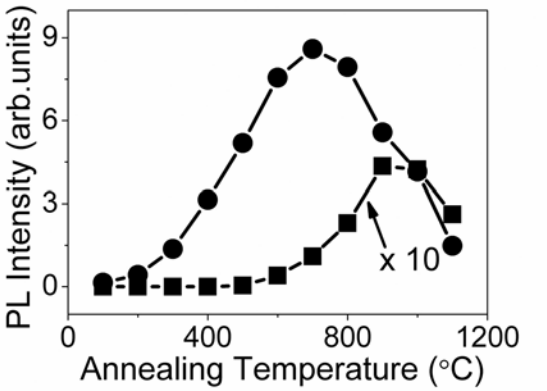

Figure 2: Room-temperature Er emission versus annealing temperature for Er in SiO_2 containing Si-nc samples with 38 at% Si and Er concentration of 8.2×10^{19} cm^{-3} (circles) and Er in SiO_2 samples with Er concentration of 9×10^{19} cm^{-3} (squares, magnified by 10). [2]

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[2] Stolfi, M., L. Dal Negro, J. Michel, X. Duan, J. LeBlanc, J. Haavisto, and L.C. Kimerling, *MRS Proceedings*, 832 F11.8 2005.

Silicon Waveguide Structures

D.K. Sparacin, S.J. Spector, L.C. Kimerling
Sponsorship: NSF-MRSEC

The silicon/silicon-dioxide materials platform (Si-SiO_2) is ideal for microphotonics due its high index of refraction difference between the waveguide core and cladding (Δn), CMOS-fabrication compatibility, and process knowledge-base. Additionally, the Si-SiO_2 system allows for optoelectronic functionality, unlike other competing high Δn, dielectric-based, CMOS-compatible, materials systems. While the properties of the Si-SiO_2 system are attractive, they are not fully realized when waveguides are fabricated. For silicon waveguides, nm-scale sidewall roughness is the prime cause of transmission loss and an impediment to use. Oxidation of rough silicon surfaces is an effective method of smoothing silicon and can enable high transmission waveguides. However, oxidation smoothing is typically performed by high-temperature annealing in an oxygen-rich environment. This process works well for smoothing silicon waveguide surfaces but lacks control in maintaining cross-sectional waveguide dimensions due to the large consumption of silicon during the oxidation process. In efforts to solve these deficiencies associated with oxidation smoothing, we developed a new, more efficient silicon waveguide sidewall smoothing process using wet chemical oxidation. In this work we used a post-etch, multi-stepped approach for efficient smoothing (in terms of roughness amplitude reduction to material consumption) of patterned SOI waveguides. Wet chemical oxidation reduces waveguide transmission loss without sacrificing dimensional integrity or thermal budget. The use of common chemical oxidants, such as those used in wafer-cleaning processes, is ideal for this oxidation-smoothing technique. Transmission loss data was determined by the Fabry-Perot technique. As shown in Figure 1, the transmission loss is reduced, when compared to the as-fabricated data, for the different wet chemistries. The effect is strongest for the thinnest waveguides, where transmission loss is most sensitive to sidewall roughness. In this proof of concept work, we have reduced Si waveguide sidewall loss from 9.2 to 1.9 dB/cm.

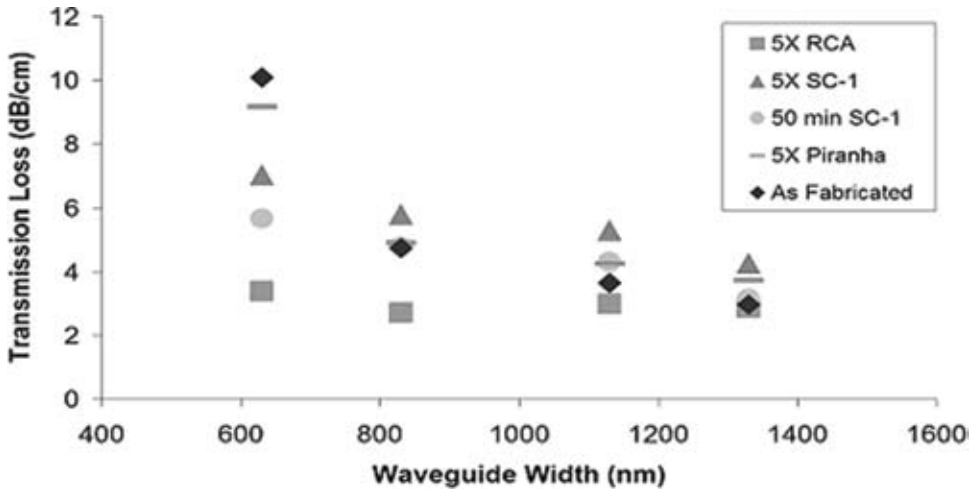

Figure 1: Transmission loss versus silicon waveguide width for various wet chemical oxidations. Measurement error bars for each data point (±1 dB/cm) have been omitted for clarity. The waveguide height is 220 nm.

Sputtered Silicon Oxynitride for Silicon Microphotonics

J.G. Sandland, A. Eshed, S. Akiyama, S. Saini, V. Nguyen, L.C. Kimerling
Sponsorship: NSF-MRSEC

Silicon oxynitride (SiON) is an ideal microphotonics waveguide material providing tunable control in composition nd refractive indices. SiON can be varied in refractive index from silicon dioxide values (n=1.46) to silicon-rich silicon nitride values (n~2.3) (Figure 1). This flexibility in refractive index enables optimization of the device's performance by executing trade-offs between the advantages of low-index contrast systems (low scattering loss and easy fiber-to-waveguide coupling) and high-index-contrast systems (small waveguide size and tight bending radii).

Sputter-processing has been investigated as a thin-film deposition alternative to traditional CVD-processing. Two room-temperature SiON sputter processes have been explored: co-sputtering of silicon oxide and silicon nitride targets and reactive sputtering from a silicon nitride target in an oxygen ambient environment. Process models were created and validated to predict refractive index and composition in both the reactive and co-sputtered depositions. Co-sputtered deposition was found to follow a mixture model, while reactive-sputter deposition was found to be either Si-flux limited or O-flux limited, depending on the partial pressure of oxygen in the reaction chamber and the power applied to the silicon nitride target (Figure 2). A study of materials composition, using SIMS showed sputtered SiON to be a homogeneous material with accurate control of refractive index. Reactively sputtered SiON was found to be Si-rich.

These sputtered materials were investigated for use as passive waveguides and active erbium-doped (Er) waveguide amplifiers. Losses below 1 dB/cm were observed for co-sputtered deposition (n=1.65) waveguides. Photoluminescence studies of Er-doped material showed lifetimes comparable to commercial EDFA material for both co-sputtered SiON and sputtered silicon dioxide. Dangling bonds from silicon were found to contribute both to waveguide-transmission loss and to non-radiative de-excitation in Er-doped materials.

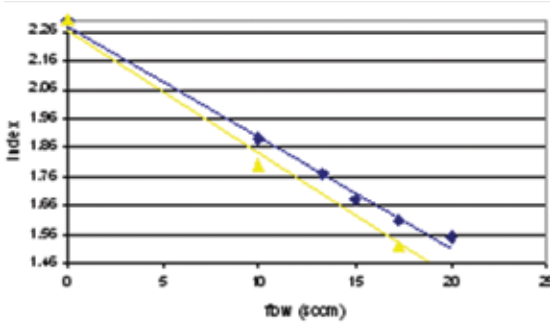

Figure 1: Theoretical prediction and experimental measurement of refractive index versus gas flow rate (10% O_2 in Ar) at 400W and 500W biased silicon nitride target power. (▲= 500 W, ◊ = 400W)

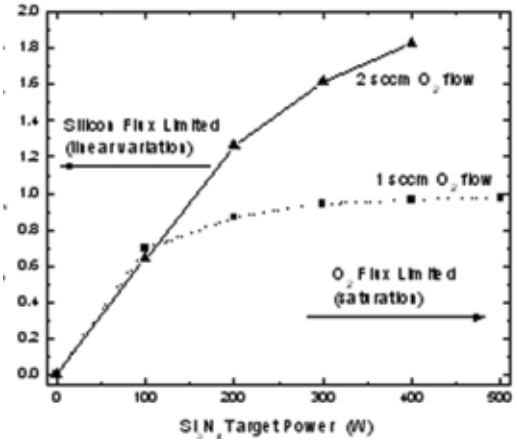

Figure 2: Gettered oxygen content versus silicon nitride target power, for 1 sccm and 2 sccm of O_2 gas flow. At high powers, the gettering rate of oxygen into the depositing film saturates, making the SiON film compositions easily tunable by adjustment of the O_2-flow rate. Solid lines are provided to guide the eye.

Modulators

S. Jongthammanurak, J. Liu, C-Y. Hong, J. Michel, K. Wada, D. Pan, L.C. Kimerling
Sponsorship: Pirelli Labs

Silicon microphotonics has drawn great interest for use in high-capacity data transfer using lightwave based technology. The Giga bit-per-second capacity data transfer in planar structures enables solutions for interconnects delay in computers. The wavelengths used in silicon microphotonics of 1.3 and 1.55 μm enable the telecommunication applications such as Local Area Networks (LANs) and fiber-to-the-Home (FTTH). Compatibility with existing complementary metal-oxide-semiconductor (CMOS) technology provides processing capability and enables the integration between microphotonics and silicon-based microelectronics.

Silicon-based optical modulators are crucial components that manipulate optical signals in the integrated microphotonics. At present, carrier related effect limits the speed of silicon-based modulators to only Gigahertz. High-speed application (> 10GHz) requires modulation based on field effect. In this work, we study the field-effect based absorption modulation in pure germanium and germanium-rich silicon-germanium epitaxial films. Using spectral responsivity measurement, we relate the material absorption coefficients to spectral responsivity.

We observed the electro-absorption effect in germanium p-i-n diodes. For the energy lower than the bandgap (0.79 eV), the spectral responsivity is enhanced by the applied field. Above the band gap, we observed the Franz-Keldysh oscillation in spectral responsivity. This oscillation is due to band structure perturbation from the electric field. In Ge-rich, SiGe p-i-n diodes, we observed decreasing material absorption between direct and indirect band edges under the applied field using spectral responsivity by a laser source. The cause of this effect is being investigated. These materials are potential candidates for using as field-effect-based optical modulators in silicon microphotonics.

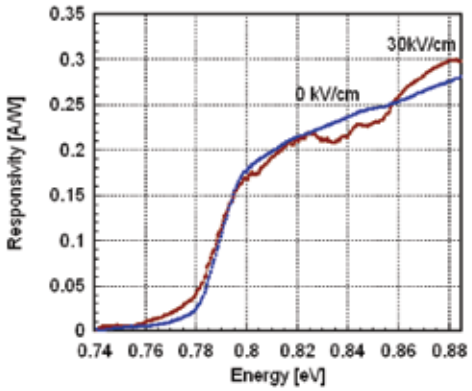

Figure 1: Spectral responsivity from Ge p-i-n diodes under 0 kV/cm and 30kV/cm.

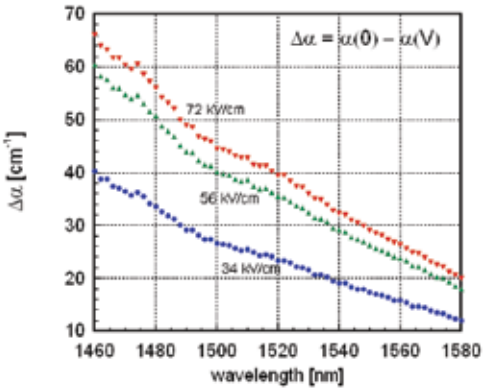

Figure 2 : Differences in Ge-rich SiGe absorption coefficients under the applied fields.

Fiber-Waveguide Coupling for HIC

V. Nguyen, T. Montalbo, C. Manolatou, A. Agarwal, J. Michel, L.C. Kimerling
Sponsorship: Analog Devices, Inc.

Integrated optical circuit designs seek to incorporate several optical functions on a single semiconductor chip. However, there is a need to couple signals from optical fibers to the on-chip waveguides and vice versa. Direct coupling results in high power-loss from three sources: reflections due to the difference in refractive index of the core materials, a mode-size mismatch between fiber and waveguide, and a mode-shape mismatch between a fiber's circular and waveguide's elliptical mode fields.

In this work, we explore an on-chip coupler to transform light from a single-mode optical fiber to a single-mode waveguide fabricated entirely by CMOS-compatible processes in MTL. In the vertical direction, the fiber mode diameter is reduced by a stack of varying refractive index layers formed on a cladding layer [1]. The layers, silicon oxynitride deposited by plasma enhanced chemical vapor deposition (PECVD), gradually increase in refractive index from top to the lower waveguide layer on oxide cladding on a silicon substrate. The lateral mode field conversion is completed with a linear taper and lens at the input facet [1, 2]. Both the lens and the tapered shape of the stack are defined through plasma etching.

The efficiency of the above fiber-to-waveguide coupling scheme has been measured and plotted as function of coupler length, input lens radius, and widths of input and output facets. The results are to supplement and correct the theoretical simulations of such structures with beam propagation (BPM) and finite-difference, time-domain (FDTD) methods.

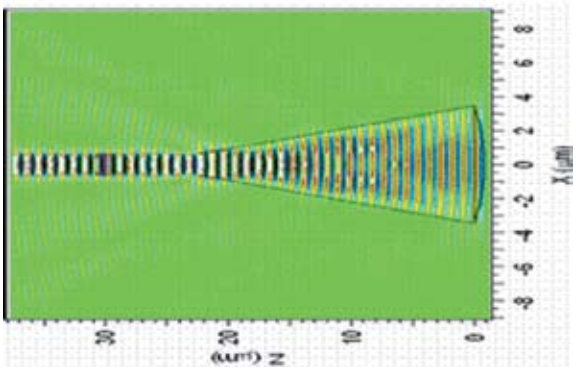

Figure 1: An FDTD simulation shows power--mode conversion to waveguide with a lens and taper combination.

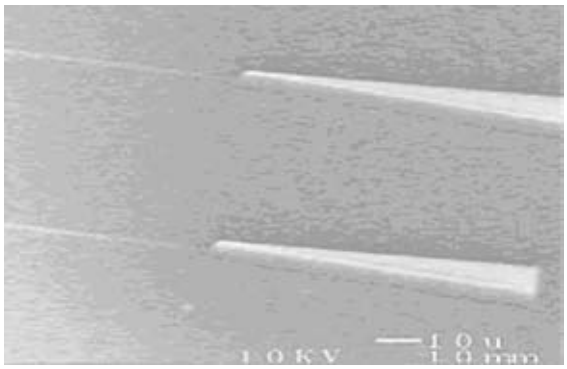

Figure 2: SEM shows 2 fabricated SiON--coupler structures on silicon.

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[1] Manolatou, C., "Passive Components for Dense Optical Integration Based on High Index Contrast" *[dissertation]* Cambridge (MA): MIT, 2001, pp 127-150 of 182. [Available from: Barker Libraries Microforms, MIT, Cambridge (MA); Thesis E.E. 2001 PhD]

[2] Montalbo, T., "Fiber to Waveguide Coupler for Silicon Photonics" *[dissertation]* Cambridge (MA): MIT, 2004, pp 39-52 of 82. [Available from: Barker Libraries Microforms, MIT, Cambridge (MA); Thesis DMSE 2004 MS]

Novel Waveguide Electro-absorption Modulators for Optical Interconnects Utilizing an Insulator/Semiconductor/Insulator Structure

C.L. Dohrman, S. Gupta, R.J. Ram, E.A. Fitzgerald
Sponsorship: MARCO IFC, BAE

We are developing a novel microphotonic device to modulate light intensity in waveguides and photonic integrated circuits. The device is a type of electro-absorption modulator that uses the well-known quantum-confined Stark effect, which causes the absorption spectrum of an ultra-thin semiconductor layer to shift to lower energies with the application of an electric field. The device differs from existing electro-absorption modulators in two important ways. First, it uses an insulator/active, region/insulator structure instead of the semiconductor/quantum well/semiconductor structure used in existing electro-absorption modulators (Figure 1). Second, it uses an amorphous, nanocrystalline, or monocrystalline wafer-bonded quantum-confined active region instead of the epitaxially deposited quantum-confined active region used in existing devices. In addition, we have discovered four methods to suppress absorption saturation and voltage screening in our new device. This suppression is accomplished by decreasing the recombination lifetime of electron-hole pairs in the active region by (i) decreasing the thickness of the active region to prevent charge separation and to increase the ratio of interface to active volume, (ii) increasing the concentration of interface states at the interface of the quantum well and insulator by modifying the cladding material, (iii) adding to the active region of impurities (such as gold) that act as recombination centers , or (iv) adding to the active region of network modifiers (such as nitrogen) that increase the concentration of dangling bonds.

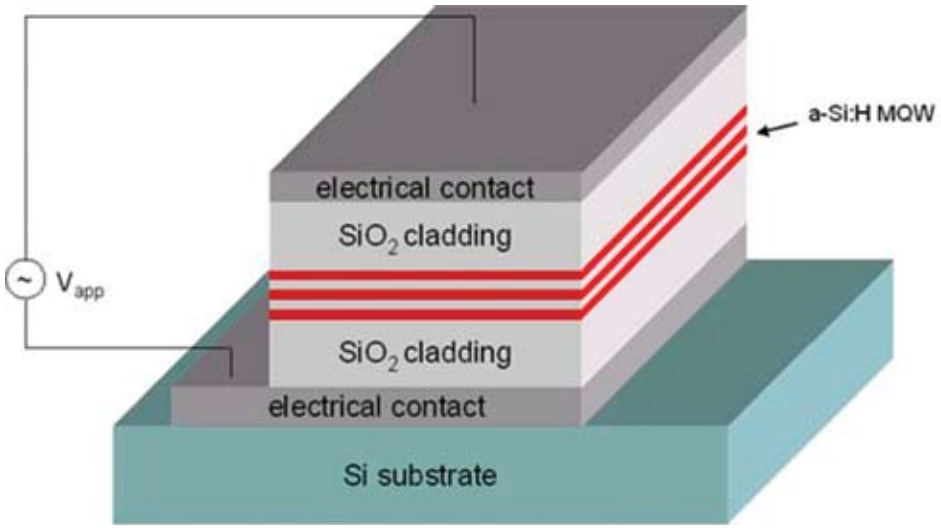

Figure 1: Schematic of insulator/semiconductor/insulator structure of electro-absorption modulator under development.

Faraday Rotation in Semiconductors for Photonic Integration

T. Zaman, X. Guo, R.J. Ram
Sponsorship: DARPA

The demonstration of waveguide isolators and circulators that can easily be integrated with active and passive optical components is essential to large-scale photonic integration. Indium Phophide (InP) is a widely used substrate for photonic components. Thus an InP-based waveguide isolator will provide the possibility for large-scale photonic integration. Iron (Fe)-doped InP with an Fe concentration of 2.9 x 10^{16} cm^{-3} was measured for its Faraday effect. At 1550 nm, the Verdet coefficient is 23.8 °/cm/T and the absorption coefficient is 0.20 cm^{-1}. The result shows that achieving isolation in acceptable length waveguides (~500um) is possible with improved Fe-doping concentration (~ 10^{18} cm^{-3}).

In order to rotate the polarization state of light within a waveguide, the Faraday material must be incorporated within a zero-birefringence waveguide. High-index contrast waveguides where the geometric birefringence is eliminated, have been demonstrated [1-2]. Deeply etched InP waveguides, as shown in Figure 2, with zero-birefringence and low optical loss have been demonstrated. In summary, the most significant materials challenges have been overcome for the realization of fully integrated waveguide optical isolators.

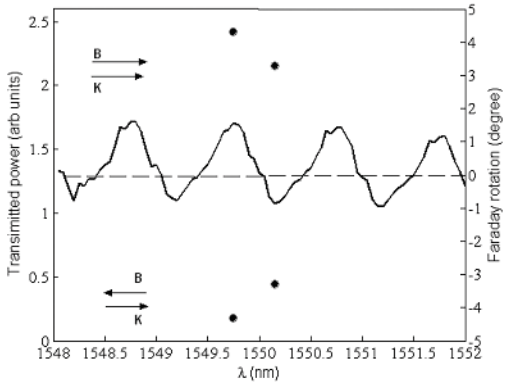

Figure 1: The dots indicate the rotation angle for linear polarization upon transmission through a InP/InGaAsP/InP resonator with an Fe concentration of 1x10^{17} cm^{-3} grown on a 300-μm InP substrate with an Fe concentration of 1x10^{16} cm^{-3}. For reference, the power transmission spectrum is also shown.

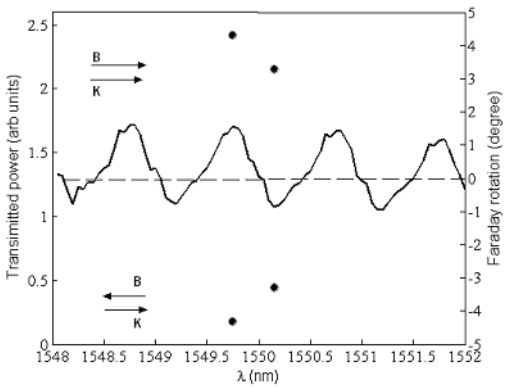

Figure 2: Waveguide width vs. wavelength to achieve zero birefringence.

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[1] Wolfe, R., J. Hegarty, J. F. Dillon, Jr., L.C. Luther, G.K. Celler, L. E. Trimble, and C. S. Dorsey, "Thin-film Waveguide Magneto-optic Isolator," *Appl. Phys. Lett.,* 46(9), pp. 817-819. 1985.

[2] Watts, M.R., S. G. Johnson, H. A. Haus, and J.D. Joannopoulos, *Opt. Lett.* 27(20), pp. 1785-1787, 2002.

Slice-and-cascade Simulation of 3-D Optical Systems

Z. Xu, G. Barbastathis, in collaboration with M.A. Neifeld (University of Arizona)
Sponsorship: Laboratory of 3D Optical Systems

Understanding the Bragg selectivity requires getting an accurate prediction of the diffraction field of a volume hologram. So far, several methods have been introduced to analyze the diffraction property of volume hologram. One popular method is the Coupled Wave Theory (CWT), which was first applied to holography by Kogelnik. His classic paper presents an elegant expression of the diffraction efficiency by considering coupling of the 0^{th} and 1^{st} diffraction orders. The drawback of CWT is the limitation for complicated fringe shapes. An alternative is the so-called Born approximation theory. Though this method gives an analytic result for the diffraction field and can be applied to arbitrary geometry of hologram, it is valid only under the first-order approximation which means weak refractive index modulation.

In 3-D imaging systems, we usually utilize the spherical wave-recorded holographic element and pursue a maximum efficiency. This requires us to choose the hologram with complicated geometry and strong modulation. To model and optimize such holograms, we have developed a novel numerical method called slice-and-cascade simulation for the problem of diffracting volume holograpic. The idea is to decompose the thick element into slices and calculate the propagation slice by slice. Intuitively, we can think the propagation in one slice as following: firstly light is translating in a homogeneous space and then is modulated by a phase grating. Also, based on this assumption, we can get a recursive relation of the fields between two adjacent slices.

Figures 1 and 2 show a very good agreement of our method with the CWT, verifying that the method works well in the well-known plane-wave hologram case. We are currently in the process of extending the slice-and-cascade method to the more complicated geometry of interest, and we are optimizing our system design.

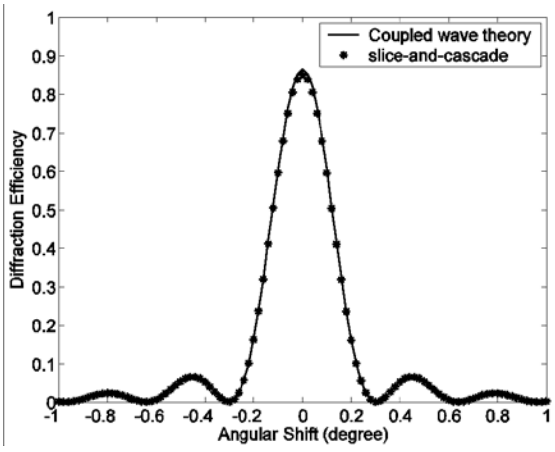


Figure 1: comparison of slice-and-cascade method with CWT as angular selectivity for plane-to-plane volume hologram

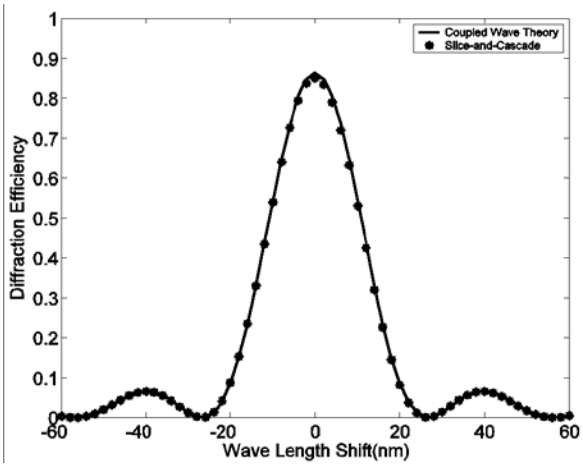
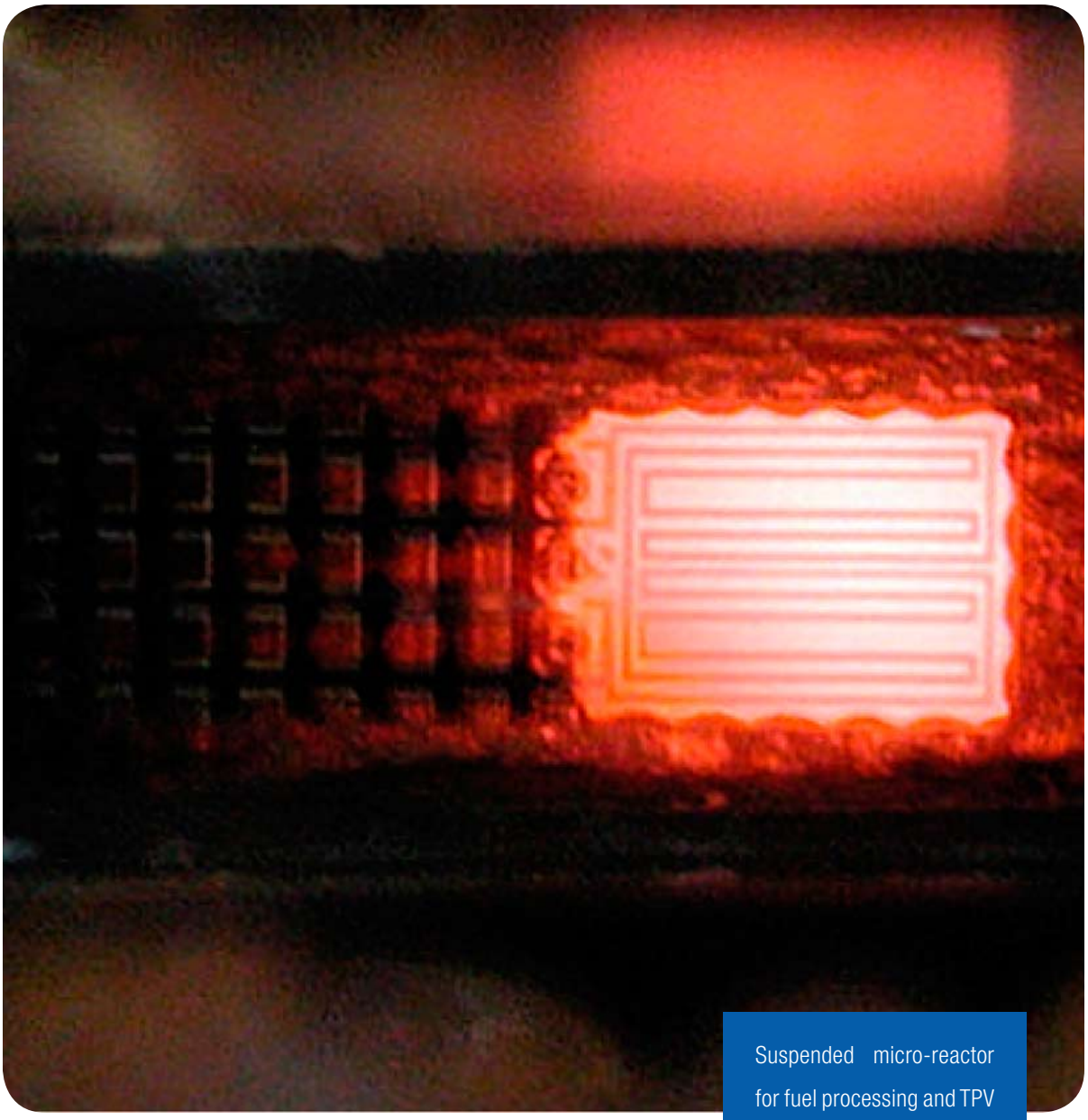


Figure 2: comparison of slice-and-cascade method with CWT as wavelength selectivity for plane-to-plane volume hologram

REFERENCES:

[1] Kogelnik, H., "Coupled Wave Theory for Thick Hologram Gratings," *Bell Syst. Tech. J.*, 48(9), 1969, pp. 2909-2947.



Suspended micro-reactor for fuel processing and TPV energy conversion. Photo by Ole Mattis Nielsen

MEMS

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Nanoscale Manipulation of Biological Entities Using Magnetic Particles and Fields

A. Balducci, D. Pregibon, H. Singh, L. Gonzalez, P. Matsudaira, T.A Hatton, P. Doyle
Sponsorship: NSF

An increasing number of "lab-on-a-chip" technologies and therapeutic treatments rely on the rapid isolation of clinically or scientifically relevant proteins, cells, and nucleic acids. Magnetic fields and forces provide a useful means of sorting and manipulating such biological entities. Researchers have successfully used magnetic particles, often decorated with target-specific antibodies, for applications in human leukocyte antigen (HLA) diagnostics, cell enrichment or depletion, protein isolation, biomechanics measurements, and the electrophoresis of nucleic acids. The goal of our research is to use uniform and non-uniform magnetic fields in MEMS devices to manipulate magnetic particles or bound entities for the purpose of developing tools that can more rapidly and efficiently sort DNA, blood cells, and cellular organelles.

We have previously demonstrated the electrophoresis of DNA in a microchannel using an array of self-assembled posts of magnetic particles [1]. We intend to investigate the effect of column spacing on separation efficiency and also the use of "blinking" magnetic fields (Figure 1) as a more rapid means to separate long-chain DNA, which tends to migrate very slowly in a static matrix. In addition, we have demonstrated, experimentally and through simulation, the ability to direct columns of magnetic beads laterally across a microfluidic channel, using patterned materials and a uniform magnetic field (Figure 2). This mechanism is the first step toward our development of a continuous, incubation-free cell-sorting device. Furthermore, we have utilized "saw-tooth" magnetic fields with aqueous ferrofluids to sort submicrometer (510 and 840nm) non-magnetic particles [2]. We believe this magnetophoresis will be useful in sorting subcellular, like-sized biological bodies, such as organelles and viruses.

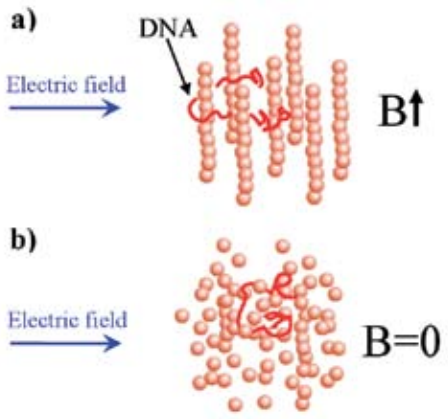

Figure 1: Conceptual electrophoresis of DNA using magnetic beads in a "blinking" magnetic field. (a) DNA caught on a post in a vertical field. (b) Release of DNA and destruction of posts when magnetic field is turned off.

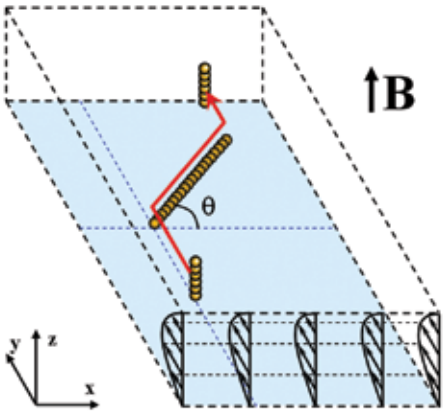

Figure 2: Schematic demonstrating the guidance of a magnetic bead column along a rail of similar beads patterned to the floor of a microfluidic channel.

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[2] Park, E.S., L.A. Gonzalez, K.A. Smith, T.A. Hatton, "Magnetophoretic Size-Based Trapping and Separation of Nonmagnetic, Submicrometer Particles in a Microsystem," submitted to *Analytical Chemistry*.

Suspended Microchannel Resonators for Biomolecular Detection

T.P. Burg, S.R. Manalis
Sponsorship: NIH, AFOSR

We have demonstrated a new approach for detecting biomolecular mass in the aqueous environment. Known as the suspended microchannel resonator (SMR), target molecules flow through a suspended microchannel and are captured by receptor molecules attached to the interior channel walls [1]. As with other resonant mass sensors, the SMR detects the amount of captured target molecules via the change in resonance frequency of the channel during the adsorption (Figures 1,2). However, what separates the SMR from the myriad of existing resonant mass sensors is that the receptors, targets, and their aqueous environment are confined inside the resonator, while the resonator itself can oscillate at high Q in an external vacuum environment, thus, yielding extraordinarily high mass resolution.

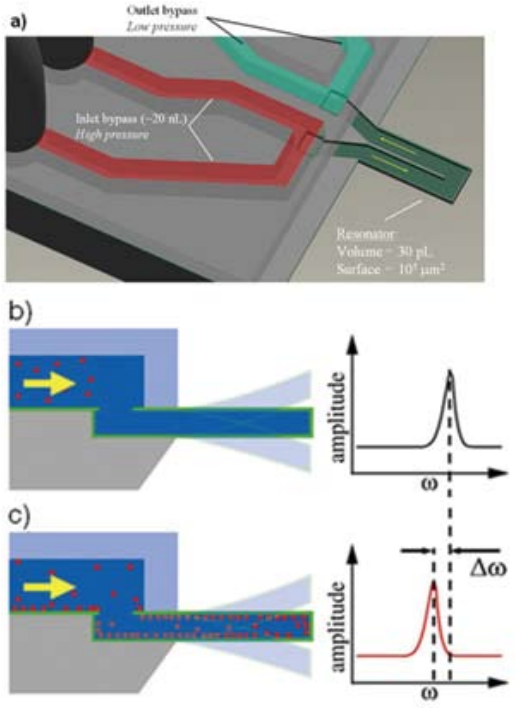

Figure 1: a) Suspended microchannel resonator (SMR); b) Cross-section of vibrating SMR; c) Targets bind to immobilized receptors (not shown), and the high surface concentration lowers the resonant frequency. Since biomolecules are more dense than solution (~1.4 g/cm^3), the resonant frequency is reduce by $\Delta\omega$.

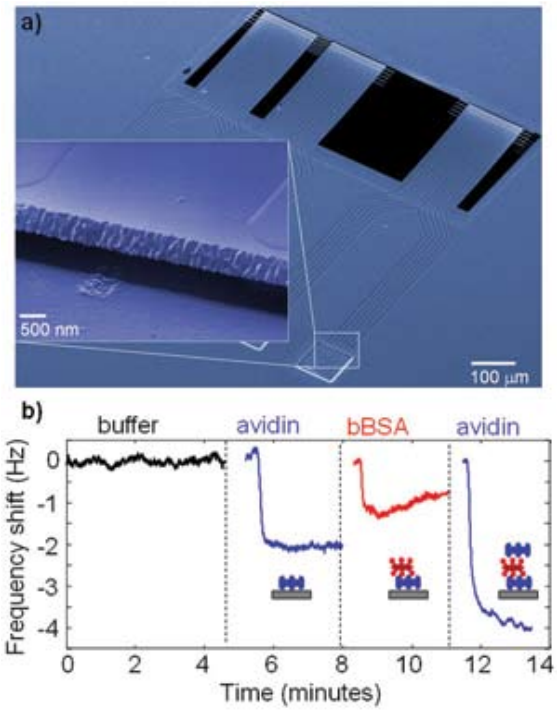

Figure 2: a) Electron micrograph of three suspended microchannel resonators; b) Relative frequency shift for a 40 kHz resonant microchannel after injection of the following solutions: buffer (black), avidin (blue), bBSA (red), and avidin (blue). The adsorption of the biomolecules to the interior channel walls increases the overall mass and lowers the resonant frequency.

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A Combined Microfluidic/Dielectrophoretic Microorganism Concentrator

N. Gadish, J. Voldman
Sponsorship: Charles Stark Draper Laboratory, Siebel Scholarship

This project focuses on the development of a microorganism concentrator for pathogen detection applications. A common problem in microfluidic systems is the mismatch between the volume of a sample and the volume that a device, such as a detector, can process in a reasonable amount of time. Concentrators can, therefore, be used in pathogen detection and other microfluidics applications to reduce sample sizes to the micro-scale without losing particles of interest.

The concentrator, illustrated in Figure 1, is an active filter that uses dielectrophoresis to concentrate bacterial spores in low-conductivity solution. Dielectrophoresis uses spatially nonuniform, alternating electric fields to move particles by polarizing them and then acting on the induced dipole [1]. This concentrator uses positive dielectrophoresis, pulling particles toward electric field maxima. In operation, we set up the electric fields by lining the bottom of the channel with interdigitated electrodes. We combine a passive mixer [2] with these electrodes to enable trapping at high flowrates: the mixer circulates the liquid, bringing particles to the bottom of the channel where they are trapped by the electrodes. When enough particles have been collected, they are all released at once in a small volume, thereby producing a concentrated sample. Figure 2 shows a plot of output concentration over time as a sample of beads is released. The plot was produced by sampling discrete droplets at the output of the device and measuring their bead concentration using a spectrophotometer. This result shows a concentration enhancement of 25x between the input (C_0) and output (Drop #5) concentrations.

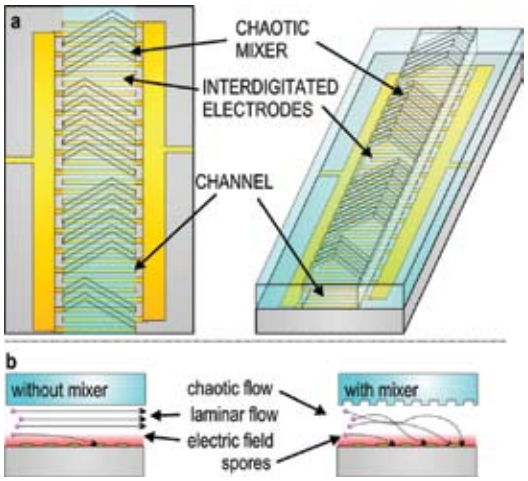

Figure 1: Illustration of the proposed concentrator. Interdigitated electrodes (a) on the bottom of the channel trap particles, and a passive mixer (b) circulates the liquid to enable trapping at high flowrates.

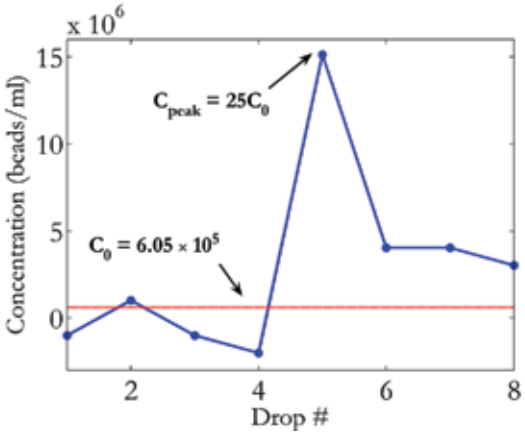

Figure 2: Experimental data of sample concentration. The blue curve shows the output concentration as it varies over time, measured in discrete drops. The peak concentration (C_{peak}) is 25 times the input concentration (C_0, indicated by the red line).

REFERENCES:

[1] Pohl, H.A, Dielectrophoresis, Cambridge University Press, Cambridge, UK, 1978.
[2] Stroock, A.D., *et al.*, "A Chaotic Mixer for Microchannels," *Science* 295, 647-651, 2002.

Single Molecule Analysis of DNA in Electric Fields

G. Randall, P. Doyle
Sponsorship: NSF

Recent advances in gene therapy and crime investigation have spurred a demand for rapid "gene mapping" of large (kbp-Mbp) DNA molecules. Because current electrophoresis technologies are inadequate for large DNA, several promising MEMS designs for DNA mapping have been recently proposed that require either: 1) a DNA molecule negotiating an obstacle course in a microchannel or 2) stretching a DNA coil for linear analysis. The goal of our research is to experimentally probe the fundamental physics that underlie these DNA mapping designs. In general, the governing physics is complex due to the confinement of the microchannel, the coiled-nature of long DNA molecules, and the induced electric field gradients from obstacles and changes in channel dimensions.

With single molecule microscopy, we have demonstrated many of the governing physical mechanisms at play in these gene mapping microfluidic devices [1-3]. For example, we have shown the experimental scaling for the diffusion coefficient of DNA in a confined channel (Figure 1a) and the probability distribution for the "collision time" of a DNA molecule unhooking from a small obstacle (Figure 1c). In addition, we have thoroughly investigated DNA stretching in electric field gradients created by a contraction and an obstacle (Figure 2). Just as a flow gradient stretches a polymer, an electric field gradient can stretch a charged polymer like DNA. Because electric field gradients have no local rotational components, a charged polymer will experience *purely extensional* deformation. These findings will aid the design of DNA separation devices that contain many obstacles and contractions, and they also offer an attractive way to completely stretch DNA for linear analysis.

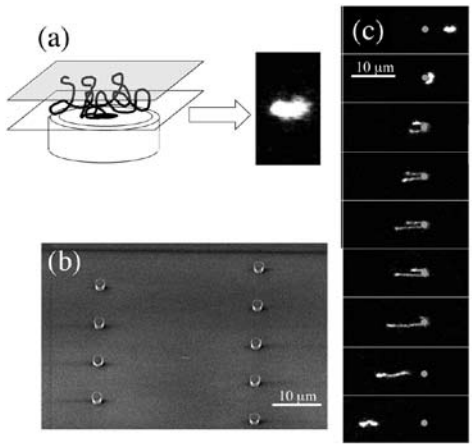

Figure 1: (a) Cartoon of a long DNA molecule in a thin slit over a microscope objective and a sample experimental image. (b) SEM image of a disperse array of small PDMS (polydimethylsiloxane) obstacles (R_{obs}=0.8 μm, height=2 μm). (c) A hooking collision of λ−DNA with one of the small obstacles (0.17 s intervals, DNA moving right to left).

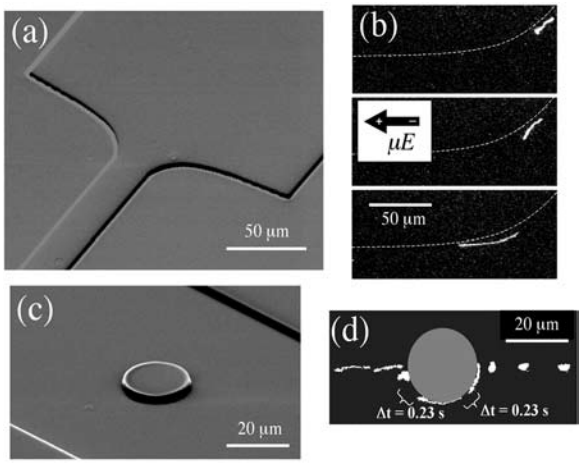

Figure 2: (a) SEM image of a hyperbolic PDMS contraction (height=2 μm). (b) A 2λ−DNA stretching near full extension in a hyperbolic contraction (DNA moving right to left). (c) SEM image of a large PDMS obstacle (R_{obs}=10 μm, height=2 μm). (d) A center-line collision of DNA with the large obstacle (0.33 s intervals unless noted, DNA moving right to left).

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[3] Randall, G.C., P.S. Doyle, "DNA Deformation in Electric Fields: DNA Driven Past a Cylindrical Obstruction," *Macromolecules*, vol. 38, pp. 2410-2418, February 2005.

Microfabricated Mechanical Biosensor with Inherently Differential Readout

C.A. Savran, T.P. Burg, J. Fritz, S.R. Manalis
Sponsorship: AFOSR, NSF

Intermolecular forces that result from adsorption of biomolecules can bend a micromachined cantilever and enable the detection of nucleic acids and proteins without any prior labeling of target molecules. Often, the cantilever deflection is detected using the optical lever method, i.e., by focusing a laser beam at the tip of the cantilever and measuring the changes in position of the reflected beam. Researchers have also shown that, by using the optical lever method to separately measure the bending of two identical cantilevers, the reliability of the signal resulting from the molecular binding reaction is improved by monitoring the relative or differential bending. [1]

We developed an interferometric sensor that inherently measures the differential bending between two adjacent cantilevers, thereby eliminating the need for two separate optical setups and alignment steps. The two cantilevers constitute a sensor-reference pair, whereby only the sensing surface is functionalized with receptors that are specific to the ligand to be detected (Figure 1). The two cantilevers have closely matched responses to background disturbances. Hence, disturbance-induced nonspecific deflections are suppressed upstream, i.e., before the optical signal is measured. We have previously shown that in air, the resolution of the interferometric cantilever-based sensor at high frequencies (40-1000 Hz) is limited by its sub-angstrom thermomechanical noise (~0.2 $Å_{RMS}$). However, at lower frequencies, the sensor exhibits a flicker or 1/f-type behavior, which yields noise levels that are much higher (~10 $Å_{RMS}$) than the thermomechanical noise. For biological applications of cantilever-based sensors, it is the low-frequency behavior in liquid that governs the detection limit. We have measured the low-frequency behavior of the sensor in liquid and demonstrated that it can be improved by differential detection (Figure 2) [2].

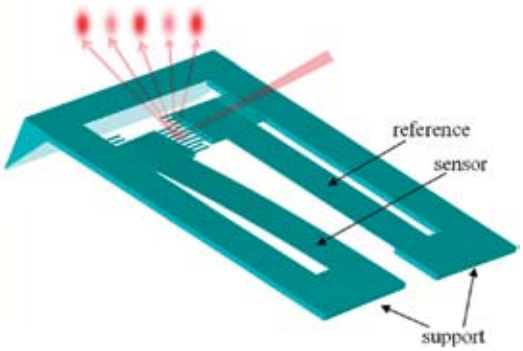

Figure 1: Schematic of the sensor. The pair of flexible sensor/reference cantilevers is supported by L-shaped thick structures that connect them to the die. The die is placed in a fluidic chamber. The differential bending is measured directly using the interference between two sets of interdigitated fingers.

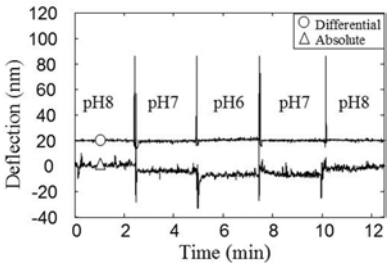

Figure 2: Absolute and differential cantilever bending due to pH changes in aqueous environment. Spikes represent injections. Absolute response (triangle) of a single cantilever to pH changes is significantly reduced by the differential detection (circle). Differential response was intentionally plotted with a DC offset for clarity.

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Micromechanical Detection of Proteins Using Aptamer-Based Receptor Molecules

C.A. Savran. S.M. Knudson, A.D. Ellington, S.R. Manalis
Sponsorship: AFOSR, NSF

Numerous studies have been conducted on using antibodies as receptors for detecting proteins. Although antibodies can be used to detect proteins with high sensitivity and specificity, they are generally produced *in vivo*, which introduces difficulties in engineering their properties. In contrast, aptamers (nucleic-acid binding species) can be selected *in vitro* and have been produced against a wide range of targets, from small molecules, to proteins, to whole cells. Aptamers are DNA or RNA molecules, which can form tertiary structures that recognize and bind to their respective targets.

We have investigated the capability of an aptamer-protein binding event to generate changes in surface stress that bend a flexible micromachined cantilever (Figure 1) [1]. We used a receptor-ligand system that was previously investigated and characterized in solution. The ligand, i.e. the target molecule, was Thermus aquaticus (Taq) DNA polymerase, an enzyme that is frequently used in polymerase chain reaction (PCR). The recognition element (receptor) of the sensor was an anti-Taq aptamer modified with a thiol group at one end to enable covalent linking onto a gold surface. The sensor cantilever was functionalized with aptamer molecules, and the reference cantilever was functionalized with oligonucleotides of nonspecific sequence. The differential bending between the two cantilevers was determined directly by using interferometry. We characterized the system in terms of its response to variation in ligand concentration, as well as, its ability to recognize a particular ligand in a complex mixture and to discriminate against nonspecific binding (Figure 2). Our results indicate that aptamers can be used with cantilever-based sensors for sensitive, specific, and repeatable protein detection.

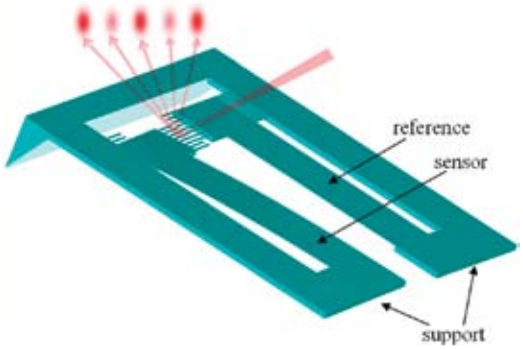

Figure 1: Schematic of the sensor. The pair of flexible sensor/reference cantilevers is supported by L-shaped thick structures that connect them to the die. The die is placed in a fluidic chamber. The differential bending is measured directly using the interference between two sets of interdigitated fingers.

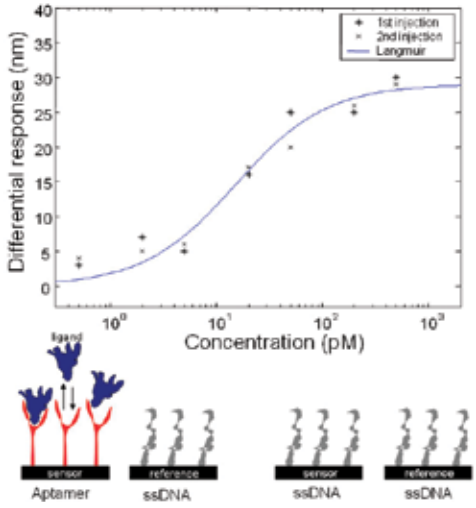

Figure 2: Variation of micromechanical sensor response with Taq DNA polymerase concentration. The experiment was performed twice for each concentration. A Langmuir-isotherm fit to the data revealed a Kd of 15pM.

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[1] Savran, C., S. Knudson, A.D. Ellington, S.R. Manalis, "Micromechanical Detection of Proteins Using Aptamer-Based Receptor Molecules," *Analytical Chemistry,* 76: 3194-3198 (2004).

Plasmon Microscopy on Gold and Gold/Oxide Surfaces

L. Chao, M. Steinback, A.P. Gast
Sponsorship: MIT ChemE

Surface plasmon resonance has primarily been used as a technique for measuring the thicknesses of very thin organic and polymer films on metallic surfaces with low lateral resolution. Its ability to sense unlabeled molecules and its speed of measurement are advantageous when observing real-time adsorption, desorption, or reactions, of biological molecules.

In this study, we will use the surface plasmon technique to create an imaging microscope to study planar lipid bilayers. We develop imaging optics that collect the plasmon reflectivity in a CCD (charged-coupled device) camera to provide real images of the optical thickness of absorbates as shown in Figure 1. To improve the lateral resolution, we will utilize protein barriers to restrict the motion of the lipids and to uniformly divide the observational field. We print these with a PDMS (polydimethylsiloxane) stamp made from photoresist masters created in the MTL Technology Research Laboratory. To provide a surface commensurate with other experimentation on the lipids, we coat the metallic interface with a 10 nm layer of silicon dioxide, which has a minimal effect on sensitivity. The metallic surface and the silicon dioxide coating are evaporated in the MTL Exploratory Materials Laboratory. In Figure 2, we show a static corral pattern with 50x50 μm^2 areas of 40% 1,2-dioleoyl-sn-glyceri-3-phosphocholine (DOPC)/30% egg-sphingomyelin/30% cholesterol surrounded by 10 micrometer wide BSA (Bovine Serum Albumin) protein spacers. The width is foreshortened by the experimental setup.

After improving the lateral resolution, this technique will be able to image the domain dynamics caused by enzyme reactions in a high throughput way.

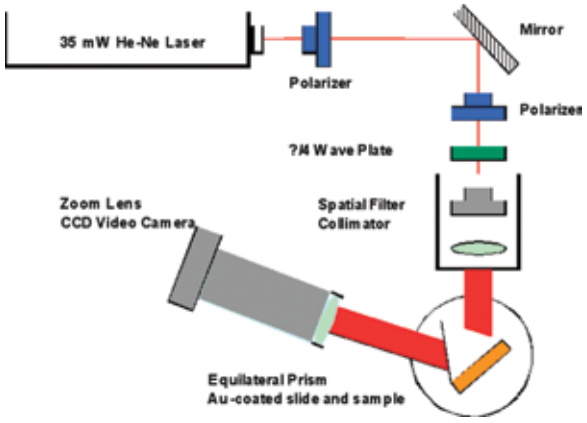

Figure 1: Optical layout of the surface plasmon microscope.

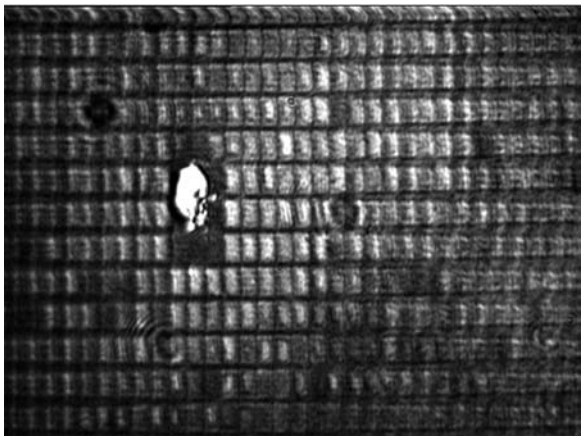

Figure 2: BSA corrals containing lipid layer. Size is 50x50 μm^2 with 10 µm separations.

Use of Stamped Protein Corrals in High Throughput Studies of Lipid Membrane Model Systems

L. Chao, M. Steinback, A.P. Gast
Sponsorship: MIT ChemE

Supported lipid bilayers are useful *in vitro* mimics for natural biological membranes, and various biotechnological applications are facilitated by their planar geometry. In this study, variable compositions or conditions will be created on supported planar lipid bilayers in order to study the coupled effects of enzyme, membrane, and solution composition on the sphingomyelinase enzymatic reaction. We combine gradients produced by microfluidic flows with membranes confined to surface patterned corrals in order to achieve a high throughput experimental system in which the preparation and measurement times can be greatly reduced. We employ poly(dimethylsiloxane) (PDMS) stamps, which are made from photoresist masters created in the MTL Technology Research Laboratory, to print proteins [1] onto glass surfaces to create barriers capable of restricting the motion of lipids to specific regions of the surface called corrals, as shown in Figure 1. The various membrane conditions in the corrals can be created by incorporating the patterned surface within a microfluidic device. The laminar flow in the micofluidic channel causes fluid elements to follow streamlines, mixing across the streamlines only by diffusion. To create varying lipid bilayer compositions, vesicles are deposited from solution and irreversibly stick to form a continuous bilayer within each corral. As a consequence, a particular vesicle composition in the microfluidic channel is captured by the surface and is restricted in each corral, as shown in Figure 2. Likewise, we can create gradients in the bulk solutions (e.g. enzyme concentration or buffer conditions) by varying the composition in neighboring laminar streams. The desired corralled lipid composition gradient or desired solution condition gradient upon corralled lipid can be adjusted by flow parameters and scale of corral size.

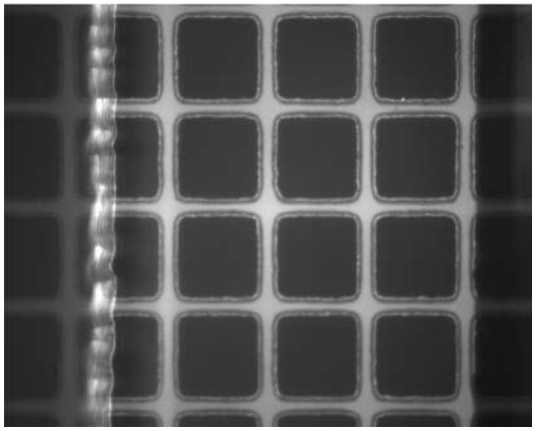

Figure 1: A Texas-Red labeled Bovine Serum Albumin (TR-BSA) corral printed on a glass coverslip in a 200μm wide microchannel. The size of each corral is 50μm x 50μm.

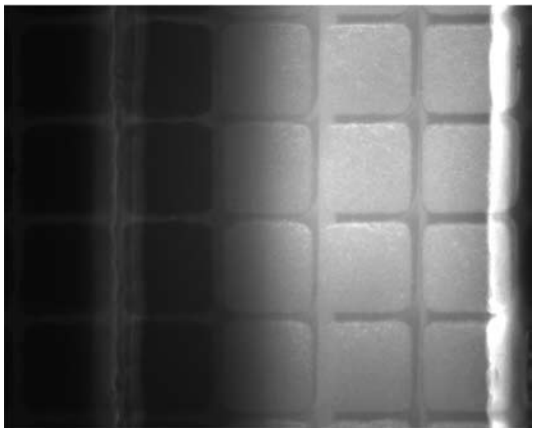

Figure 2: A preliminary lipid bilayer composition gradient formed in a 200μm wide and 50 μm high channel. Neighboring streams of vesicles are flowed over the glass coverslip patterned with BSA. The vesicles deposit a supported lipid bilayer, and the excess is washed away with the buffer. The corrals capture the composition gradient after the flow is stopped.

REFERENCES:

[1] Kung, L.A., L.Kam, J.S. Hovis, S.G. Boxer, "Patterning Hybrid Surfaces of Proteins and Supported Lipid Bilayers," *Langmuir*, vol. 16, p. 6776, 2000.

Use of Microfluidic Device to Study Protein-Polymer Interactions

P.A. Achurra[§], C.R. Robertson[§], A.P. Gast*
Sponsorship: E&J Gallo Winery

In recent years, the importance of polymer architecture on their physical properties has been recognized. We are studying the effect of a polymer's macromolecular architecture on its ability to interact with other molecules, in particular with proteins.

In order to study a variety of protein-polymer interactions we developed a microfluidic platform. We monitor polymer-protein interactions by means of fluorescence resonance energy transfer (FRET), where the polymer molecules are unlabeled and two populations of protein molecules are fluorescently labeled with a FRET donor and an acceptor pair. Because a FRET signal is highly distance-dependent, without interaction we observe little FRET, and upon complexation, we observe a strong FRET signal (Figure 1).

We are interested in the effects of polymer branching on protein aggregation and have chosen a model system of different generations of Poly(amidoamine) PAMAM dendrimers and fluorescently labeled Streptavidin. We can manipulate the overall charge of PAMAM dendrimers either by selecting dendrimers generation (G0, G2, G4, etc) or by adjusting the solution pH.

We create a microfluidic device from polydimethylsiloxane (PDMS). The laminar flow in these channels allows us to directly compare polymer or control solutions interacting with the protein solution by interdiffusion. Our initial results show qualitative differences between Streptavidin/PAMAM (G2) and Streptavidin/PAMAM (G4) interactions (Figure 2). As molecules move along the channel, they start interacting. We observe both a shift in peak position, as well as, changes in intensity profiles as the molecules move away from the junction point. The peak position shift indicates that, indeed, both polymers interact with Streptavidin and that changes in intensity profiles are not solely caused by diffusion. Differences between the intensity profiles of Streptavidin/PAMAM G2 and Streptavidin/PAMAM G4 show that indeed both polymers interact differently with Streptavidin molecules; we are currently analyzing these FRET profiles to provide a quantitative measure of protein-polymer interaction.

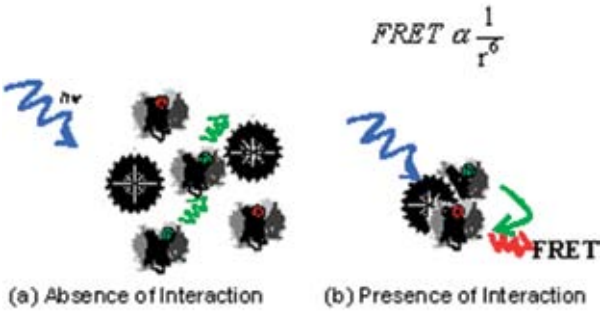

Figure 1: Schematic of FRET experiment. In the absence of interaction, there is little or no FRET signal observed; in the presence of interaction significant energy transfer occurs between donor and acceptor molecules, and FRET is observed D: FRET donor, A: FRET acceptor.

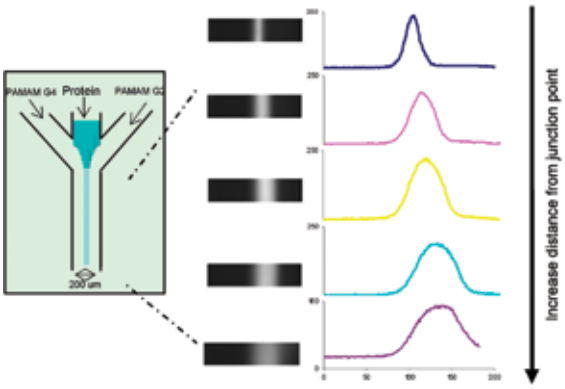

Figure 2: A microfluidic device for studying protein/polymer interactions. On the left is a diagram of the device; in the center are FRET images at different distances from the junction; on the right are intensity profiles from FRET images.

§ Department of Chemical Engineering, Stanford University.
* Department of Chemical Engineering, Massachusetts Institute of Technology.

Super-Hydrophobic Surfaces for Hemocompatibility

A.J. Schrauth, N. Saka, N.P. Suh
Sponsorship: Korean Institute of Machinery and Materials

It is well known that in fluid systems, as geometric scale decreases, the effect of surface forces increases relative to body forces. This property has been exploited to modify the wetting behavior of fluids on a surface by structuring the surface. By reducing feature size, surfaces have been developed that have a contact angle with water that approaches 180° when the flat-surface contact angle of the material is closer to 100° [1]. Our project focuses on making these so-called super-hydrophobic surfaces practical to manufacture. We have manufactured surfaces with water contact angles above 160° by casting poly-dimethylsiloxane (PDMS), a material with a flat-surface water contact angle of approximately 100°. Our methods are limited by the size of a low temperature oven, not by wafer size. Thus, we can scale production size up beyond the limits of typical microfabrication techniques.

Additionally, we are interested in the application of super-hydrophobic surfaces in bio-medical systems to improve hemocompatability. A material is hemocompatable if it does not react unfavorably in the presence of blood. Hemocompatible surfaces are crucial to the performance of many biomedical devices. One of the requirements for such surfaces is the ability to resist the coagulation of proteins from blood. The increase in contact angle for super-hydrophobic surfaces is driven by a reduction in the interaction between the fluid and the surface. We are investigating the hypothesis that reducing the fluid-surface interaction between blood and a surface by microstructuring will decrease protein deposition on the surface.

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[1] Krupenkin *et al.*, "From Rolling Ball to Complete Wetting: The Dynamic Tuning of Liquids on Nanostructured Surfaces," *Langmuir*, 20, pp.3824-3827, 2004.

Electrical Properties of the Tectorial Membrane Measured with a Microfabricated Planar Patch Clamp

R. Ghaffari, D.M. Freeman
Sponsorship: NIH

The tectorial membrane (TM) is a mechanical structure in the cochlea that plays a critical role in hearing. Although its composition suggests that it contains an abundance of charged molecules–charges that may contribute to its mechanical properties–measuring the concentration of this fixed charge has been difficult. Since the TM lacks an insulating cell membrane, traditional micropipette techniques have not yielded stable measurements of the electrical potential of the TM.

We have developed a microfabricated chamber that overcomes this problem by placing the TM as an electrochemical barrier separating two fluid baths. The chamber consists of a small aperture into a microfluidic channel (Figure 1), similar to previous planar patch clamp designs [1]. The aperture diameter was chosen to be small enough to be covered by the TM, while large enough to contribute little electrical resistance. The microfluidic channel allows perfusion of the fluid below the TM, so the ionic composition of fluids in both baths can be rapidly changed. Varying the ionic concentration of the baths changes the electrical potential between baths in a manner that depends on the fixed charge of the TM. The microfabricated chamber has enabled the first stable, repeatable measurements of this electrical potential (Figure 2). The results suggest that the TM contains sufficient charge to completely account for its mechanical rigidity.

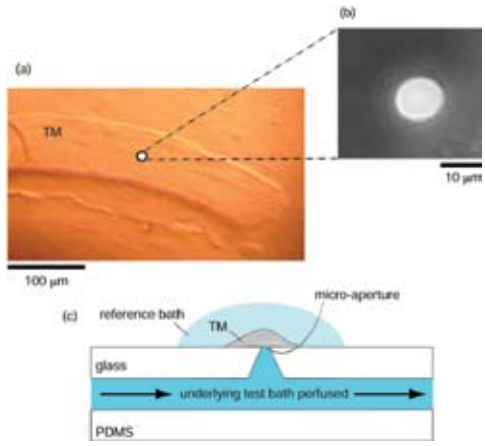

Figure 1: Microfabricated planar patch clamp setup. (a) Top view of a section of TM placed on the planar patch clamp containing a micro-aperture, drawn as a white circle for visibility. (b) Closer view of the micro-aperture with the TM removed. (c) The test bath in the underlying fluidics channel was perfused with solutions of different ionic strength during voltage recordings.

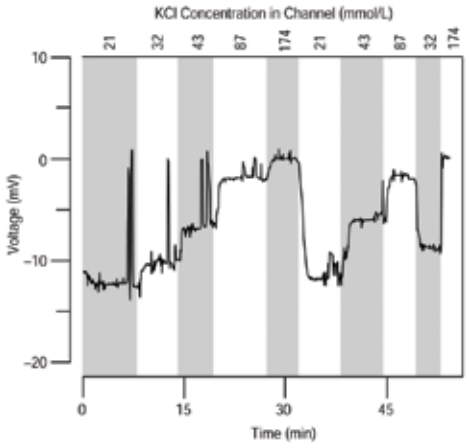

Figure 2: Voltage measurements with varying test solutions. Voltages were found to be stable and repeatable over several minutes up to hours during perfusion and TM voltage recordings. The shaded regions indicate times with different perfusates. The large transient voltage spikes result from intentionally shorting the two baths to check for drift in the measurement system.

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[1] Sigworth, F.J., K.G. Klemic, "Patch Clamp On A Chip," *Biophys J*, vol. 82, 2002, pp. 2831-2832.

Microfabricated Shearing Probes for Measuring Material Properties of the Tectorial Membrane at Audio Frequencies

J.W. Gu, A.J. Aranyosi, W. Hemmert, D.M. Freeman
Sponsorship: NIH

The tectorial membrane (TM) is ideally located to exert shearing forces on sensory hair cells in the cochlea in response to sound. Consequently, measuring the shear impedance of the TM is important for understanding the mechanical basis of hearing. However, few direct measurements of TM shear impedance exist, because the small size of the TM and the need to measure its properties at audio frequencies render traditional impedance measurement methods infeasible. We have overcome these limitations by designing and microfabricating shearing probes that are comparable in size to the TM and that can exert forces at audio frequencies.

The probes consist of systems of cantilevers designed to apply forces in two dimensions (Figure 1). Forces applied to the base of the probe are coupled through the cantilevers to a shearing plate, which is brought into contact with the TM. By measuring the relative deflection of the base and plate and knowing the probe stiffness, we can determine the shear impedance of the TM. A variety of probes with different stiffnesses and geometries allow measurement of impedance over many orders of magnitude. Figure 2 shows a probe whose shearing plate is in contact with the TM. To determine TM impedance at audio frequencies, we have coupled these probes to a computer microvision system that allows measurements of nanometer-scale motions at high frequencies [1]. The probes were calibrated, and could exert forces with amplitudes in the range 3-300 nN at frequencies from 10-9000 Hz, a large fraction of the hearing range. Measurements of TM shear impedance, using these microfabricated probes, have helped to characterize this enigmatic component of the cochlea.

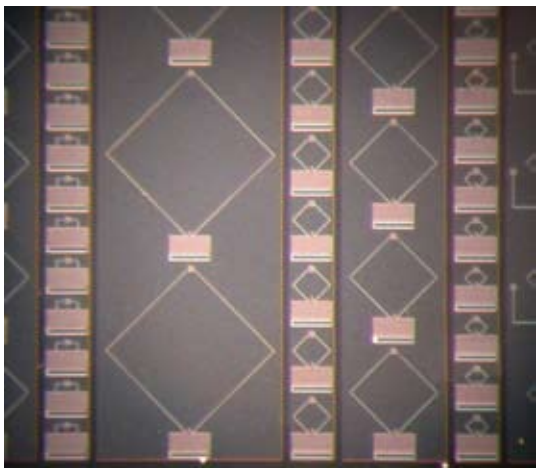

Figure 1: Microfabricated shearing probes on a silicon chip. Each probe consists of a base, a pair of cantilevered arms, and a small shearing plate. The probe stiffness depends on its size.

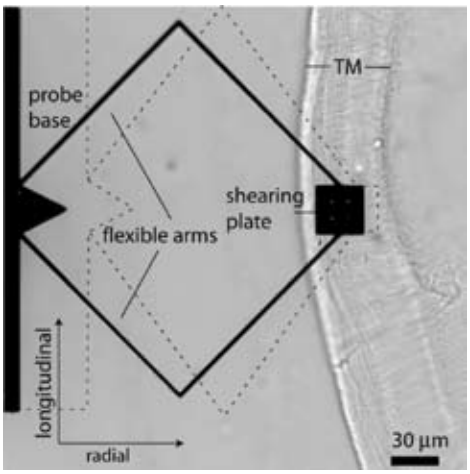

Figure 2: Stop-action video image of microfabricated probe on TM specimen. Displacements of the base cause relative motion of the base and plate (dotted line); this relative motion varies with TM impedance. Probe motions are greatly exaggerated for clarity.

REFERENCES:

[1] Davis, C.Q., D.M Freeman, "Using A Light Microscope To Measure Motions With Nanometer Accuracy," *Opt Eng,* vol. 37, pp. 1290-1298, 1998.

Implantable MEMS for Drug Delivery

H.L. Ho Duc, R.S. Langer, M.J. Cima
Sponsorship: NIH, NCI

We have developed an implantable silicon microelectromechanical system (MEMS) device for biomedical applications [1]. This device contains an array of wells that hermetically store its contents. Activation of the device electrochemically dissolves gold membranes covering the wells, by application of an anodic voltage through a wire-bonded connector (Figure 1). The well contents are then exposed to the surrounding environment. This system allows temporal control of several activations and the ability to store a variety of contents separately. Targeted application for this device is local drug delivery.

We have focused our drug delivery efforts on carmustine (BCNU), a potent brain cancer drug. Local delivery of BCNU from an implanted device results in efficacious concentrations at the tumor site, coupled with reduced systemic toxicity, which is a major drawback of the systemic delivery of BCNU [2]. We have achieved successful *in vitro* and *in vivo* release of BCNU, and have shown it to significantly impede tumor growth in rats as a result of co-formulation with polyethylene glycol (PEG) to improve release kinetics, and of the development of a new, Pyrex-based package that increases the capacity of the device [3]. Combination therapy of BCNU with Interleukin-2 (IL-2), however, has been shown to be more effective than either alone against tumors [4]. We, therefore, plan to use our device to achieve combination releases, to fully utilize the advantages of our MEMS, i.e., temporal control and multi-drug releases.

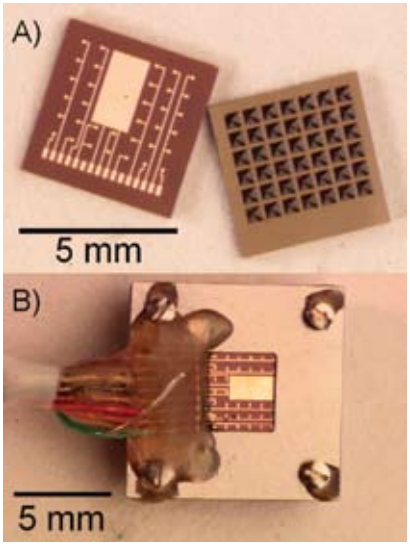

Figure 1: Photographs showing (A) top and bottom of the silicon microchip, and (B) a packaged device with wire-bonded connector

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A Peristaltic Oxygenating Mixer for Miniature Integrated Bioreactors

H.L.T. Lee, R.J. Ram
Sponsorship: Dupont-MIT Alliance

We have developed a mixer and corresponding fabrication process to address problems involved in the development of a miniaturized parallel integrated bioreactor array system, whose functional objectives include: (1) the ability to support cell growth of aerobic micro-organisms without oxygen limitation, (2) scalability to a large number of reactors, (3) online sensing of culture parameters, and (4) individual control over pH. In order to achieve these design objectives, we have developed a flat form factor, all PDMS (silicone elastomer), peristaltic oxygenating mixer (Figure 1), using a fabrication process that allows integrating multiple scale (100μm-1cm) and multiple depth (100μm-2mm) structures in a simple molding process. The flat form factor ensures a high surface area to volume ratio for high oxygen transfer rates, and the peristaltic action achieves in-plane homogeneous mixing within 5-20 seconds, depending on the depth of the well and actuation parameters, which is three orders of magnitude faster than lateral mixing from diffusion alone. The peristaltic action also contributes to mixing in the vertical direction, which further improves the oxygen transfer rate. The volumetric oxygen transfer coefficient (k_La) was measured by a gassing-in method [1], using an integrated platinum-octaethylporphyrine based dissolved oxygen sensor [2]. Calibrated measurements of the oxygen transfer coefficient (Figure 2) in devices of various well depths agree with theoretically expected oxygen transfer coefficients for unmixed devices. For devices mixed with various actuation frequencies, the measured oxygen transfer coefficient falls short of the theoretical values due to non-instantaneous vertical mixing. Even with non-optimized devices, preliminary results from eight simultaneous bacteria growth experiments, using four different medium compositions with online measured optical density and dissolved oxygen concentration, indicate that the oxygen transport is sufficient to maintain a greater than 55% dissolved oxygen concentration for the duration of the bioreaction.

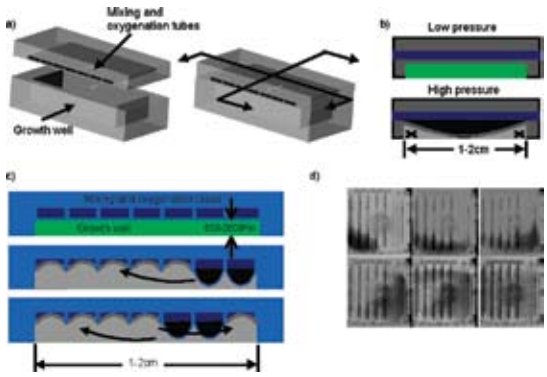

Figure 1. a) Exploded view of peristaltic oxygenating mixer. b) Low and high pressure cross sections along a mixing tube. X's indicate the return path for fluid flow. c) Cross -section across mixing tubes showing the actuation pattern, which approximates peristalsis. Arrows indicate direction of fluid flow. d) Photographs of a 750µm deep 15mm x 15mm device for 0, 1, 2, 4, 6, and 10 seconds after mixing at 25Hz and 4psi was initiated.

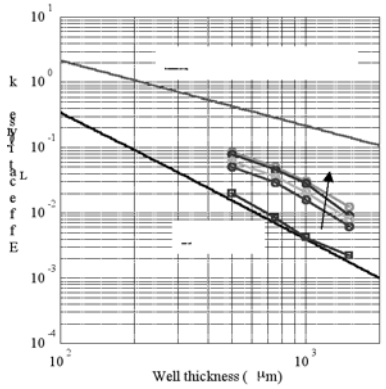

Figure 2: Calibrated oxygen transfer coefficient measurements for 500µm, 750µm, 1000µm and 1500µm deep wells and a 50µm thick peristalsis membrane. Actuation pressure was 4psi, and the arrow indicates increasing actuation frequency from 6, 12, 25, and 40Hz.

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Microfluidic Platform for High-Density Multiplexed Biological Assays

J. A. Benn, J. Hu, T. Thorsen
Sponsorship: Deshpande Center for Technological Innovation

We have developed a microfluidics-based technology that will support the ongoing need to reduce the cost and increase the capabilities of genetic testing in areas such as: population studies for the identification of inherited disease genes, more effective evaluation of drug candidates, and rapid determination of gene expression in tissues for disease management. This technology will also reduce the cost of the clinical testing of novel genetic targets related to disease risk and drug response.

Specific improvements promised by this technology are the following:

- Provides a flexible microfluidic enabling platform for genomic, proteomic and cellular array-based assays;
- Can be used with current diagnostic protocols and instrumentation;
- Tests many samples in parallel on the same microarray;
- Reduces the time it takes to perform genetic tests on microarrays from hours to minutes.

The elastomeric microfluidic device can print high-density DNA microarrays with dimensions as small as 10 µm. The device (Figure 1), which hermetically seals to a glass slide, patterns hundreds of DNA targets in parallel as lines on the glass surface. DNA samples are introduced into the sample entry ports and drawn along the channels, where they are exposed to and bind to the slide. After patterning, subsequent probe-target hybridization is simply achieved by running fluorescently labeled samples orthogonally over the target DNA-patterned glass slide, using a second microfluidic chip. Hybridization is achieved in less than 5 minutes; orders of magnitude faster than conventional DNA microarrays that require 16 hours for the same process. Using 10 µm wide microchannels, the hybridization spot density can be increased to over 400,000 assays per cm^2.

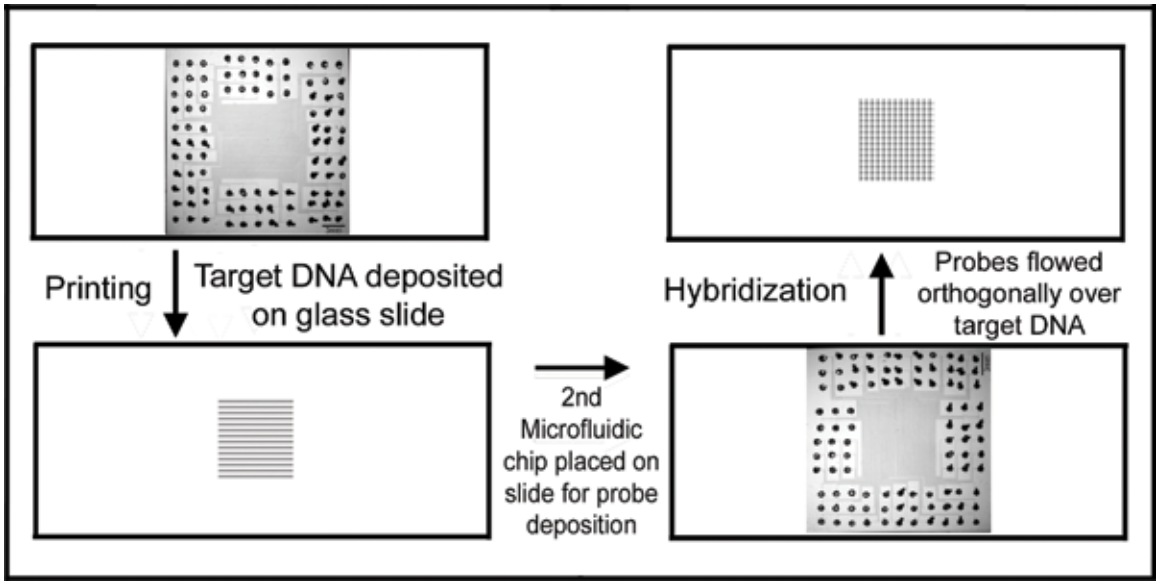

Figure 1: Illustration of DNA target printing and subsequent probe hybridization using a microfluidic array device.

Polymer-Based Microbioreactors for High Throughput Bioprocessing

Z. Zhang, G. Perozziello, N. Szita, A. Zanzotto, P. Boccazzi, A.J. Sinskey, K.F. Jensen
Sponsorship: Dupont-MIT Alliance

This project aims to develop high-throughput platforms for bioprocess discovery and developments, specifically automated microbioreactors; each with integrated bioanalytical devices, and operating in parallel. By microfabrication and precision machining of polymer material such as poly(dimethylsiloxane) (PDMS) [1] and poly(methylmethacrylate) (PMMA) [2, 3], we realize microliter (5~150 µl) microbioreactors (Figure 1) with integrated active magnetic mixing and dissolved oxygen, optical density, and pH optical measurements (Figure. 2) for monitoring nutrients and products. Reproducible batch and fed-batch [2] fermentation of *Escherichia coli* and *Saccharomyces cerevisiae* have been demonstrated in the microbioreactor. With the integration of local temperature control, cell-resistance surface modification, and pressure-driven flow at ~µL/min rates, the microbioreactor was also proven to be capable for chemostat continuous cell culture [3], which is a unique and powerful tool for biological and physiological research. As examples of bioanalysis, HPLC [1] and gene expression analysis [4] using microbioreactors have demonstrated potential applications in bioprocess developments.

Parallel microbial fermentations were undertaken in a multiplexed system demonstrating the utility of microbioreactors in high-throughput experimentation [5]. A key issue for high-throughput bioprocessing is to have inexpansive and disposable microbioreactors to save operation time and labor. Current works include the integration of plug-n-pump microfluidic connections [6] in the microbioreactor system, as well as, incorporation of fabricated polymer micro-optical lenses and connectors for biological measurements to produce "cassettes" of microbioreactors.

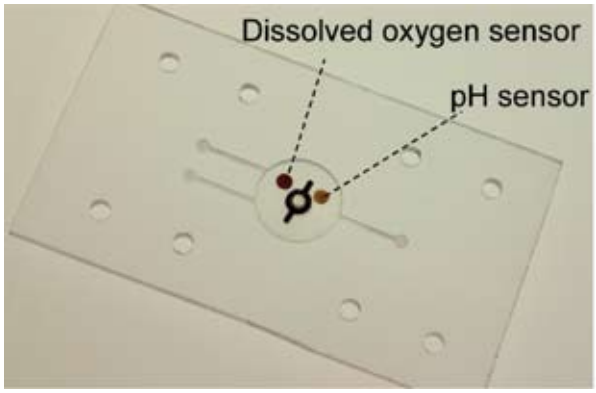

Figure 1: Photograph of the empty PMMA chamber of the microbioreactor. The magnetic stir bar in the center and the fluorescent sensors for DO and pH are visible.

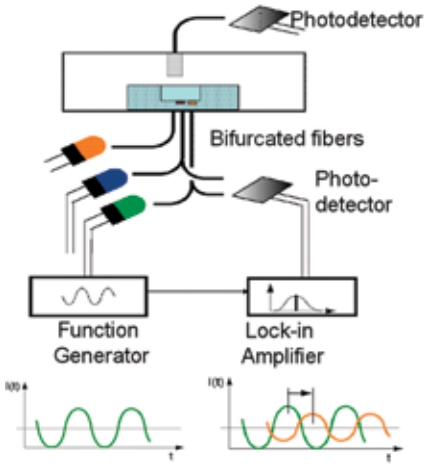

Figure 2: Experimental setup for optical measurements in the microbioreactor. Dissolved oxygen and pH are monitored by luorescence lifetime measurements. Biomass concentration is obtained by optical density, the transmission measurement by using an orange LED.

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Cell Stimulation, Lysis, and Separation in Microdevices

J. Albrecht, J. El-Ali, S. Gaudet, K.F. Jensen
Sponsorship: NIH

Quantitative data on the dynamics of cell signaling induced by different stimuli requires large sets of self-consistent and dynamic measures of protein activities, concentrations, and states of modification. A typical process flow in these experiments starts with the addition of stimuli to cells (cytokines or growth factors) under controlled conditions of concentration, time, and temperature, followed at various intervals by cell lysis and the preparation of extracts (Figure 1). Microfluidic systems offer the potential to do these experiments in a reproducible and automated fashion.

Figure 1 shows a schematic of a microfluidic device for rapid stimulus and lysis of cells. The fluidic systems with stimulus and lysis zones are defined using soft lithography in a poly(dimethylsiloxane) (PDMS) layer, which is then bonded to a glass slide. Temperature regulation for the two zones is achieved by using a thermo electric (TE) heater at 37°C to mimic physiological conditions during stimulation and a TE cooler at 4°C to inhibit further stimulus during lysis. Mixing in the device is enhanced by the use of segmented gas-liquid flow.

To extract meaningful data from cellular preparations, current biological assays require labor-intensive sample purification to be effective. Micro-electrophoretic separators have several important advantages over their conventional counterparts, including shorter separation times, enhanced heat transfer, and the potential to be integrated into other devices on-chip. A PDMS isoelectric focusing device has been developed to perform rapid separations by using electric fields orthogonal to fluid flow (Figure 2). This device has been shown to separate low molecular weight dyes, proteins, and organelles [1].

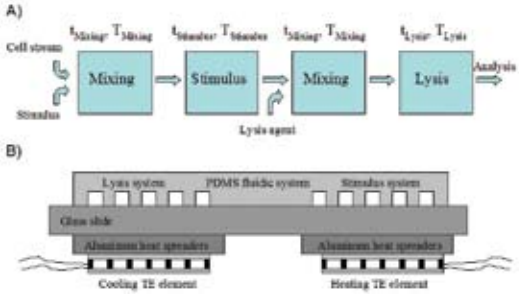

Figure 1: A) Typical process flow for cell stimulus. B) Schematic of cell stimulus device. A PDMS fluidic system is bonded to a glass slide and TE elements attached on the back through aluminum heat spreaders, which are used to control the temperature on the device.

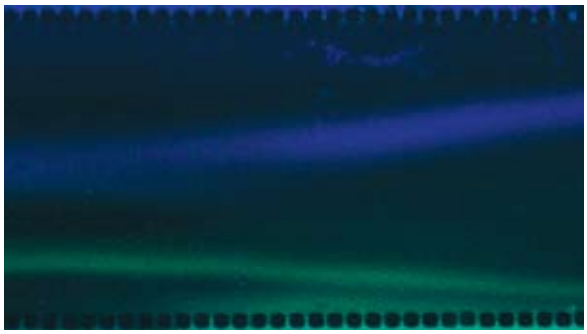

Figure 2: Rapid isoelectric focusing of two fluorescently labeled dyes. Flow is right to left. The anode is above the top row of posts, and the cathode at the bottom. Image shows focusing occurs in as little as 10 seconds.

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Microfluidic Devices for Biological Cell Capture

A.L. Gerhardt, M. Toner, M. Gray, M.A. Schmidt
Sponsorship: MGH, Shriners Burns Hospital

Over the past century, cellular biology and biomechanical engineering blazed ahead in areas, such as: genome sequencing, optical probes, and high-throughput biochemical testing. For example, an increasing variety of optical imaging probes now are available for chemical and biological analyses of molecular events, physiological processes, and pathologic conditions. In contrast, cell culture techniques have remained virtually stagnant [1]. Advances in MEMS, including microfluidics and soft lithography, are providing a toolset from which to develop biological MEMS devices. In addition to miniaturizing macro biological analysis tools, techniques, and assays, microfluidic devices can utilize microscale phenomena and systems to probe single- and multi-cellular levels yielding complimentary static and dynamic data sets [1,2]. Combining these advances with more traditional microtechnology provides groundwork for developing a new generation of cell culture and analysis. Assay protocols can be run in parallel, and dynamic single-cell event information can be collected on a small or large population of cells. Cells can be probed rapidly and inexpensively in large or small quantities with small sample sizes in custom, portable microenvironments developed to more physiologically resemble in vivo conditions [2]. Modular microfluidic devices are expanding possibilities, enabling snap-in modifications for different or second-pass assays. Biological cell capture and analysis devices are shown in Figure 1 and Figure 2. Designed to capture and maintain a specific number of cells in predetermined locations, the devices yield a mechanism by which to study isolated cells or cell-to-cell interaction. Once captured, the cells can be probed and static and dynamic data extracted on the single- and multi-cellular levels.

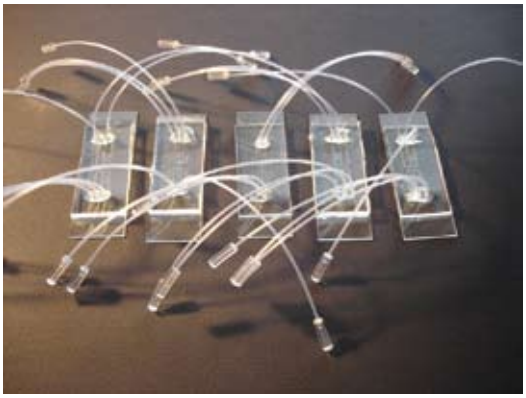

Figure 1: Packaged microfluidic devices for biological cell capture. Composed of a polydimenthylsiloxane (PDMS) cast bonded to a glass substrate, each device has standard microscope slide horizontal dimensions (25 mm x 75 mm) and a vertical dimension of about 10 mm (excluding macro connections). Captured cells can be viewed using non-inverted and inverted optical techniques.

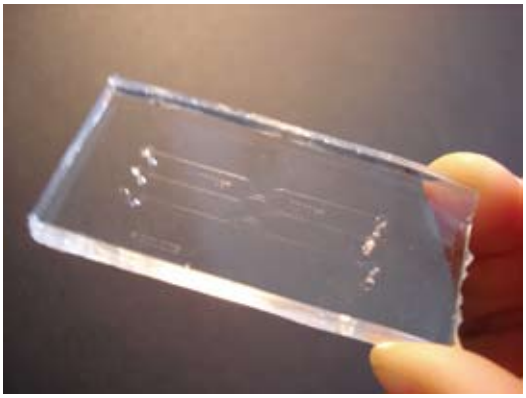

Figure 2: SU-8 masters define the microfluidic channel patterns, which are then cast in PDMS. Custom-machined hollow needles are used to punch holes for macro fluidic connections. Shown above is a 25 mm x 50 mm punched PDMS cast with 3 channels. Multiple channels enable process parallelization and more cell capture sites, increasing the statistical significance of collected data.

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Manipulating Solid Particles In Microfluidic Systems

J.G. Kralj, M. Sultana, M.A. Schmidt, K.F. Jensen
Sponsorship: MIT Microchemical Systems Technology Center, Merck

Microfluidic systems offer a unique toolset for the separation of microparticles and for the study of the growth kinetics of crystal systems because of laminar flow profiles and good optical access for measurements. Conventional separation techniques for particles, such as sieving, are limited to sizes larger than ~ 50 microns with large dispersion. Sorting microparticles (e.g. small crystals, single cells), requires different techniques. Dielectrophoresis is particularly attractive for microfluidic systems because large electric field gradients that drive the force are easily generated at low voltages using microfabricated electrode structures, and fixed charges are not required as in electrophoresis. It is possible to continuously separate particles of 1-10 microns with ~ 1 micron resolution (Figure 1) using dielectrophoresis with asymmetric electric fields and laminar flow (Figure 2).

Microfluidic devices can also be used to study crystallization and extract kinetic parameters of nucleation and growth, and to study different polymorphs of a system. Crystallization has been achieved in some batch processes that do not have uniform process conditions or mixing of the reactants, resulting in polydisperse crystal size distributions (CSD) and impure polymorphs. Microsystems allow for better control over the process parameters, such as the temperature and the contact mode of the reactants, creating uniform process conditions. Thus, they have the potential to produce crystals with a single morphology and uniform size distribution.

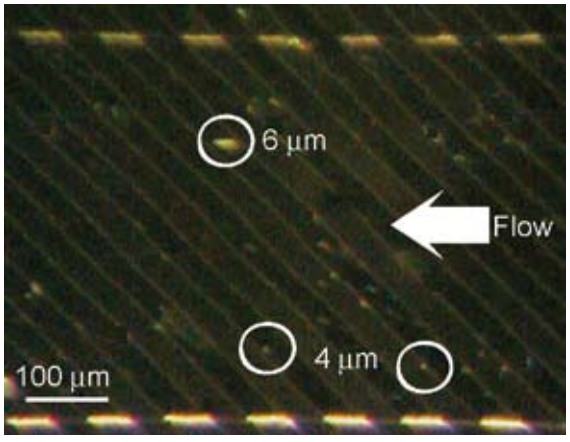

Figure 1: Dielectrophoretic forces generated by AC voltage and slanted electrode structures separate 4 & 6 micron particles, shown here near the device outlet.

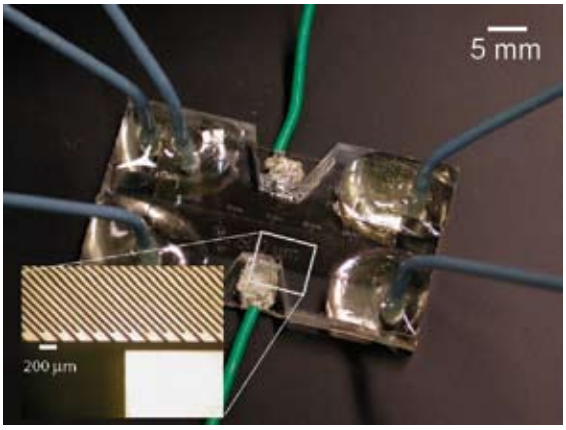

Figure 2: The packaged separator device is made of silicone rubber (PDMS), using soft-lithography techniques on interdigitated electrodes.

BioMEMS for Control of the Stem Cell Microenvironment

L. Kim, A. Rosenthal, J. Voldman
Sponsorship: NIH

The stem cell microenvironment is influenced by several factors, including: cell-media, cell-cell, and cell-matrix interactions. Although conventional cell-culture techniques have been successful, they offer poor control of the cellular microenvironment. To enhance traditional techniques, we have designed a microscale system to perform massively parallel cell culture on a chip.

To control cell-matrix and cell-cell interactions, we use dielectrophoresis (DEP), which uses non-uniform AC electric fields to position cells on or between electrodes [1]. We present a novel microfabricated DEP trap, designed to pattern large arrays of single cells. We have experimentally validated the trap using polystyrene beads, and have shown excellent agreement with our model predictions without the use of fitting parameters (Figure1A) [2]. In addition, we have demonstrated trapping with cells by using our traps to position murine fibroblasts in a 3x3 array (Figure 1B).

To control cell-media interactions, a 4x4 microfluidic parallel cell culture array has been designed and fabricated (Figure 2A). Each of the 16 culture chambers has microfluidic inlets and outlets that geometrically control the flow rate and type of media in each cell culture chamber. Reagent concentration is varied along one axis of the array, while the flow rates are varied along the other axis. The system is fabricated out of multilayer polydimethylsiloxane (PDMS) on glass and includes an on-chip diluter to generate a range of concentrations. We have cultured murine fibroblasts in a similar PDMS-on-glass environment at comparable flow rates (Figure 2B).

This microfabricated system will serve as an enabling technology that can be used to control the cellular microenvironment in precise and unique ways, allowing us to do novel cell biology experiments at the microscale.

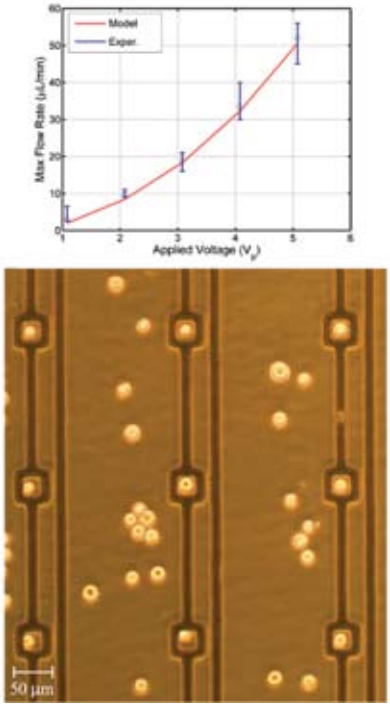

Figure 1: DEP trapping results. A. Maximum flow rate for trapped beads compared to our modeling predictions [2]. B. Trapping of murine fibroblasts in a 3x3 array.

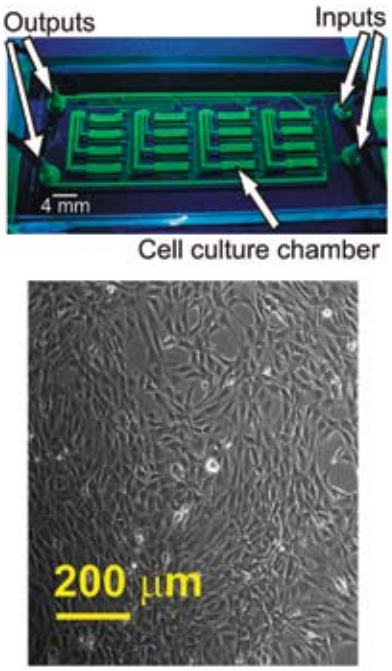

Figure 2: Parallel cell culture on chip. A. Microfluidic 4x4 array of cell culture chambers for creating a range of flow rate and reagent concentration conditions. B. 3T3 fibroblast perfusion culture on a comparable chip.

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Development of Microfluidic Channels for Endothelial Cell Chemotaxis

C.Y. Park, C.F. Dewey Jr
Sponsorship: NIH

Many cells have the ability to sense the direction of external chemical signals and respond by polarizing and migrating toward chemoattractants or away from chemorepellants. This phenomenon, called chemotaxis, has been shown to play an important role in embryogenesis, neuronal growth and regeneration, immune system response, angiogenesis, and other biological phenomena.[1] In addition, cell migration is also important for emerging technologies, such as tissue engineering and biochemical implants.[2] This simple behavior is apparently mediated by complex underlying diffusion and migration mechanisms that have been the focus of many studies and models. These mechanisms may be studied by various chemotactic assays. There have been several chemotaxis assay chambers developed in the past. The most widely used is the Dunn chamber.[3] The drawback of this chamber is that the cells that are squeezed between the cover glass and the chamber walls might release toxic enzymes and organells, and their effect, if any, on the viable neighborhood cells can not be easily quantified. Additionally, the linear gradient of chemokines lasts only 1 to 2 hours. The Whitesides group at Harvard designed a chemotaxis assay chamber using soft lithography.[4] They incorporated several serial mixers to generate multi-profile chemical gradient. This chamber can generate gradient with a simple linear or complex profile without limit in time, but it needs continuous flow to maintain gradient in the direction normal to gradient direction, which is not physiological.

A novel chemotaxis chamber using diffusion characteristics to develop a chemotactic gradient has been developed.[5] This chamber generates a stable and linear gradient along a narrow channel without limitation in time and unnecessary physical stresses. The chamber has 2 inlet ports for 2 kinds of solutions and 1 outlet. One of the input solutions is mixed with a growth factor, and the other solution is mixed with a fluorescent dye or microspheres to verify that there is no bypass flow through the cross channel that supports diffusion. There are two main channels through which the input solutions flow and one narrow cross channel that connects the two main channels, into which a growth factor diffuses from one main channel by diffusion.

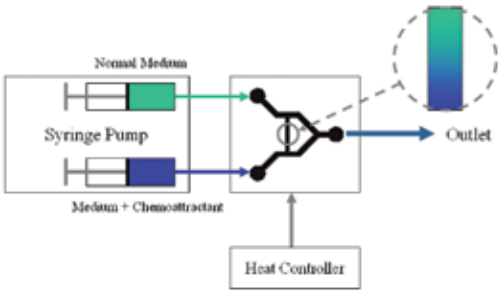

Figure 1: Diagram of experimental setup using syringe pump

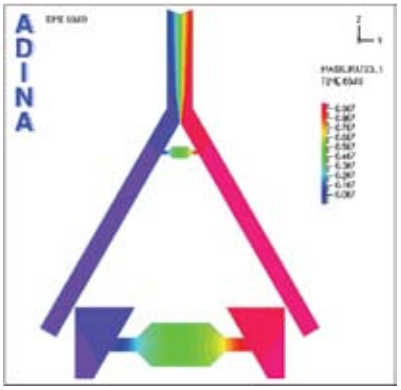

Figure 2: Numerical simulation of diffusion profile across the cross channel

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A Microfabricated Sorting Cytometer

B. Taff, S. Desai, J. Voldman
Sponsorship: NSF Graduate Fellowship, NIH NCRR

This research involves the development of a microfabricated sorting cytometer for genetic screening of complex phenotypes in biological cells (Figure 1). Our technology combines the ability to observe and isolate individual mutant cells from a population under study. The cytometer merges the benefits of both microscopy and flow-assisted cell sorting (FACS) to offer unique capabilities on a single technology platform. Biologists will be able to use this platform to isolate cells based upon dynamic and/or intracellular responses, enabling new generations of genetic screens.

We are implementing this technology by developing an array of switchable traps that rely upon the phenomena known as dielectrophoresis (DEP) [1,2]. The DEP-enabled traps allow for capturing and holding cells in defined spatial locations, and subsequently, releasing (through row-column addressing) a desired subpopulation for further study. Using DEP, non-uniform electric fields induce dipoles in cells that, in turn, enable cellular manipulations. At present, no scalable DEP-based trap configuration exists that can robustly capture single cells and is also amenable to high-throughput microscopy. Such a platform requires performance characteristics that can only be met through quantitative modeling. We have undertaken much of the front-end work necessary for such a system and are continuing our efforts to realize this desired functionality.

To date, we have developed second-generation trap geometries implemented in 4x4 trap arrays (Figure 2) to compare our front-end simulation-based modeling with the performance of actual devices. We have designed, fabricated, and tested both n-DEP (cells held at electric-field minima) and p-DEP (cells positioned at electric-field maxima) based configurations [3]. Our first design and test iteration demonstrated partial functionality and first-order proof of concept, while offering insight for future design improvements. We are also investigating the effects of DEP trapping on cell health and the impact that it may have on our ability to assess specific complex phenotypic behaviors.

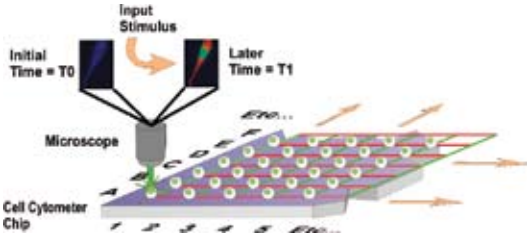

Figure 1: A sorting cytometer for screening complex phenotypes. The cytometer consists of a two-dimensional array of traps, each of which holds a single cell. After loading the traps, the array is optically interrogated, and cells with phenotypes of interest are sorted. In this case, the putative screen is for cells exhibiting altered kinase activation. Such a mutation would dynamically and spatially alter associated intracellular fluorescent responses.

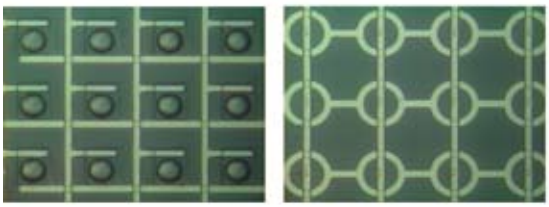

Figure 2: Fabricated traps. Left shows a Nomarski image of the n-DEP trap configuration in plan view, while right shows the ring-dot geometries of the p-DEP layout

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Vacuum Sealing Technologies for Microchemical Reactors

K. Cheung, K.F. Jensen, M.A. Schmidt
Sponsorship: ARO MURI

Current portable power sources may soon fail to meet the increasing demand for larger and larger power densities. To address this concern, our group has been developing MEMS power generation schemes that are focused around fuel cells and thermophotovoltaics. At the core of these systems is a suspended tube microreactor that has been designed to process chemical fuels [1]. Proper thermal management is critical for high reactor efficiency, but substantial heat loss is attributed to conduction and convection through air, as shown in Figure 1. A straightforward solution is to eliminate the heat loss pathways associated with air by utilizing a vacuum package. We are exploring a glass frit bonding method for vacuum sealing.

The leading cause of failure for a glass frit hermetic seal is large voids that are formed in the frit while bonding [2]. Progress has been made toward the optimization of presintering and bonding parameters to reduce or eliminate void formation. A vacuum package of 150 mTorr was obtained after optimization, but became leaky shortly after. An alternate packaging method using a two-step bond process, inspired by [3], was devised and developed. Recent experiments of the process, depicted in Figure 2, show that the initial box bond is capable of producing a hermetic seal. Enhancements through the incorporation of non-evaporable getters will be assessed once a vacuum package is achieved.

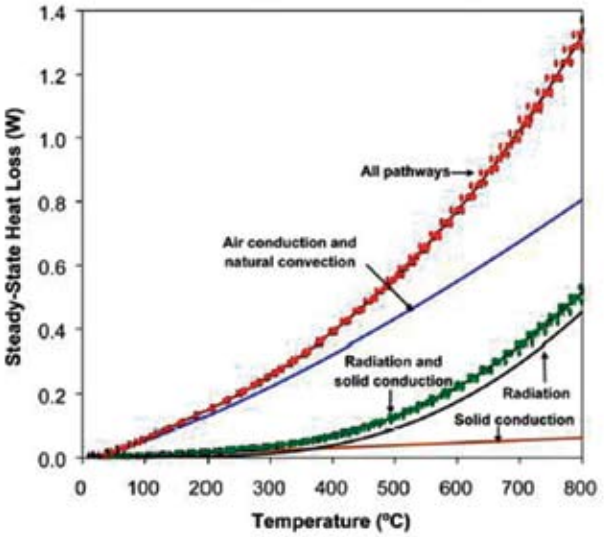

Figure 1: Experimental data for the heat loss of a suspended tube microreactor as a function of temperature in atmosphere (red) and in vacuum (green), plotted with the heat loss components through air, radiation, and solid conduction (blue, black, and orange respectively) [1]

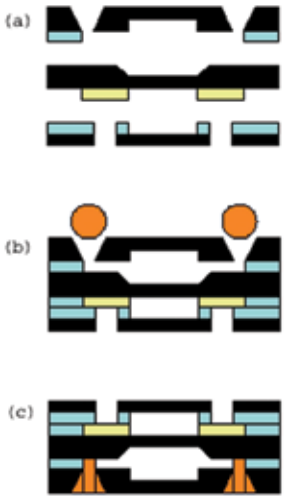

Figure 2: Basic concept of the two-step approach (a) initial bond in box furnace (blue = frit, black = silicon, yellow = metallization) (b) place solder/frit (orange) into pump-out hole, and (c) final seal-off

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Scaled-out Multilayer Microreactors with Integrated Velocimetry Sensors

N. de Mas, A. Günther, T. Kraus, M.A. Schmidt, K.F. Jensen
Sponsorship: MIT Microchemical Systems Technology Center

Microreactors are a new class of continuous reactors, with feature sizes in the submillimeter range, which have emerged over the last decade and, for a number of applications, present capabilities exceeding those of their macroscale counterparts. Unlike conventional reactors, the throughput of microreactors is increased by "scale-out," i.e., operating a large number of identical reaction channels in parallel under equal reaction conditions. We have developed a scaled-out gas-liquid microreactor, built by silicon processing, which consists of three vertically stacked reaction layers, each containing twenty reaction channels. The reaction channels are operated in parallel from single gas and liquid feeds with a liquid volumetric throughput of 80 mL/h. Gas and liquid are introduced to the device through single inlet ports, flow vertically to each reaction layer, and are distributed horizontally to the reaction channels via individual auxiliary channels that provide a significantly larger pressure drop than that across a single reaction channel. These auxiliary channels eliminate cross-talk between reaction channels and ensure uniform flow distribution. The product mixture flows out of the device through a single outlet port. The design rationale of the scaled-out microreactor is illustrated in Figure 1. It is based on flow visualization studies and pressure drop measurements, obtained in a single channel, with the same channel geometry as the reaction channels of the scaled-out device (triangular cross section, channel width = 435 μm, channel length ~ 20 mm) [1]. A photograph of the scaled-out unit is presented in Figure 2. Flow visualization by pulsed-fluorescence microscopy across the top reaction layer reveals that the same flow regime is present in all channels. To further validate the reactor design and monitor flows during continuous operation, pairs of integrated multiphase flow regime sensors are integrated into the device [2]. Comparable slug velocities are measured across the reaction layers.

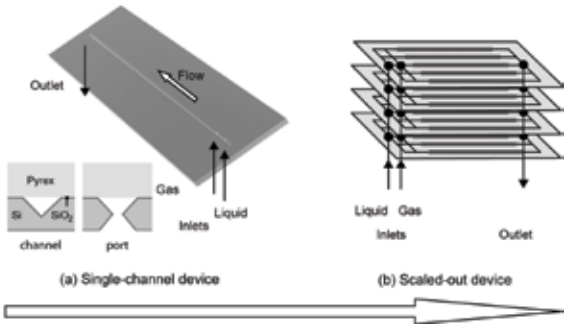

Figure 1: (a) Single-channel device (drawn to scale) formed in silicon and capped by Pyrex (Pyrex not shown). (b) Schematic of scaled-out device with several reaction layers and a large number of channels operating in parallel.

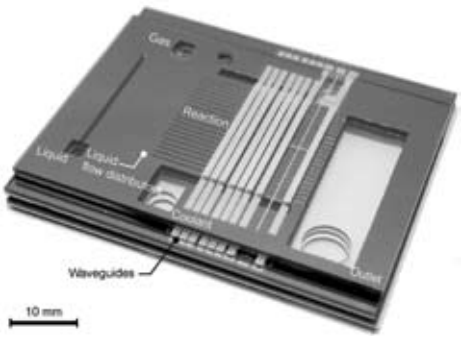

Figure 2: Scaled-out multilayer microreactor with three pairs of flow regime optical sensors, each integrated into the top and middle reaction layers. All channels are formed in silicon by nested potassium hydroxide etching and capped by silicon–Pyrex anodic bonding. The Pyrex layers are used as waveguides.

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Multiphase Transport Phenomena in Microfluidic Systems

A. Günther, S.A. Khan, B.H.K. Yen, M.A. Schmidt, K.F. Jensen
Sponsorship: MIT Microchemical Systems Technology Center

Microscale multiphase flows (gas-liquid and liquid-liquid) possess a number of unique properties and have applications ranging from use in microchemical synthesis systems to heat exchangers for IC chips and miniature fuel cells. Our work is focused on gas-liquid flows in microfabricated channels of rectangular or triangular cross section. We characterize the phase distribution and pressure drop of such flows and apply such information to a systematic design of gas-liquid microchemical reactors. The inherently transient nature of such multiphase flows provides a rich variety of flow regimes and dynamic flow properties. Characterization is done using pulsed-laser fluorescence microscopy and confocal microscopy (spinning disk and scanning), as well as by integrated flow regime sensors. Superficial gas and liquid velocities were varied between 0.01-100 m/s and 0.001-10 m/s, respectively.

Particular attention is given to segmented (slug or bubbly) flows in hydrophilic channels. Figure 1a illustrates the distribution of gas and liquid in the channel. Gas bubbles are surrounded by thin liquid films (thickness ~ 1μm) at channel walls and liquid menisci in the corners. Such flows create a recirculation in the liquid segments (Figure 1b) and can, therefore, be used to efficiently mix two miscible liquids on the microscale within a length of only a few tens of the microchannel width [1,2]. We demonstrate that the transient nature of gas-liquid flows can be used to significantly improve mixing of miscible liquids compared with existing methods. After mixing is accomplished–Figure 2 (bottom) provides an illustration for mixing of two differently colored streams–the gas can be removed from the mixed liquid phase in a capillary phase separator for arbitrary velocities and flow patterns [1]. In addition to providing mixing enhancement, segmented flows narrow the distribution of residence times of fluid elements in the liquid phase, as compared to single-phase flows [1]. A narrower residence time distribution is particularly essential for particle synthesis on a chip.

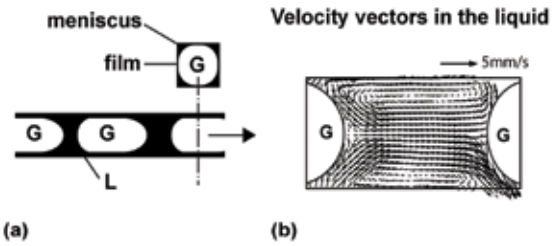

Figure 1: Segmented gas-liquid flow. (a) Gas-liquid phase distribution and (b) liquid phase velocity field obtained by microscopic particle image velocimetry (PIV). The mean velocity was subtracted from all velocity vectors to illustrate the recirculation motion in the liquid segment.

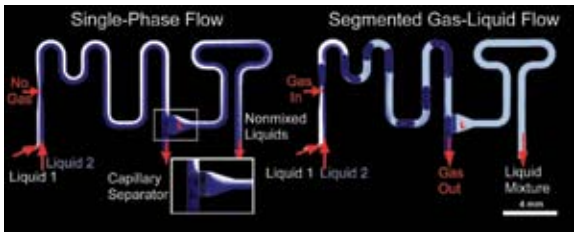

Figure 2: Illustration of enhanced liquid mixing in a microfluidic device by introducing a gas phase. Fluorescence micrographs show (a) the co-flowing liquid streams, L_1 and L_2, without the introduction of a gas phase, G, and (b) mixing in segmented gas-liquid flow and separation of the gas from the liquid in a single-stage microfluidic device.

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Integrated Microreactor System

H.R. Sahoo, E.R. Murphy, N. Imlinger, A. Günther, N. Zaborenko, K.F. Jensen
Sponsorship: Deshpande Center for Technological Innovation

Individual microreactors have been fabricated for many different chemical reactions, but the development of microreaction technology will require combining separation with microreactors to enable multi-step synthesis. The realization of integrated microchemical systems will revolutionize chemical research by providing flexible tools for rapid screening of reaction pathways, catalysts, and materials synthesis procedures, as well as, faster routes to new products and optimal operating conditions. Moreover, such microsystems for chemical production will require less space, use fewer resources, produce less waste, and offer safety advantages. The need for synthesizing sufficient quantities of chemicals for subsequent evaluation dictates that microchemical systems are operated as continuous systems. Such systems require fluid controls for adjusting reagent volumes and isolating defective units. The integration of sensors enables optimization of reaction conditions, as well as, the extraction of mechanistic and kinetic information.

We are developing integrated microchemical systems that have reactors, sensors, and detectors with optical fibers integrated on one platform. New approaches for connecting modular microfluidic components into flexible fluidic networks are being explored. Real-time control of reaction parameters, using online sensing of flowrate, temperature, and concentration, allows for precise attainment of reaction conditions and optimization over a wide range of temperatures and flow-rates. The multiple microreactors on the system can be used together to give higher throughputs or they can be used independently to carry out different reactions at the same time. Figure 1 shows a schematic of an integrated microreactor platform along with an early stage microreactor "circuit board" [1].

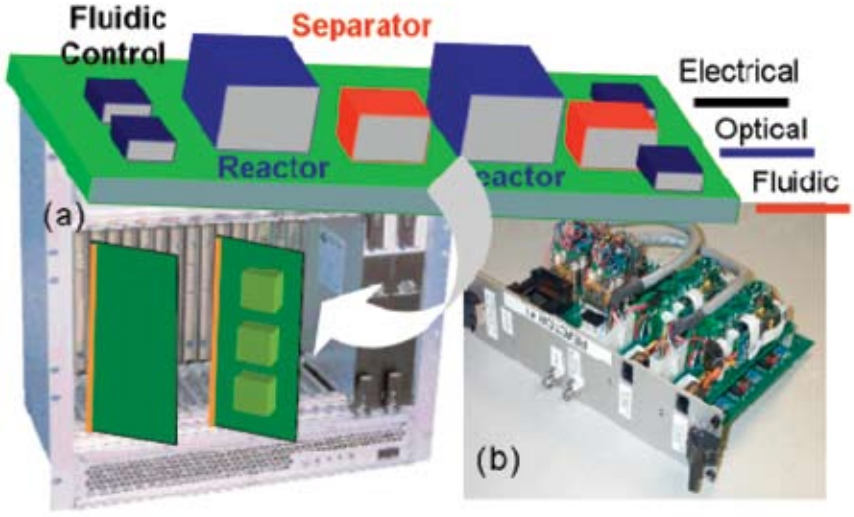

Figure 1: Schematic of an integrated microreactor platform along with an early stage microreactor "circuit board" [1]

REFERENCES:

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Micro Gas Analyzer

L.F. Velásquez–García, L.Y. Chen, L. Lebel, A.I. Akinwande, M.A. Schmidt
Sponsorship: DARPA

The US Department of Defense is currently interested in developing the technology to sense, in real time, deployable agents used in chemical warfare. The Micro Gas Analyzer Project (MGA) is the result of this interest, and aims to develop a portable sensor of wide rage and robustness. Current state-of-the-art technology involves bulky equipment (not portable), high power consumption due to the use of thermionic sources and impact ionization mechanisms, high voltage (in the kilovolt range), and long processing times. Thus, the project has a number of key technological challenges, such as the enhancement of the state-of-the-art sensitivity and specificity capabilities, power consumption reduction, and portability, while keeping the processing time below two seconds.

The MGA is composed of an ionizer (a CNT field ionization array / CNT field emission array), a mass filter (a micro quadrupole mass spectrometer -μQMS), an ion counter/multiplier, an electrometer/mass detector, and a pumping system (passive – absorption pump/active – piezoelectric pump). A schematic of the MGA system is shown in Figure 1. The goal is to make low vacuum (in the millitor range), ionize the species inside the gas using the CNT arrays, filter them with the quadrupole, and then, sense them with the electrometer. The project team is composed of MIT (Ionizer, μQMS, μPump, Valves), University of Texas (Ionization, μPump), Cambridge University (Ion Counter), and Raytheon/CET (System Integration).

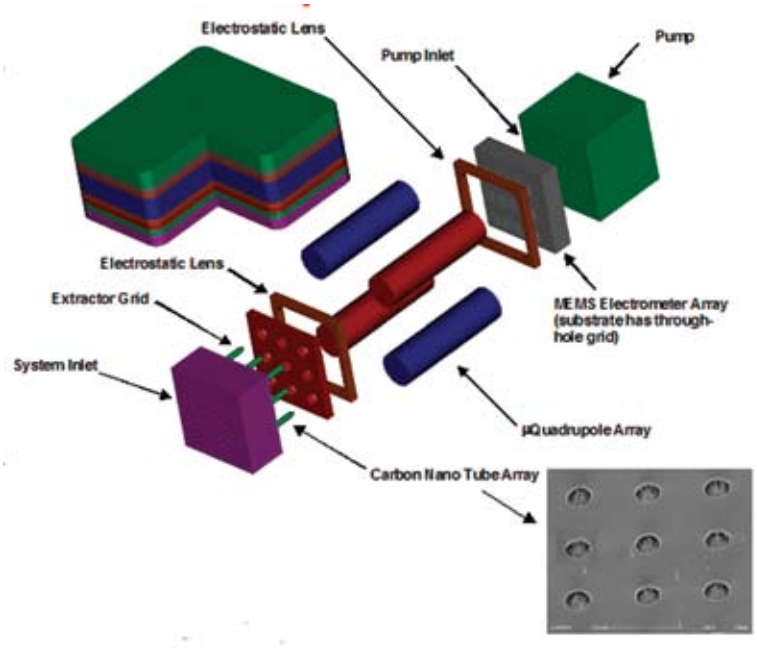

Figure 1: Schematic of the Micro Gas Analyzer

Micro Quadrupole Mass Spectrometer

L.F. Velásquez–García, L. Lebel, A.I. Akinwande
Sponsorship: DARPA

One of the subsystems of the Micro Gas Analyzer Project is a mass filter. The purpose of this filter is to select the kind of species that will be sensed downstream by the electrometer. A microfabricated quadrupole mass filter array is being developed for this purpose where a confining potential sorts the unwanted species (Figure 1). Both high sensitivity and high resolution are needed over a wide range of ion mass-to-charge ratios, from 20 to 200 atomic mass units, to achieve the versatility and resolution that are intended for the program. In order to achieve the high resolution and sensitivity, multiple micro-fabricated quadrupoles, each with specific geometrical parameters, are operated in conjunction with each other.

From a theoretical point of view, the Mathieu equations describe the dynamics of a particle inside the quadrupole. These equations predict a series of stability regions (Figure 2). Each stability region has its own strengths, such as: less power consumption, less operational voltage, or more sensitivity. For example, lower stability zones are used to improve ion transmission, whereas, higher stability zones are used to improve the selectivity of the filter. Therefore, we plan to explore the stability regions of the Mathieu equations to optimize our design. Two sets of variable voltage sources are needed for the mass filter to operate properly, with voltages ranging between 20 and 200 V, at frequencies of 250 and 500 MHz. We plan to try three different approaches to build the device: LIGA (a german acronym for the process that generates high aspect ratio metallic structures), rods assembled using micro-fabricated deflection springs [1], and rod mounts made with KOH [2]. The device has a cross-sectional area of 20 mm^2. The aperture of the individual quadrupoles ranges from 10 to 100 microns.

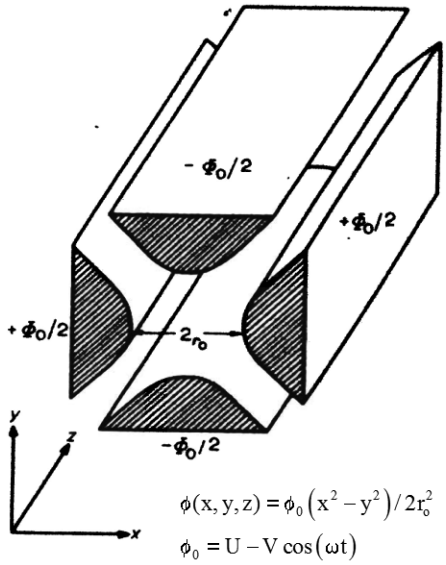

Figure 1: Electric potential inside a quadrupole. The electrodes of a quadruple are ideally hyperboloid surfaces, but quadruple implementations with circular rods perform satisfactorily.

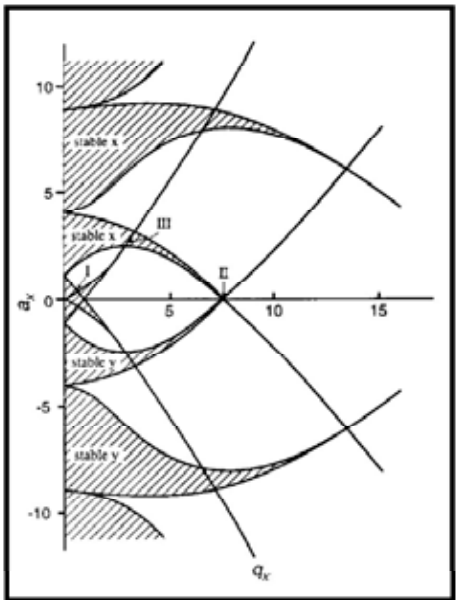

Figure 2: Stability regions of the Mathieu equations. The intersection of the x-stability and y-stability regions determines the possible parameters a and q where the trajectories of a charged particle traveling through a quadrupole is stable.

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Design Tools for Bio-Micromachined Device Design

C. Coelho, N. Ngoc Son, D. Vasilyev, J. Han, J. Peraire, N. Hadjiconstantinou, J. Voldman, J. White
Sponsorship: SMA, NSF

Using micromachining for biological applications requires complicated structures such as mixers, separators, preconcentrators, filters, and pumps; and these elements are used to process biomolecules or biological cells. To accelerate the design of these complicated devices, new tools are needed that can efficiently simulate mixing and particle or cell motion in complicated three-dimensional flows. In addition, for microfluidic devices intended for use in molecular separation, the length scales are such that noncontinuum fluid effects must be considered, and therefore, hybrid approaches that combine molecular and continuum models must be developed. Finally, the wide variety of structures being developed implies that generating models for system-level simulation will require efficient simulation combined with automated model extraction [3]. Our recent work in addressing these problems includes: the development of efficient time integration techniques for cells in flow [1], techniques for accurately extracting diffusion constants from measurements [2], and efficient techniques for extracting models from detailed simulations [4].

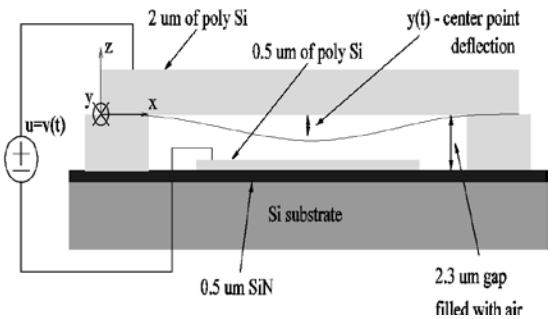

Figure 1: Micromachined clamped-clamped beam example. The input is the applied voltage, the output is the center deflection.

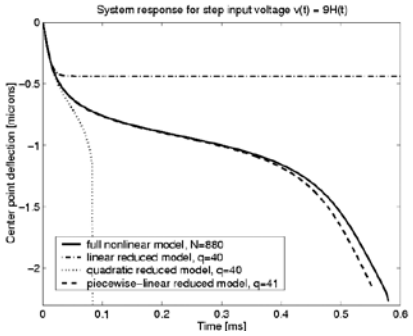

Figure 2: The Trajectory PWL extracted model (dashed line) agrees with the discretized PDE model of the device.

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Microfabricated Solid-Oxide Fuel Cell Systems

B.A. Wilhite, J. Hertz, D. Quinn, J. Cui, K.T. Deshpande, H. Tuller, B. Wardle, J. Ying, M.A. Schmidt, K.F. Jensen
Sponsorship: ARO MURI

Solid-Oxide Fuel Cells (SOFCs), employing ceramic electrolytes, are a promising alternative to low-temperature PEM (proton-exchange membrane) fuel cells for portable power applications. The use of an oxygen-ion conducting electrolyte, operating at high temperatures, offers the potential for internal reforming of a variety of fuels, with improved tolerance to competitively adsorbing species at the anode (e.g. CO); thus, removing the need for pretreatment stages for conversion of hydrocarbon fuel to high-purity hydrogen. However, the appropriate thermal management of this high-temperature fuel cell system is required to achieve an energy-efficient device.

A chip-scale micromembrane architecture has been developed for thermally efficient thin-film applications[1] and has been successfully demonstrated for hydrogen separation via ultra-thin palladium films. Resistive heaters placed directly upon a thermally-isolated membrane allow for rapid heating and cooling of the supported thin film at a minimum expenditure of energy. In addition, the mechanical strength provided by the micromembrane support allows the use of sub-micron films for significant improvement in ion permeability. For these reasons, the micromembrane architecture has been investigated for SOFC development. The extension of this technology is achieved, utilizing a silicon-nitride girder-grid support system to mechanically reinforce the solid-oxide thin films (Figures 1 and 2).

Efforts include: the determination of optimal free-standing fuel cell stack dimensions, integration of individual stacks into a reinforced membrane structure, design of current collectors, and electrical performance tests of fabricated devices. Stability tests of free-standing membranes of varying length scales and aspect ratios are performed for a variety of fuel cell stacks and individual stack layers, with results compared to mechanical models of layered free-standing films. The resulting information is incorporated into the design of a silicon-nitride reinforced free-standing membrane architecture. Lastly, microdevice testing stations allow for performance studies of prototype microdevices.

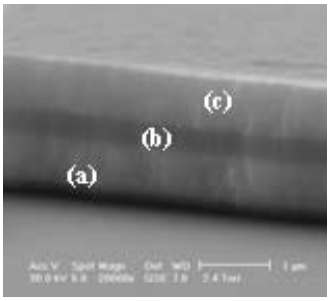

Figure 1: Cross section of ESEM image of solid-oxide fuel cell stack, comprised of (a) co-sputtered Pt-8%Y_2O_3-Zr_2O_3(YSZ) anode, (b) reactively sputtered YSZ electrolyte, and (c) co-sputtered Pt-YSZ cathode.

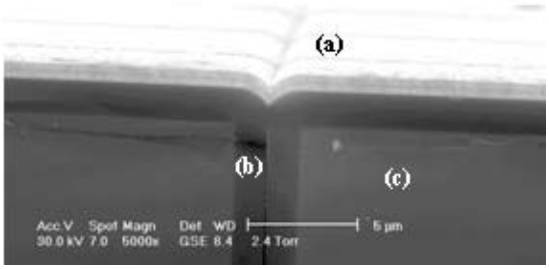

Figure 2: Cross section of ESEM image of (a) solid-oxide fuel cell stack, supported on (b) silicon nitride girders, formed in single-crystal silicon (c). Subsequent removal of silicon substrate produces free-standing fuel cell membrane.

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Catalytic Micromembrane Devices for Portable High-Purity Hydrogen Generation

K. Deshpande, B.A. Wilhite, S.E. Weiss, J.Y. Ying, M.A. Schmidt, K.F. Jensen
Sponsorship: ARO MURI

The development of portable-power systems employing hydrogen-driven fuel cells continues to garner significant interest in the scientific community, with applications ranging from the automotive industry to personal electronics. While progress has been made in the development of efficient hydrogen-storage devices, it is still preferable for portable-power systems to operate from a liquid fuel with a high energy density (e.g., methanol, ammonia). This necessitates the integration of a hydrogen generator capable of converting stored fuels to hydrogen to drive the fuel cell.

Previous research has focused upon the development of novel catalysts and autothermal microreactor designs for efficient conversion of liquid fuels (e.g. methanol, ammonia) into hydrogen for use by a polymer-electrolyte fuel cell [1]. Additionally, micromembrane devices (Figure 1) have been developed for purification of the resulting hydrogen stream to remove impurities (e.g. CO) that adversely affect fuel cell performance [2]. Our current research aims to integrate (i) catalyst design, (ii) autothermal microreformer design, and (iii) micromembrane technology to realize microscale chemical systems capable of producing high-purity hydrogen for fuel cell operation. By combining microfabrication techniques for generation of micromembrane devices with wet-chemical deposition methods for a variety of catalysts, multiple membrane reactor applications for hydrogen generation can be realized, taking full advantage of superior mass transport and film permeabilities achievable at the microscale. Results obtained for $LaNi_{0.95}Co_{0.05}O_3$ perovskite catalysts integrated with 23 wt% Ag-Pd membranes (Figure 2) demonstrate promising high-purity hydrogen yields at low methanol feed compositions, and demonstrate the applicability of catalytic membrane reactors effected at the microscale for efficient production of high-purity hydrogen. Resulting microdevices are directly applicable as part of an integrated portable-power system.

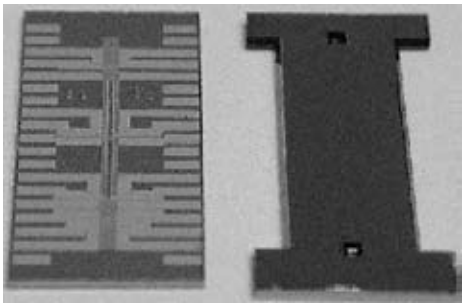

Figure 1: The micromembrane device, which provides a robust platform for the study of multiple thin-film applications.

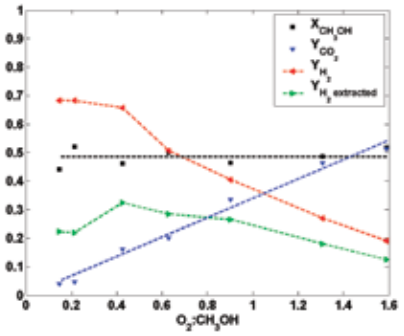

Figure 2: Results for 23 wt% Ag-Pd film (0.2 μm) coated with 1.7 mg of $LaNi_{0.95}Co_{0.05}O_3$ / Al_2O_3 catalyst for varying O_2:CH_3OH feed ratio at 400°C.

REFERENCES:

[1] Arana, L.R., S.B. Schaevitz, A.J. Franz, M.A. Schmidt, K.F. Jensen, "A Microfabricated Suspended-Tube Chemical Reactor for Thermally Efficient Fuel Processing," *Journal of Microelectromechical Systems.*, vol. 12, pp. 600-612, 2003.

[2] Wilhite, B.A., M.A. Schmidt, K.F. Jensen, "Palladium-Based Micromembranes for Hydrogen Separation: Device Performance and Chemical Stability," *Ind. Eng. Chem. Res.*, vol. 43, pp. 7083-7091, 2004.

Thermal Management in Devices for Portable Hydrogen Generation

B. Blackwell, M.A. Schmidt, K.F. Jensen
Sponsorship: ARO MURI

As power requirements of portable electronic devices continue to increase, the development of an efficient portable power generation scheme has remained an active research area. Specifically, hydrogen-driven fuel cells have received significant attention. This work focuses on microreaction technology for the conversion of fuel to electrical power. Emphasis has been placed on developing microreactors for high-purity hydrogen production. Critical issues in realizing high-efficiency devices capable of operating at high temperatures have been addressed: specifically, thermal management, the integration of materials with different thermophysical properties, and the development of improved packaging and fabrication techniques.

A microfabricated suspended-tube reactor (Figures 1, 2) has been developed for efficient combustion and reforming of chemical fuels.[1] The reactor, designed specifically to thermally isolate the high-temperature reaction zone from the ambient, consists of thin-walled U-shaped silicon nitride tubes formed by deep reactive ion etching (DRIE) and subsequent nitride deposition via chemical vapor deposition (CVD). Thin-film platinum resistors are integrated into the reactor for heating and temperature sensing. Detailed thermal characterization demonstrates reactor operation up to 900ºC and quantifies heat losses. Additionally, this high-temperature microcombustor is applicable for thermophotovoltaic generation.

A new fabrication scheme for the suspended-tube reactor incorporates wet potassium hydroxide (KOH) etching, an economical and time-saving alternative to DRIE]. In this design, pre-fabricated thin-walled glass tubes replace the silicon nitride tubing to provide inlet and outlet conduits. The thermal conductivity of the resulting tubes is 50% lower than that of silicon nitride. Hence, this technique allows for the incorporation of robust tubing, while maintaining thermal efficiency.

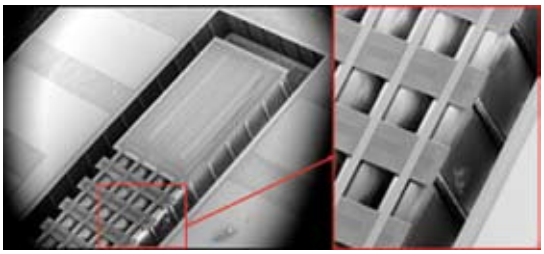

Figure 1: SEM of suspended tube reactor showing four SiN_x tubes, the suspended Si reaction zone with integrated Ti/Pt heater, and temperature-sensing resistor, and Si slabs thermally linking the four tubes.

Figure 2: Photograph of suspended tube reactor during hydrogen combustion. The suspended Si reaction zone glows (~800C) whereas the surrounding area remains cool.

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Materials and Structures for a MEMS Solid Oxide Fuel Cell

D. Quinn, P. Capozzoli, N. Wicks, N. Yamamoto, S.M. Spearing, B.L. Wardle, in collaboration with B.A. Wilhite, J. Hertz, K. Deshpande, K.F. Jensen, H. Tuller
Sponsorship: ARO MURI

Microfabricated solid oxide fuel cells are currently being investigated for portable power applications requiring high energy densities [1, 2]. Reducing the thickness of fuel cell stack materials improves the electrochemical performance versus traditional devices. This motivation for thinner structures, combined with significant temperature excursions during processing and operation (~600 – 1000 °C), presents the thermomechanical stability of such membranes as a major challenge. A buckled electrolyte/SiN thin film is shown in Figure 1. The prediction and management of structural stability (buckling) and failure require accurate knowledge of many parameters including: thermomechanical properties, residual stress, and fracture strength.

Our group has characterized the residual stress and microstructure of the electrolyte layer of the fuel cell stack. Residual stress in sputter-deposited yttria stabilized zirconia (YSZ) thin films (5nm – 1000nm thickness), as a function of deposition pressure and substrate temperature, has been completed [3]. The results indicate variations in intrinsic stress from ~0.5GPa compressive to mildly tensile (~50 MPa) (Figure 2). Changes in microstructure are subsequently characterized using X-ray diffraction of as-deposited and annealed films and correlated with relevant mechanisms/models of residual stress evolution. Frameworks for using such residual stress data to design mechanically stable membranes for μSOFC devices have also been developed.

Current research areas include: continued microstructural and residual stress characterization under thermal cycling, elastic/fracture properties characterization, design and fabrication of thermomechanically stable fuel cell stacks, exploration of proton conducting solid oxide thin films for lower-temperature operation, investigation of the mechanical properties of anode and cathode materials, and nonlinear modeling of film postbuckling and failure.

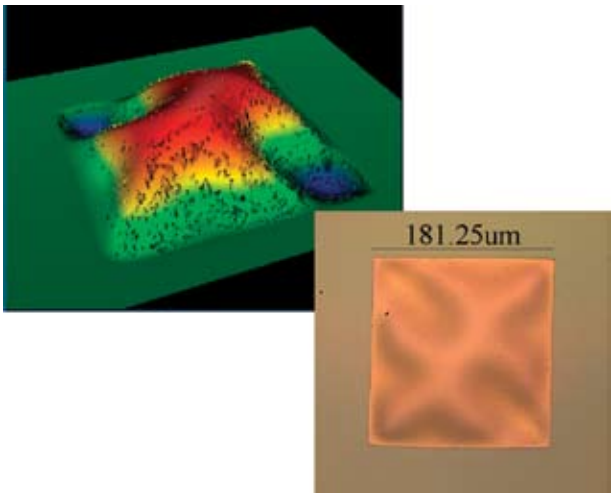

Figure 1: Postbuckled YSZ/SiN membranes on Si. Displacement contour plot (top) and top-down view (bottom).

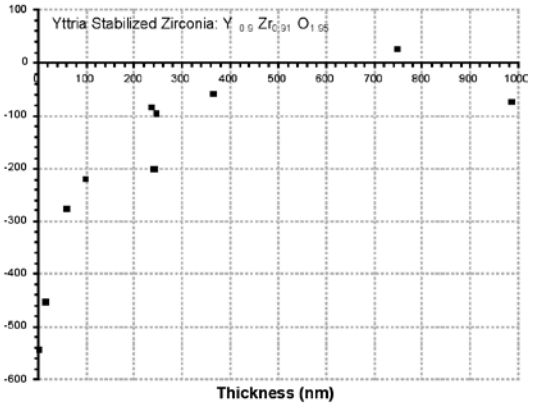

Figure 2: YSZ electrolyte film stress as a function of film thickness.

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Microfabricated Proton-Conducting Solid Oxide Fuel Cell System

K.T. Deshpande, J. Cui, B.A. Wilhite, J. Ying, M.A. Schmidt, K.F. Jensen
Sponsorship: ARO MURI

Owing to their high efficiency and energy density, miniaturized fuel cells are an attractive alternative to batteries in the mW-W power generation market for portable consumer and military electronic devices [cf. 1-3]. Hydrogen is being actively considered as a fuel for power generation. It can be supplied either by storage devices or its in-situ generation using reformers. However, safety and reliability issues persist with current storage choices, such as zeolites and carbon nanotubes [4]. For these reasons, fuel cells based on direct fuel reforming are advantageous. The processes typically involve either high temperature reforming of fuel to hydrogen combined with a low temperature Proton exchange membrane (PEM) fuel cell, which implies significant thermal loss. Alternatively, fuel reforming can be combined with solid oxide fuel cells capable of operating at high temperatures.

Typical components of a solid oxide fuel cell include electrodes and an electrolyte. Typically ZrO_2, CeO_2, and $LaGaO_3$, which are oxide ion conductors are used as separator materials [5]. However, one of the disadvantages of these materials is the need for operation at high temperatures (~700°C). These operating temperatures, in turn, lead to associated problems of materials compatibility and low tolerance with respect to variations in operating conditions. As an alternative, proton conducting solid oxide membranes, typically alkaline earth metal substituted perovskites, such as $BaCeO_3$, $SrCeO_3$, and $BaZrO_3$, exhibit high protonic conductivity even at 400°C [6].

In the current research, we explore the possibility of fabricating a fuel cell using these low temperature electrolytes. Previous work on Pd-based membranes on MEMS-supported membranes indicates that hydrogen yields up to 93% can be achieved for methanol using $LaNiCoO_3$ anode catalyst at 475°C. We plan to extend this concept further to prepare a complete fuel cell assembly and test its performance.

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Thermophotovoltaic (TPV) MEMS Power Generators

O.M. Nielsen, K.F. Jensen, M.A. Schmidt
Sponsorship: ARO MURI

Batteries have, for a number of years, not kept up with the fast development of microelectronic devices. The low energy densities of even the most advanced batteries are a major hindrance to lengthy use of portable consumer electronics, such as laptops, and of military equipment that most soldiers carry with them today. Furthermore, disposing of batteries constitutes an environmental problem. Hydrocarbon fuels exhibit very high energy densities in comparison, and micro-generators converting the stored chemical energy into electrical power at even modest levels, are, therefore, interesting alternatives in many applications. This project focuses on building thermophotovoltaic (TPV) micro-generators, in which photocells convert radiation from a combustion-heated emitter, into electrical power. TPV is an indirect conversion scheme that goes through the thermal domain and therefore, does not exhibit very high efficiencies (10-15% max). However, because of its simple structure and because the combustor and photocell fabrication processes do not need to be integrated, the system is simpler to micro-fabricate than other generator types (e.g. thermoelectric systems and fuel cells). It is also a mechanically passive device that is virtually noiseless and less subject to wear than engines and turbines. In this TPV generator, a catalytic combustor, the suspended micro-reactor (Figure 1) is heated by combustion of propane and air, and the radiation emitted is converted into electrical energy by low-bandgap (GaSb) photocells (Figure 2). Net power production of up to 1 mW has been achieved [1], constituting a promising proof of concept. Work is underway to build a new micro-reactor more suited for the needs of TPV than the original design.

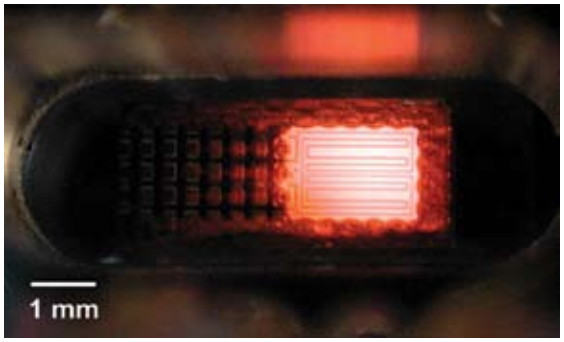

Figure 1: Suspended micro-reactor for fuel processing and TPV energy conversion.

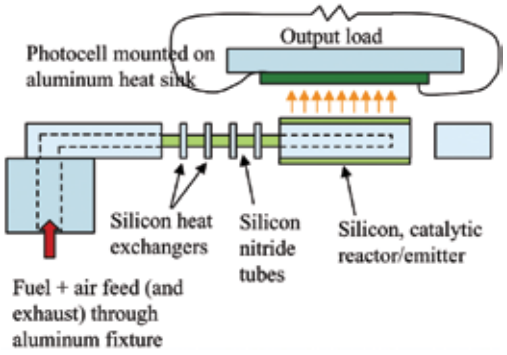

Figure 2: Suspended micro-reactor with photocell in TPV micro-generator configuration.

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Thermoelectric Energy Conversion: Materials and Devices

H. Lee, Q. Hao, R.G. Yang, X. Chen, G. Chen, in collaboration with M.S. Dresselhaus (MIT), Z.F. Ren (Boston College), J.-P. Fleurial (JPL)
Sponsorship : NASA, Intel, Nanolab SBIR

Thermoelectric devices based on Peltier effect and Seebeck effect use electrons as a working fluid for energy conversion. These solid-state energy conversion devices have important applications in refrigeration and electrical power generation. Our work follows two directions: nanostructured materials and microdevices.

The efficiency of thermoelectric devices is characterized by the nondimensional thermoelectric figure of merit $ZT = S^2\sigma T / k$, where S is the Seebeck coefficient, σ the electrical conductivity, and k the thermal conductivity of their constituent materials, and T is the average device temperature. Identifying materials with a large ZT has been challenging because of the interdependency of those three properties. With both quantum size effects on electrons and classical size effects on phonons, nanostructures provide an alternative way to engineer thermoelectric properties.[1,2] Our current effort is focused on designing, synthesizing, and characterizing nanostructures in bulk form that can be produced for mass applications. Figure 1 illustrates ballistic phonon transport in a unit cell of a nanocomposite, which leads to low thermal conductivity.[3] We are also working on fabricating micro thermoelectric devices, first using thin film devices such as SiGe alloy and Si-Ge superlattices,[4] and more recently on thick films to reduce parasitic heat losses.[5] In addition, we are also exploring novel microdevice configurations that can improve energy conversion efficiency, by utilizing the hot electron concepts.[6,7]

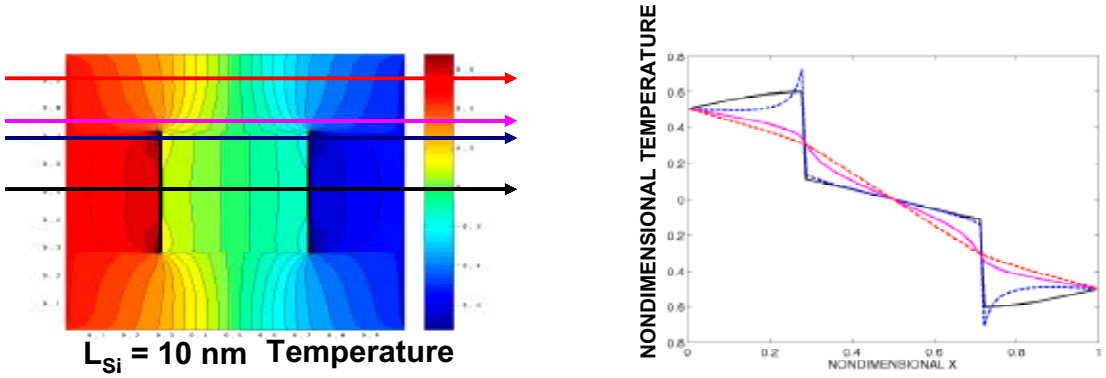

Figure 1: Temperature distributions in one unit cell of two-dimensional periodic structure made of Si nanowires embedded in a Ge matrix.

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Far-Field Spectral Control and Near-Field Enhancement of Thermal Radiation Transfer for Energy Conversion Applications

A. Narayanaswamy, L. Hu, Z. Chen, G. Chen, in collaboration with J.D. Joannopoulos
Sponsorship: ONR, MURI (through UC Berkeley)

The performance of thermophotovoltaic (TPV) energy conversion systems is greatly affected by the radiation characteristics of the thermal emitter. Ideally, one would want a selective emitter with high emissivity above the band gap and low emissivity below the band gap. Various approaches have been proposed to fabricate effective selective emitters with 2D or 3D photonic crystals, which involve considerable intricate microfabrication. Instead, we have proposed a simpler-to-fabricate 1D structure that exhibits many of the features of its 2D and 3D counterparts [1]. The key has been to use ultra thin metallic films arranged as a periodic multilayer stack with a suitable non-absorbing dielectric material in-between. Figure 1 shows the numerical computation of the total hemispherical emissivity of two such structures as a function of wavelength.

In addition to improving the selective emission of thermal radiators, we are also exploring near field effects to improve the energy density and efficiency of thermal-to-electric energy conversion devices. Electromagnetic surface waves, like surface phonon polaritons or surface plasmon polaritons, can increase the energy transfer by two or three orders of magnitude compared to the near-field enhancement between materials that do not support such surface waves. Our work has shown that such enhancements in thermal radiative transfer can not only increase the power density and efficiency of TPV devices [2] but can also contribute to the improvement of thermoelectric devices [3]. We are also exploring a new TPV device structure involving interdigitized hot-and-cold fingers with increased surface area, built-in photon recycling, and potentially built-in spectral control [4]. Experimental work involving microfabrication and device testing is in progress.

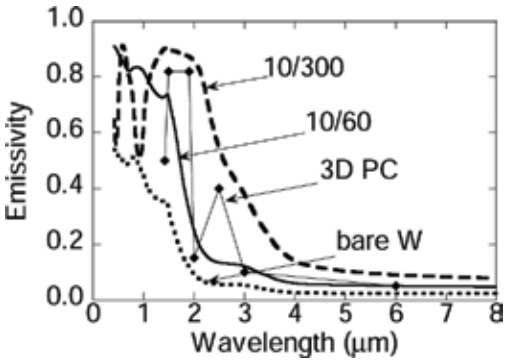

Figure 1: Spectral emissivity of 1D photonic crystal. The curves with legend 10/60 (10/300) refers to 10 nm of tungsten and 60 nm (300 nm) of alumina in each unit cell. For comparison, the emissivity of the 3D photonic crystal1 and bare tungsten are shown.

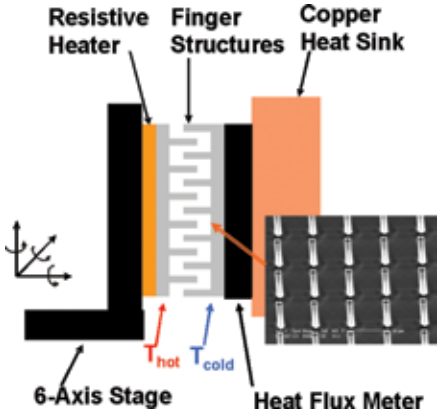

Figure 2: Illustration of the testing rig for the interdigitized thermophotovoltaic device structure. The SEM picture shows one set of figure structures.

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Development of a High Power Density Microscale Turbocharger

N. Savoulides, L. Ho, H. Li, M. Schmidt, C.J. Teo, L. Wang, S. Jacobson, A. Epstein
Sponsorship: ARL

A microscale turbocharger has been fabricated as part of a program to develop a microfabricated gas turbine generator to serve as a battery replacement with seven times the energy density of today's best batteries. The turbocharger will evolve into the gas turbine generator with minimal fabrication process changes. The turbocharger lacks an electric generator, and its turbine and compressor flow paths are independent; otherwise, the two devices are virtually identical. The turbocharger is a test vehicle for developing fabrication processes and turbomachinery/bearing technology. The turbocharger is formed by fusion bonding six silicon wafers. The hatched structure in Figure 1 is the rotor, which is free to spin within the device on hydrostatic gas bearings. The turbocharger has a design rotation rate of 1.2 million rpm and a design compressor pressure ratio of 2.2.

Journal bearing dimensional control is a key challenge: 15 +/- 0.75 μm in width and 330 +/- 5 μm in depth. The bearing width tolerance, which is half that of previous devices in this program, is achieved through refinements in the etch recipe as well as modifications to the masking material profile. The masking material must be carefully controlled because of its finite etch rate and the effects of sidewall-passivation-layer erosion from ions deflected by the resist slope. The journal bearing specification is met on device wafers with a yield of more than 60%. Another challenge for this device is obtaining a rotor blade height uniformity of about 1%, which is critical for low levels of imbalance in the rotor.

A turbocharger has been operated to a rotation rate of 480,000 rpm, which is equivalent to a tip speed of 200 m/s (450 miles per hour). Figure 2 shows the measured compressor pressure ratio for two runs of the same device with different throttle settings. The compressor achieved a pressure ratio of 1.21 with a flow rate of 0.14 g/s at its top speed. The measured pressure and flow characteristics are consistent with the design models for this device.

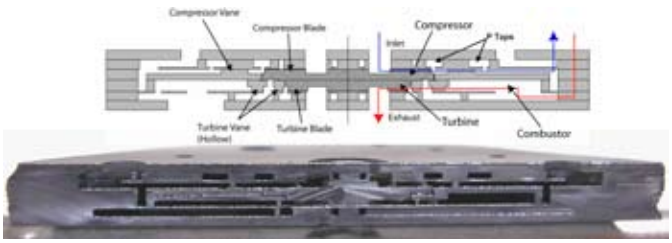

Figure 1: Turbocharger Cross Section: Compressor Rotor Diameter = 8.2 mm, Turbine Rotor Diameter = 6 mm, Die Size = 23 x 23 x 2.9 mm.

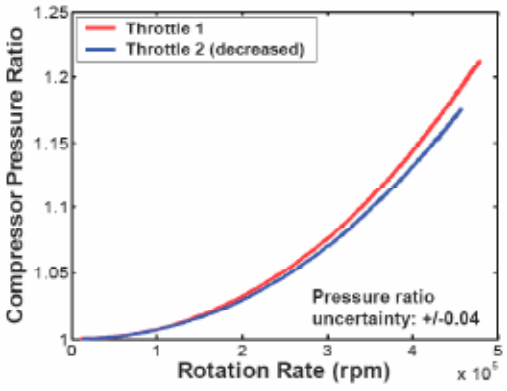

Figure 2: Turbocharger high speed operation.

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A MEMS Electroquasistatic Induction Turbine-Generator

J. Lodewyk Steyn, J.H. Lang, C. Livermore
Sponsorship: DARPA, ARL

Presented here is a microfabricated electroquasistatic (EQS) induction turbine-generator that has generated net electric power. A maximum power output of 192 μW was achieved under driven excitation. We believe that this is the first report of electric power generation by an EQS induction machine of any scale in the open literature. This work forms part of a program at MIT to fabricate a MEMS-scale gas turbine-generator system. Such a system converts the enthalpy of combustion of a hydrocarbon fuel into electric power. For even modest efficiency levels of the gas turbine engine cycle (10-15%), a small gas turbine would be a portable energy source with higher energy density than the best batteries available [1]. In MIT's device, this small engine provides the shaft power needed to drive a small electric generator. Although magnetic machines are preferred at large scales, EQS machines become attractive at small scales, primarily because very small airgaps between the rotor and stator allow higher breakdown electric fields of approximately 10^8 V/m. The generator comprises five silicon layers (Figure 1) fusion bonded together at 700°C. The stator is a platinum electrode structure formed on a thick 20 μm recessed oxide island. The rotor is a thin film of lightly doped polysilicon also residing on an oxide island, which is 10 μm thick. We also present a generalized state-space model for an EQS induction machine that takes into account the machine and its external electronics and parasitics. This model correlates well with measured performance, and was used to find the optimal drive conditions for all driven experiments. Figure 2 shows the results of an experiment under driven excitation. In this particular experiment, 108 μW was generated at 245krpm. Good correlation with the models is observed. In other experiments, self-excited operation was attained. In this case, the generator self-resonates and generates power without the use of any external drive electronics [3].

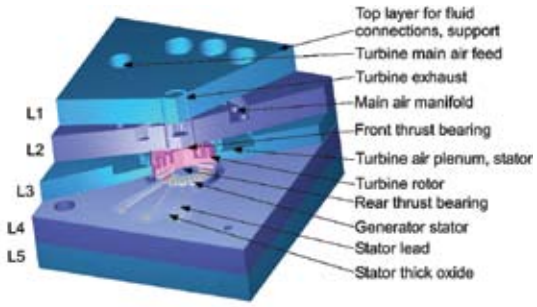

Figure 1: 3D section view of the turbine generator device. The device consists of five silicon layers fusion bonded together. The electric generator is located in Layers 3 and 4 and consists of a stator with 786 electrodes. Every 6th electrode is connected to form a 6-phase machine with 6 sets of 131 electrodes.

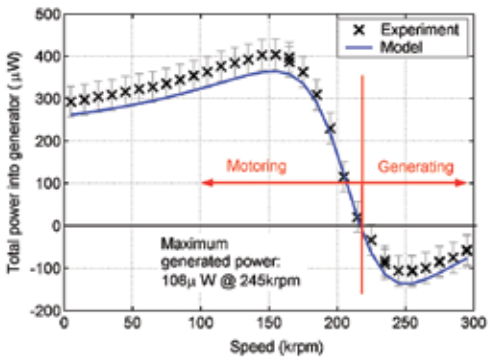

Figure 2: Power output vs. speed for the generator device. This figure shows the sum of the power from all 6 phases of the generator. This curve is typical of an induction machine. As indicated, when the rotating speed is slower than the synchronous speed, it acts as a motor. Beyond the synchronous speed, it acts as a generator.

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Multi-Watt Electric Power from a Microfabricated Permanent-Magnet Generator

S. Das, D.P. Arnold, I. Zana, J.W. Park, J.H. Lang, M.G. Allen
Sponsorship: DARPA, ARL

Presented here are the design, fabrication, and characterization of three-phase permanent magnet (PM) machines that convert 2.3 W of mechanical power and deliver 1.1 W of DC electrical power to a resistive load at a rotational speed of 120,000 rpm. Such microgenerators are an important system-level component of compact MEMS-based power sources, such as combustion-driven or air-driven microengines [1].

The generators are three-phase, eight-pole, synchronous machines, each consisting of a surface-wound stator (Figure 1) and a multi-poled PM rotor (Figure 2(a)). The stator uses three Cu windings that are dielectrically isolated from a 1-mm thick NiFeMo (Supermalloy) substrate by a 3 μm spin-on-glass layer and/or 5 μm polyimide layer. The coils were fabricated using a two-layer electroplating process [2]. They were measured to be 80-120 μm thick and 50-550 μm in width. The microfabricated coils, with their small inter-conductor gaps and variable width geometry, are the key for enabling high power output. The rotor contains an annular SmCo PM and a ferromagnetic FeCoV (Hiperco50) backiron, each 9.525 mm OD, 3.175 mm ID, and 500 μm thick. The SmCo PM and FeCoV backirons were, then, assembled and glued into a pre-formed PMMA cup, which was fit onto a 1.6 mm shaft (Figure 2(b)).

For characterization, a high-speed spinning rotor test stand, incorporating an air-turbine driven spindle, was constructed. The stator was positioned under the rotor using an xyz-micropositioner, which permitted precise (± 5 μm) adjustment of the air gap. A three-phase step-up transformer (1:6 turn ratio) and Schottky diode bridge were used to rectify the output voltage for DC power generation across a load resistor. The power data for the 2-turn/pole machine shows a quadratic dependence on speed for a fixed load (Figure 2(c)) and typical power transfer dependence for varying loads (Figure 2(d)), with a maximum demonstrated power of 1.1 W (2.9 MW/m^3 power density).

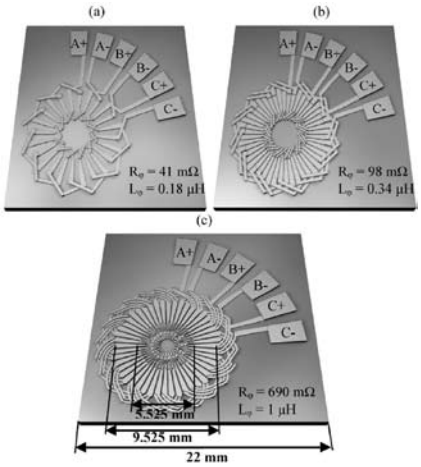

Figure 1: Conceptual drawings of (a) 1-turn/pole, (b) 2-turn/pole, and (c) 4-turn/pole surface wound stators. The measured phase resistance and inductance are indicated for each type.

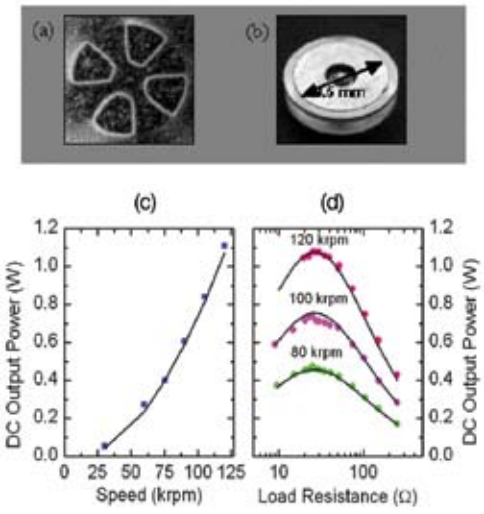

Figure 2: (a) Magnetic pole pattern using magnetic viewing paper and (b) 500 μm thick PM rotor and backiron mounted onto shaft. DC output power across load resistor for 2-turn stator at 100 μm air gap vs. (c) rotational speed for 30 Ω load and (d) load resistance at 80, 100, and 120 krpm.

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High-speed Micro-scale Gas Bearings for Power MEMS

L.X. Liu, C.J. Teo, F. Ehrich, L. Ho, H. Li, S. Jacobson, Z.S. Spakovszky
Sponsorship: ARL

The high-speed micro hydrostatic gas journal bearings used in the high-power density MIT micro-engines are of very low aspect ratio, with a bearing length-to-diameter ratio of less than 0.1, and are running at surface speeds of order 500 m/s. These ultra-short high-speed bearings exhibit whirl instability limits and dynamic behavior very different from conventional hydrostatic gas bearings. The design space for stable high-speed operation is confined to a narrow region and involves singular behavior [1]. The narrow design space together with the limits on achievable fabrication tolerance that can be achieved in the silicon chip manufacturing technology severely affects journal bearing operability and limits the maximum achievable speed of micro turbomachinery. The hydrostatic gas thrust bearings are located near the center of the rotor, and play a vital role in providing axial support for the rotor. The thrust bearing geometry is designed to provide the required axial and tilting stiffness, and ensures stable thrust bearing operation at high-speed [2].

Our technical approach involves the combination of numerical simulations, experiment, and simple, first principles based on modeling of the gas journal and gas thrust bearing flow fields and the rotordynamics. A novel variation of the axial-flow hydrostatic micro-gas journal bearing concept is introduced that yields anisotropy in bearing stiffness [3]. By departing from axial symmetry and introducing biaxial symmetry in hydrostatic stiffness (Figure 1), the bearing's top speed is increased and fabrication tolerance requirements are substantially relieved, making more feasible extended stable high-speed bearing operation. An existing analytical hydrostatic gas journal bearing model [4] is extended and modified to guide the journal bearing design with stiffness anisotropy. In addition, a novel micro gas thrust bearing model is established. High-speed experimental spin tests were conducted in several micro-bearing test devices, and all 11 test devices were spun to high-speed, achieving an average rotor speed of 720,000 rpm. Figure 2 depicts a typical test run, and shows good agreement between the newly established bearing theory and the measurements.

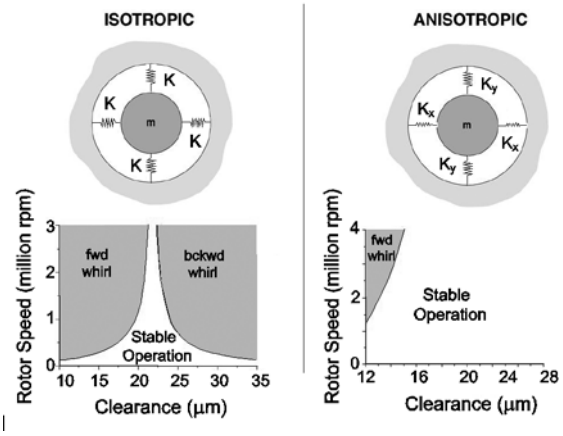

Figure 1: Elimination of singular behavior of whirl instability limit and extension of geometric design space for stable high-speed operation using bearing stiffness anisotropy in ultra-short hydrostatic micro-gas journal bearings [3].

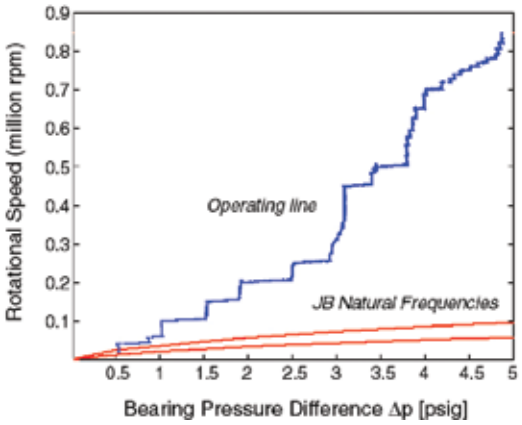

Figure 2: Experimental demonstration of operating schedule for a micro-electrostatic turbine-generator which achieved a maximum speed of 850,000 rpm (93% design speed) [2].

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Piezoelectric Micro Power Generator (PMPG): A MEMS-based Portable Power Device

W. Choi, R. Xia, J. Brewer, S.-G. Kim
Sponsorship: NSF, Korean Institute of Machinery and Materials

A thin-film lead zirconate titanate $Pb(Zr,Ti)O_3$ (PZT), MEMS energy-harvesting device is developed to enable autonomous sensors for in-service integrity monitoring of large scale infrastructures. It is designed to resonate at specific frequencies from external vibrational energy sources, thereby creating electrical energy via the piezoelectric effect. The corresponding energy density of the 1st prototype is 0.74 mW-h/cm^2, which compares favorably to lithium ion batteries. [1] Current efforts are focused on improving the harvest efficiency of the device. A geometric optimization of the cantilever design is made to suppress damping contributions from air and structural dissipation. Additionally, a serpentine cantilever has been designed to achieve a low resonant frequency structure. The dominant contributors to low Q factor at the MEMS scale are air damping and internal structure damping. For 2nd generation PMPG [3], we have optimized the cantilever shape to minimize the damping effect. Analytical modeling of PMPG predicts a 77% decrease of the damping coefficient of a new PMPG device.[4] This reduced damping coefficient enables 4.3 times larger resonance amplitude of the cantilever structure and 10.2 times larger maximum strain of the PZT layer. As a result, power density increases up to 1850% of the old PMPG device at the same footprint. We also designed a serpentine cantilever to achieve a low resonant frequency structure, as well as, a low damping effect, when it resonates. (Figure 2)

PMPG has been integrated with a commercial wireless sensor, Telos, to simulate a self-powered RF temperature monitoring system. Such devices will play an important role in remote sensing network applications. Telos on average consumes 350μJ for 38 ms per measurement. Since PMPG offers limited power, a storage capacitor and a power management module are implemented to power the node at discrete time intervals.

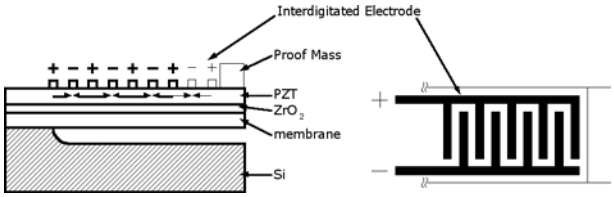

Figure 1: Schematic of 1st generation PMPG

Figure 2: Design of a low resonant frequency serpentine structure

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MEMS Piezoelectric Ambient Vibration Energy Harvesting for Wireless Sensors

N.E. duToit, A. Mracek, B.L. Wardle, in collaboration with W. Choi, S.-G. Kim
Sponsorship: CMI

Recently, numerous investigations have focused on the development of distributed wireless sensor node networks. Power for such devices can be supplied through harvesting ambient environmental energy, available as: mechanical vibrations, fluid motion, radiation, or temperature gradients [1]. Envisioned applications include: building climate control and warehouse inventory control, identification and personalization (RFID tags), structural health monitoring (aerospace and automotive sectors), agricultural automation, and homeland security.

Advances in "low-power" DSP's (Digital Signal Processors) and trends in VLSI (Very Large Scale Integration) system design have reduced power requirements to 10's-100's of μW. These power levels are obtainable through piezoelectric harvesting of ambient vibration energy. Current work focuses on harvesting this energy with MEMS resonant structures. Coupled electromechanical models have been developed to predict the electrical and mechanical performance obtainable from known low-level ambient vibration sources. These models have been validated by comparison to prior published results [2] and tests on a MEMS device. A non-optimized, uni-morph beam prototype (Figure 1) has been designed and modeled to produce 30 μW/cm^3 [3]. A MEMS fabrication process for a prototype device is presented based on past work at MIT [4]. Dual optimal frequencies with equal peak powers and unequal voltages and currents are characteristic of the response of such coupled devices when operated at optimal load resistances (Figure 2).

Future work will explore active sources, such as: aircraft skin for harvestable power, fabrication and testing of the uni-morph prototype beam, and optimization of device configurations for aerospace structural health monitoring applications. System integration and development, including modeling the power electronics, will be included.

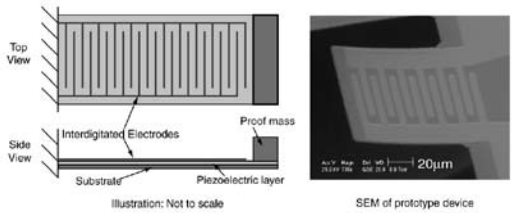

Figure 1: Illustration of MPVEH unimorph configuration (left) and SEM of a prototype device (right).

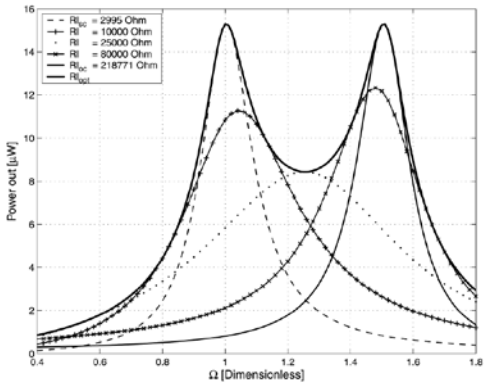

Figure 2: Power vs. normalized frequency with varying electrical load resistance [3].

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Micro Chemical Oxygen Iodine Lasers (MicroCOIL)

T. Hill, B. Wilhite, L.F. Velásquez-García, H. Li, A. Epstein, K. Jensen, C. Livermore
Sponsorship: DARPA, MDA

Conventional Chemical Oxygen Iodine Lasers (COIL) offer several important advantages for materials processing, including short wavelength (1.3 μm) and high power. However, COIL lasers typically employ large hardware and use reactants relatively inefficiently. This project is creating an alternative approach called microCOIL. In microCOIL, most conventional components are replaced by a set of silicon MEMS devices that offer smaller hardware and improved performance. A complete microCOIL system includes: microchemical reactors, microscale supersonic nozzles, and micropumps. System models incorporating all of these elements predict significant performance advantages in the microCOIL approach [1].

Initial work is focused on the design, microfabrication, and demonstration of a chip-scale Singlet Oxygen Generator (SOG): a microchemical reactor that generates singlet delta oxygen gas to power the laser. Given the extensive experience with microchemical reactors over the last decade [2-4], it is not surprising that a microSOG would offer a significant performance gain over large scale systems. The gain stems from basic physical scaling; surface to volume ratio increases as the size scale is reduced, which enables improved mixing and heat transfer. The SOG chip being demonstrated in this project employs an array of microstructured packed-bed reaction channels interspersed with microscale cooling channels for efficient heat removal. Figure 1 shows a schematic top view of the microSOG chip, including inlets and outlets for the reactant and product flows, and packed-bed reaction channels. Figure 2 shows a schematic diagram of stacked microSOG chips, micronozzles, and micropumps forming a complete microCOIL system.

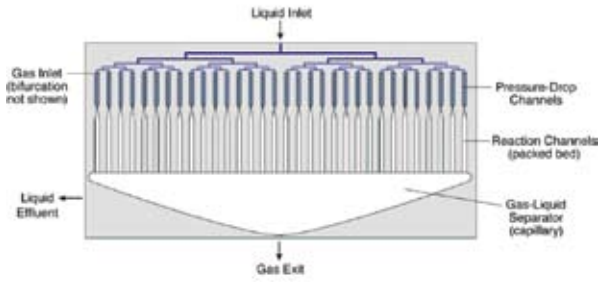

Figure 1: Schematic diagram of microSOG chip, showing reactant inlets, packed-bed reaction channels, and flow outlets.

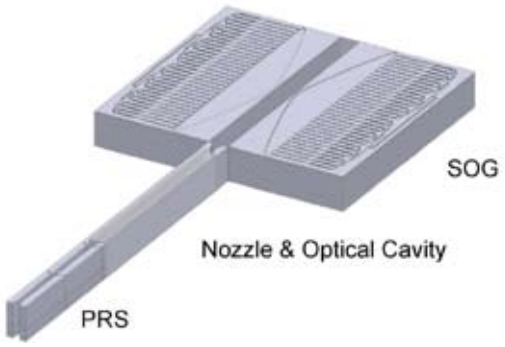

Figure 2: Schematic diagram showing multiple SOG chips, micronozzles, and micropumps (PRS) combined to form a microCOIL system.

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Linear Array of Electrospray Micro Thrusters

L.F. Velásquez–García, A.I. Akinwande, M. Martínez–Sánchez
Sponsorship: AFOSR

Electrospray thrusters are electrostatic accelerators of charged particles that use the electrohydrodynamic effect known as *Taylor cone* as propulsive effect [1]. These particles could be charged droplets, solvated ions, or a mix of the two. Since the new advances in electrospray technology that occurred in the late 1980s [2], the field of electrospray propulsion has experienced a renaissance, specifically aiming to provide efficient high-tunable precision low-thrust engines for micro-satellites and high accuracy astrophysics missions [3]. The MIT Space Propulsion Laboratory and the Microsystems Technology Laboratories are currently pursuing the development of a micro-fabricated electrospray emitter array for space propulsion. The project is developing in parallel two radically different concepts, a pressure-fed engine, and a surface tension-fed engine. This abstract reports the design, fabrication, and experimental characterization of a micro-fabricated, internally-fed linear array of electrospray emitters (Figure 1). This work demonstrates the feasibility of high clustering of electrospray emitters. The linear array is composed of 1 plenum, 12 manifolds, and 240 emitters. The emitters are sharpened to reduce the startup voltage. The electrodes are micro-fabricated with conductive paths made of tungsten and electrical insulation provided by vacuum gaps 350 µm wide and 10 µm thick PECVD silicon oxide. The electrodes are hand-assembled to the engine using a novel technique that relies on clusters of micro-fabricated springs [4]. This assembly scheme allows us to have two independent process flows for the electrodes and the engine hydraulics. The emitter-to-emitter separation is 130 μm, and the hydraulic diameter is 12 µm. The length of each channel is 15 mm. The engine uses highly doped formamide as propellant, with electrical conductivity in the 0.3 – 3.0 S/m range. The electrospray array operates in the single Taylor cone droplet emission regime, and it requires about 2000 V to become activated. The engine implements the concept of hydraulic and electrodynamic flow rate matching to achieve electrical control. Current versus flowrate characteristics of the engine are in agreement with a well-established reduced order model (Figure 2). Experimental data, demonstrating the low divergence of electrospray emitter arrays operated in the single Taylor cone, is in qualitative agreement with a reduced order mode that assumes the absence of a thermalized tail in the plume.

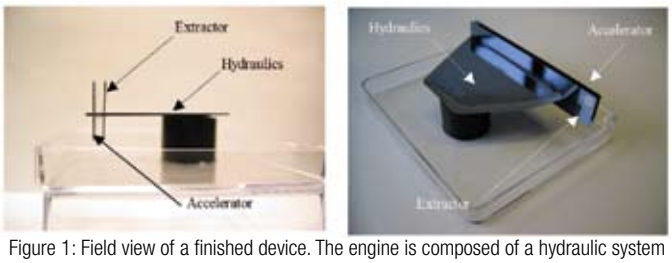

Figure 1: Field view of a finished device. The engine is composed of a hydraulic system and two electrodes, involving a total of four substrates. The electrodes are assembled to the hydraulic system using microprecision mesoscale silicon springs.

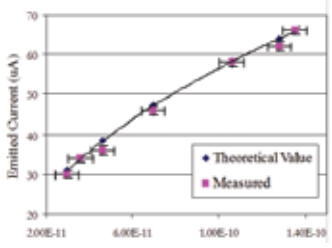

Figure 2: Experimental flowrate vs. emitted current using formamide with an electrical conductivity equal to 0.612 Si/m

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Planar Array of Electrospray Micro Thrusters

L.F. Velásquez–García. A.I. Akinwande, M. Martínez–Sánchez
Sponsorship: AFOSR, NASA

Electrospray thrusters are electrostatic accelerators of charged particles using the electrohydrodynamic effect known as *Taylor cone* to generate thrust [1]. These particles could be charged droplets, solvated ions, or a mix of the two. Since the new advances in electrospray technology that occurred in the late 1980s [2], the field of electrospray propulsion has experienced a renaissance, specifically aiming to provide efficient high-tunable precision low-thrust engines for micro-satellites and high accuracy astrophysics missions [3]. The MIT's Space Propulsion Laboratory and the Microsystems Technology Laboratories are currently pursuing the development of a micro-fabricated electrospray emitter array for space propulsion applications. The project is developing, in parallel, two radically different concepts, a pressure-fed engine and a surface tension-fed engine. This abstract reports the design, fabrication, and experimental characterization of a hybrid macro-fabricated/micro-fabricated, externally fed planar array of micro-fabricated electrospray emitters with macro-fabricated electrodes (Figure 1). An externally-fed engine has a number of advantages compared to the other implementations reported in the literature. For example, the engine lacks a static pressure difference between the plenum and the emitters; therefore, there cannot be propellant emission unless it is electrically activated. In this sense, the planar array is less vulnerable to unplanned propellant emission compared to pressure fed schemes. Additionally, clogging is not an issue in this engine because the propellant is not doped, and the flow channels are open. The planar array uses the ionic liquid EMI-BF_4 as a propellant. The ionic liquid EMI-BF_4 has a very low vapor pressure, making it suitable to be used in an open architecture engine. The array is composed of a set of spikes, i.e., emitters, coming out from a propellant pool. There are two configurations for the emitters: fully sharpened slender emitters, i.e., pencils, and truncated pyramidal emitters, i.e., volcanoes. The arrays have between 4 and 1024 emitters in an active area of 0.64 cm^2. The surface of the engine (tank and emitters) is covered with "black silicon" that acts as wicking material. The hydraulic system has been experimentally characterized, including: start-up tests (Figure 2), wettability tests, current-per-emitter versus voltage characteristics, imprints of the exit stream on a collector, and a thrust test in agreement with the current-per-emitter versus voltage characteristics and the time-of-flight measurements that we have independently obtained at the Space Propulsion Laboratory. Preliminary results demonstrating the feasibility of obtaining substantially larger emission currents at the same extraction voltage by controlling the temperature have also been obtained. The emission from the array seems to be described by a Schottky emission mechanism.

Figure 1: Field view of a highly packed planar emitter array *(left)*; field view of a hybrid macro-fabricated/micro-fabricated planar array *(right)*.

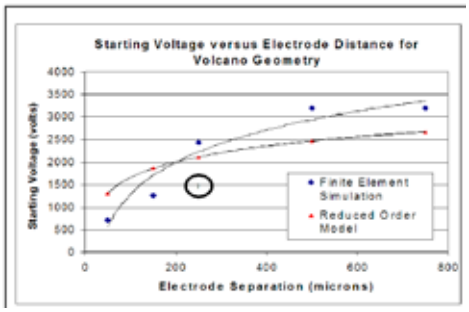

Figure 2: Start-up voltage vs. extractor separation for volcano emitters. The experimental points (from the testing facility with a fixed emitter-to-electrode separation equal to 250 μm) fall inside the circle drawn on the left plot.

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Numerical Techniques for Integral Equations

M. Altman, J. Bardhan, X. Hu, S. Kuo, D. Willis, L. Daniel, J. Peraire, B. Tidor, J. White
Sponsorship: MARCO IFC and GRC, NSF, SRC, SMA, NIH

Finding computationally efficient numerical techniques for simulation of three-dimensional structures has been an important research topic in almost every engineering domain. Surprisingly, the most numerically intractable problem across these various disciplines can be reduced to the problem of solving a three-dimensional potential problem with a problem-specific Greens function. Application examples include: electrostatic analysis of sensors and actuators, electromagnetic analyses of integrated circuit interconnect and packaging, detailed analysis of frequency response and loss in photonic devices, drag force analysis of micromachined structures, and potential flow based aircraft analysis. Over the last fifteen years, we have been developing fast methods for solving these problems, and have developed widely used programs such as FastCap (capacitance), FastHenry (magnetoquasistatics), FastLap (general potential problems), FastImp (full wave impedence extraction),and FastStokes (fast fluid analysis). Our most recent work is in developing higher order methods[1], methods that efficiently discretize curved geometries[2], methods that are more efficient for substrate problems [3], and methods for analyzing rough surfaces [4].

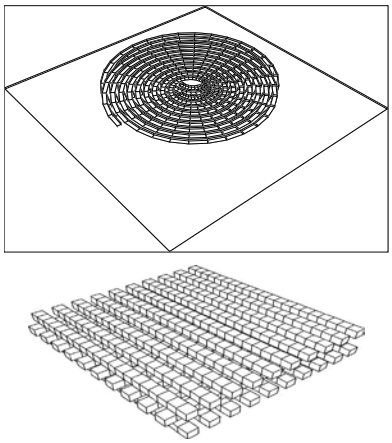

Figure 1: A buss crossing structure and a spiral inductor over a substrate. Analyzed by FastImp in minutes.

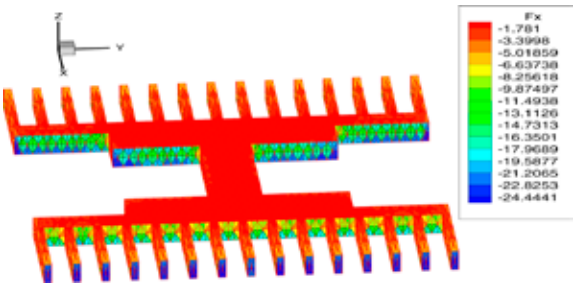

Figure 2: The fluid drag force distribution for a micromachined comb, computed using FastStokes in under five minutes.

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Characterization and Modeling of Nonuniformities in DRIE

H.K. Taylor, H. Sun, T.F. Hill, D.S. Boning
Sponsorship: CMI, SMA

We contribute a quantitative and systematic model to capture etch nonuniformity in the deep reactive ion etching (DRIE) of microelectromechanical systems (MEMS) devices [1]. DRIE is commonly used in MEMS fabrication where high-aspect ratio features are to be produced in silicon. It is typical for many devices, of diameters on the order of 10 mm, to be etched simultaneously into a silicon wafer of diameter 150 mm. Devices containing a range of feature diameters exhibit aspect ratio-dependent etching rates, a phenomenon that is well understood [3]. In addition, equivalent features within supposedly identical devices are observed to etch at varying rates. These spatial variations have been explained in terms of uneven distributions of S_xF_y ions and fluorine neutrals at the wafer scale, and of competition for those species at the device, or die, level. An ion–neutral synergism model [7] is constructed from data obtained by etching several layouts of differing pattern opening densities (Figure 2). Such a model is used to predict wafer-level variation with an r.m.s. error below 3% (Figure 1). This model is combined with a die-level model, which we have reported previously [2,8], on a MEMS layout. The two-level model is shown to enable prediction of both within-die and wafer-scale etch rate variation for arbitrary wafer loadings.

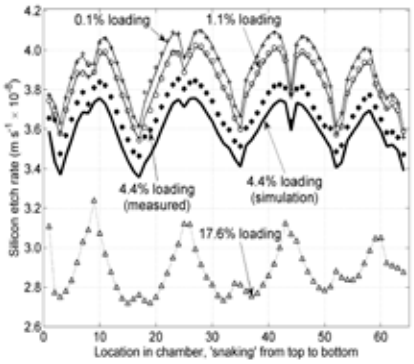

Figure 1: Four silicon wafers were etched in a deep reactive ion etcher, each wafer having one of the following proportions of its total surface area exposed for etching: 0.1%, 1.1%, 4.4%, 17.6%. An ion–neutral synergism model was fitted to etch rate data from wafers with 0.1%, 1.1% and 17.6% 'loading'. The 0.1%, 1.1% and 17.6% traces on this graph indicate that the model has successfully been fitted to the data. Lines represent the model's predictions; markers represent measured etch depths. The model can predict etch rates across a wafer with 4.4% loading, with an r.m.s. error of less than 3%.

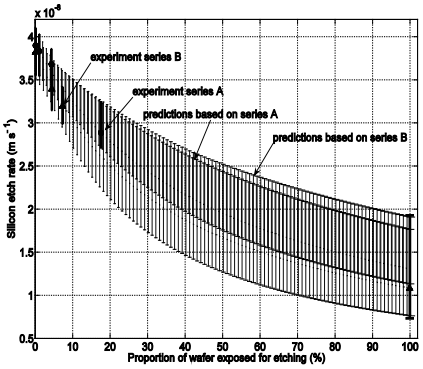

Figure 2: Measured and predicted etch rates as a function of the proportion of the wafer exposed for etching ("loading"). Data is presented for two sets of experiments performed on different dates using the same tool. At any given value of loading, a range of etch rates is observed across a wafer. The heights of the vertical bars in this figure indicate the size of that range. The thick vertical bars indicate the measured data; the bands constructed from thin lines indicate predictions of etch rates made using parameters extracted from the measured data.

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[8] Sun, H., T. Hill, M.A. Schmidt, D. Boning, in 2003 Materials Research Society Fall Meeting, Boston, MA, 2003.

Measuring the Mechanical Properties of Thin Films Using MEMS Structures

R. Bernstein, D. Moore, C. Thompson
Sponsorship: CMI, SMA

Simple micromechanical devices are being developed to measure the mechanical properties of thin films in localized areas after processing. The simplest devices to fabricate are cantilevers overhanging a pit formed using an anisotropic etch. Cantilevers formed from a material of interest can be used to measure the through-thickness stress-gradient and the elastic modulus of that material. Measuring the elastic modulus requires applying a known force to the tip of the cantilever and measuring the subsequent deflection or curvature. We have developed a technique for high accuracy modulus measurement by application of a force with a beam having known properties, with deflection measurements made in an optical profilometer.

Membrane devices, as shown in Figure 1, can be used to measure the stress in a thin film without further processing. The membranes are fabricated using an SOI wafer as the starting material. An anisotropic etch from the backside is used to form the membrane, which consists of two layers: buried silicon dioxide under the device single crystal silicon. The membrane buckles because the buried silicon dioxide is under compressive stress relative to the silicon. The amount of buckling is determined by the mechanical properties and the geometry of the membrane, and is measured using optical profilometry. Depositing a film on either side of the membrane changes the buckling, and therefore, the stress of the new material can be determined. Films deposited on both sides of the membrane contribute to the change in deflection; consequently, the stress in CVD films can be measured.

Buckling of doubly-supported beams can be used to characterize compressive stresses. To characterize tensile stresses, we have recently developed a new type of device, a V-shaped beam, as shown in Figure 2(a). The V-beam is made from a material of interest. A tensile stress causes out-of-plane bending that can be measured using an optical profilometer. The measured deflections are then compared to finite element analyses. Two modes of bending have been seen in V-beams produced from silicon nitride thin films. Finite element models of the 2 modes showing vertical deflection contours can be seen in Figures 2(b) and 2(c). Mode 1 bending is symmetric and produces very large deflections that are often too large to measure in an optical profilometer. Most beams tend to bend into Mode 2, which is asymmetric, but easily measured using an optical profilometer. Mode 2 deflections also have the advantage that the through-thickness stress gradient does not change the deflection. Because all the devices described above are small, they can be placed in many locations on the wafer.

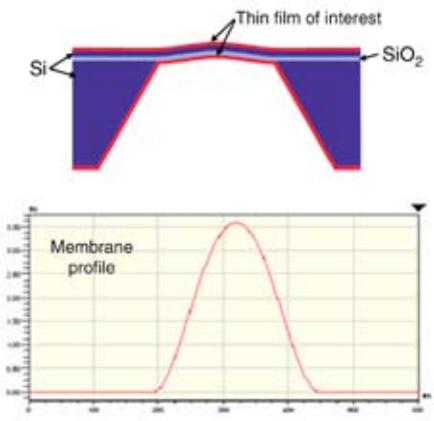

Figure 1. Cross section of a square membrane after the CVD thin film of interest has been deposited, with measured deflection from optical profilometry.

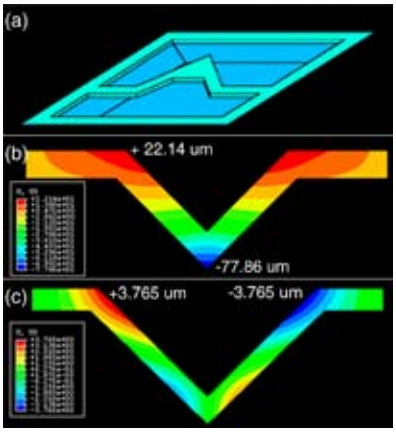

Figure 2. (a) V-beam device released by anisotropic etch. (b) Finite element analysis (FEA) of Mode 1 bending in a v-beam, with maximum deflection at tip of V. (c) FEA of Mode 2 bending.

Scanning Probe Microscopy with Inherent Disturbance Suppression Using Micromechanical Devices

A.W. Sparks, S.R. Manalis
Sponsorship: AFOSR

Scanning probe microscopes are notoriously susceptible to disturbances, or mechanical noise, from the surrounding environment that couple to the probe–sample interaction. These disturbances include vibrations of mechanical components, piezo drift, and thermal expansion. Disturbance effects can be substantially reduced by designing a rigid microscope, incorporating effective vibration isolation, and selecting an appropriate measurement bandwidth and image filter. However, it is not always possible to satisfy these requirements sufficiently, and as a result, critical features in an image can be obscured.

The cause of this problem is that the actuator (control) signal is used both to readout topography and correct for disturbances. We have introduced a general approach for inherently suppressing out-of-plane disturbances in scanning probe microscopy [1]. In this approach, two distinct, coherent sensors simultaneously measure the probe-sample separation. One sensor measures a spatial average distributed over a large sample area, while the other responds locally to topography underneath the nanometer-scale probe. When the localized sensor is used to control the probe-sample separation in feedback, the distributed sensor signal reveals only topography. This configuration suppresses disturbances normal to the sample. We have applied this approach to scanning tunneling microscopy (STM) with a microcantilever that integrates a tunneling tip and an interferometer (Figure 1) and have shown that it enables Angstrom resolution imaging of nanometer-sized gold grains in a noisy environment (Figure 2). For disturbances applied normal to the sample, we measured disturbance suppression of -50 dB at 1 Hz, compared to 0 dB with conventional imaging.

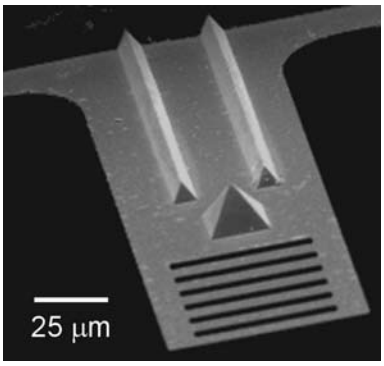

Figure 1: Scanning electron micrograph of the silicon nitride cantilever with integrated tunneling probe and interferometer.

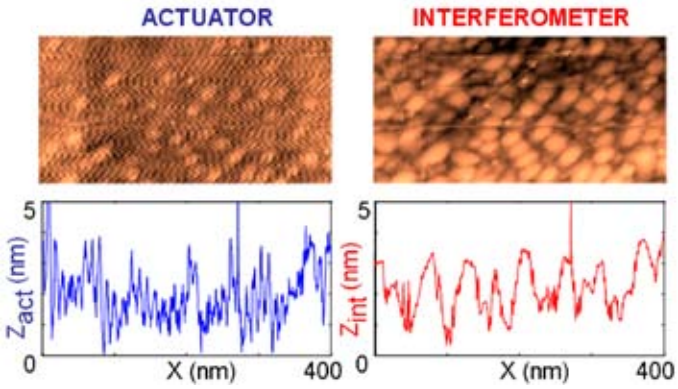

Figure 2: 400 x 200 nm^2 STM images of Au/Pd/Ti on a silicon substrate, imaged at 0.2 Hz on a mechanically grounded optics table. Cross sections from each image are shown for the same scan line.

REFERENCES:

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In-Plane AFM Probe with Tunable Stiffness

C. Mueller-Falcke, S.-G. Kim
Sponsorship: IMC

We developed an in-plane Atomic Force Microscope (AFM) probe that is specifically tailored to the needs of biological applications. It features a variable stiffness, which makes the stiffness of the probe adjustable to the surface hardness of the sample [1]. The inherent capability of the in-plane AFM probe for building a massively parallel array is also an important feature that greatly affects the speed of the AFM scanning process.

Concept and Functionality

The switchable stiffness probe allows the scanning of biological samples with varying surface hardness without changing probes during scanning and therefore, prevents a loss of positional information, as is unavoidable with conventional devices. For the integration of the components into a MEMS device, the conventional cantilever-type design of AFM probes has been abandoned in favor of an in-plane design. The new design has an advantage in that it facilitates a high-density array of AFM probes and allows for easy surface micromachining of the integrated device. It also enables the integration of micro-fluidic channels for reagent delivery and nanopipetting. For scanning nano-scale trenches and grooves, a multi-walled carbon nanotube, embedded in a nanopellet [2], is mechanically assembled to the AFM probe as a high-aspect-ratio tip.

Design and Fabrication

The variable stiffness is accomplished in a mechanical way by engaging or disengaging auxiliary beams to the compliant beam structure by the means of electrostatically actuated clutches (Figure 1). Figure 2 shows the integrated AFM probe system. For actuation, an electrostatic combdrive is considered to move the probe tip up and down. The vertical displacement of the tip can be measured by a capacitive sensor, which can easily be integrated into the system.

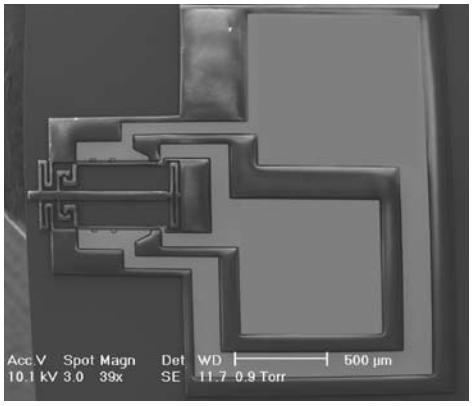

Figure 1: Unreleased in-plane AFM probe with electrostatic actuators that engage the clutches.

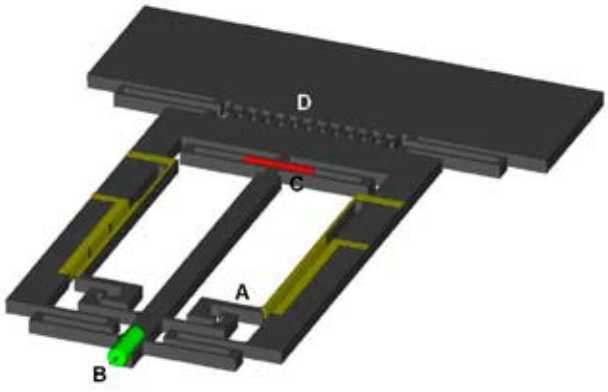

Figure 2: Device design (A: Electrostatic clutch, B: High-aspect-ratio carbon nanotube tip, C: Capacitive sensor, D: Combdrive actuator).

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Direct Patterning of Organic Materials and Metals Using a Micromachined Printhead

V. Leblanc, J. Chen, S.H. Kang, P.J. Benning, M.A. Baldo, V. Bulovic, M.A. Schmidt
Sponsorship: Hewlett-Packard

Organic optoelectronic devices are promising for many commercial applications, if methods for fabricating them on large area low-cost substrates become available. Our project investigates the use of MEMS in the direct patterning of materials needed for such devices.

In our first demonstration, we used an electrostatically actuated micromachined shutter integrated with an x-y-z manipulator to modulate the flux of evaporated organic semiconductors and metals and to generate patterns of the deposited materials. The micromachined printhead consists of a free-standing silicon microshutter actuated over a 25 micron square aperture by a comb-drive actuator. Figure 1 shows the microshutter and aperture. The device is fabricated, starting with a SOI (silicon on insulator) wafer, and using deep reactive ion etching to pattern both the through-wafer aperture and the free-standing structure and actuation mechanism. An operating voltage of 30 V is needed to obstruct the aperture with the microshutter. The simulated first mechanical resonant frequency of the device is 6 kHz.

We tested the printing method in a vacuum chamber by depositing an organic semiconductor, Alq_3 (tris (8-hydroxyqunolinato) aluminum), and silver on glass substrates. We also printed arrays of organic light emitting devices (OLED). Figure 2 shows patterns obtained using this method: photoluminescence image of 40 micron pixels of Alq_3, optical microscope image of 30 microns wide line patterns of silver, and electroluminescence of 30 micron pixels arrays of TPD:10%DCM/Alq3/TAZ at 20 V (with blue filter), and of TPD/Alq3/TAZ at 10V (no filter). The results show that this printing technique is capable of patterning small molecule organic light emitting devices at high resolution (800 dpi in our case).

The next stage of this project will involve investigating the use of a microporous layer with integrated heaters for local evaporation of the materials.

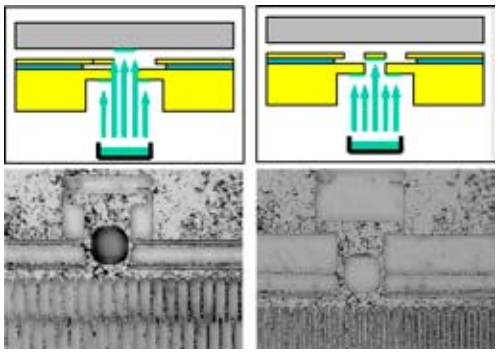

Figure 1: Schematic of printing principle and microscope image of aperture (dark area) and shutter. Left: when no voltage is applied, the material deposits on the substrate. Right: the shutter covers the aperture, and no material can be deposited on the substrate.

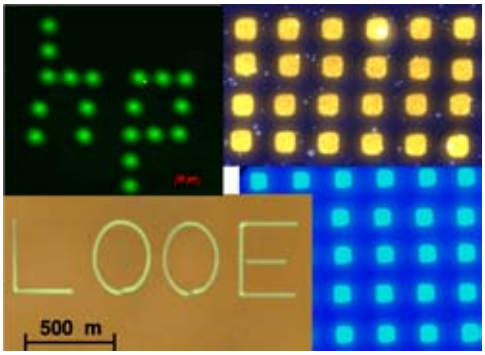

Figure 2: Patterns obtained using our direct patterning method. Clockwise from top right: photoluminescence of Alq3 pixels, electroluminescence of 2 different OLED arrays with 30 micron pixels, and reflection image of silver pattern.

Nanometer-Level Positioning in MEMS without Feedback Control

M. Culpepper, S. Chen, C. DiBiasio
Sponsorship: NSF Nanomanufacturing Program

Traditional macro-scale nanopositioners rely on sensors and feedback control to achieve nanometer-level accuracy and repeatability. The need for low-cost, high-speed precision positioning devices has led to a trend in miniaturization of these machines. Miniaturization of precision positioning devices is problematic as precision positioners require feedback control, and feedback control is not readily adapted to small-scale machines. The difficulty in adaptation is due mainly to the challenges encountered during the integration of small-scale sensors, mechanisms, and actuators. In this work, we are designing multi-axis MEMS that are capable of nanometer-level positioning without sensing/feedback control. The approach has grown from binary actuation technologies used in macro-scale robotics [1,2].

In our approach, Digital Nanoactuation Technology (DNAT), a positioner is equipped with actuator-flexure building blocks. The blocks consist of a pair of binary actuators that work together to generate discrete, repeatable positions. The actuators are attached to a positioning stage via flexures such that the actuator-flexure sets are diametrically opposed. An actuator set is shown on the left side of Figure 1. The opposed flexures differ in stiffness, one compliant, K_C, and one stiff, K_S. When both actuators are activated (four possible on-off combinations), four repeatable positions may be obtained. DNAT building blocks may be superimposed to provide many position states. For example, the 64 states shown on the right side of Figure 1 are obtained by superimposing the output of three blocks. The number of states scales with the number of actuator pairs, N, as 2^{2N}. A positioner with N = 6 is capable of over 4000 discrete positions. If these points are encompassed within a space of a few microns, simple on and off actuator commands may be used to obtain nanometer-level repeatability without sensing/feedback. A macro-scale analogy of a small-scale device has been constructed and tested [3] to demonstrate that nanometer-level positioning is possible. The small-scale prototype shown in Figure 2 is being tested to characterize a 64 state prototype before we progress to a smaller, 4000 state device.

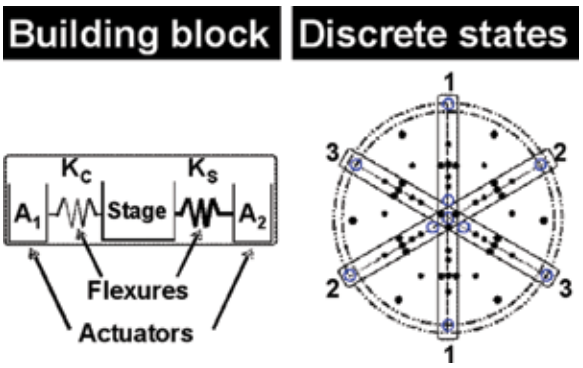

Figure 1: DNAT building block (left) and 64 Discrete position states obtained with three building blocks (right)

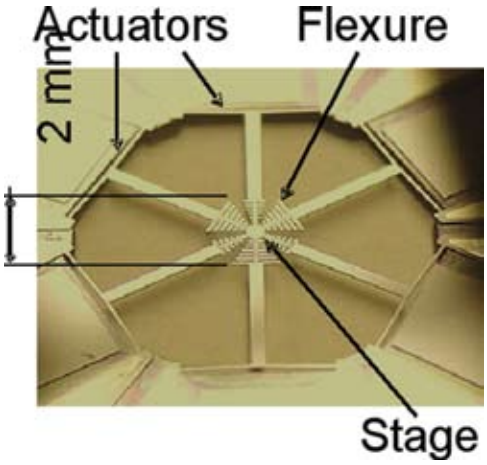

Figure 2: Small-scale DNAT positioner

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An Electrostatic, Circular Zipping Actuator for the Application of a Tunable Capacitor

X. Yang, A.H. Slocum, J.H. Lang
Sponsorship: Deshpande Center for Technological Innovation

A tunable capacitor is devised using a circular zipping actuator, based on its ability to potentially control a gap between two large surfaces with nanometer resolution [1]. The device consists of three wafers; a SOI (Silicon-On-Insulator) wafer sandwiched by two *Pyrex* glass wafers that are anodically bonded together, as shown in Figure 1. In the center of the device is a circular membrane that is supported by tethers that are connected to the outer walls. A cylindrical fulcrum, fabricated by the deep reactive ion etching technique, acts as the pivot for the membrane and divides the membrane into the outer actuator region and the center capacitor region. The top of the fulcrum is bonded to the top glass wafer for structural rigidity. The SOI layer is used as the membrane-actuator because of its uniform thickness and the low stress of single-crystal silicon. Thermally grown silicon dioxide is used as dielectric insulation. The bottom wafer contains the bottom electrodes for the actuator and the capacitor. The actuator electrode is etched into the glass to form the gap of the actuator. Gold is deposited on top of the glass wafer as both actuator and capacitor electrodes. Voltage is applied between the top and the bottom actuator electrodes. At a certain threshold, the outer membrane snaps down. With increasing actuation voltages, the membrane zips along the radial direction, as shown in Figure 2, and results in the separation of the two capacitor surfaces. Because of the poor adhesion of gold to oxide, the membrane will not be bonded to the gold surface, although the two are in close contact during operation. Thus, the design makes it possible to have two initially closed-contacted surfaces that can be pried apart. By changing the gap between the two plates of the capacitor, the capacitance can be tuned.

The device is modeled using both numerical methods with Matlab and FEM with ANSYS. Tests are done using a laser interferometer to measure the center displacement and a network analyzer to measure the capacitance change.

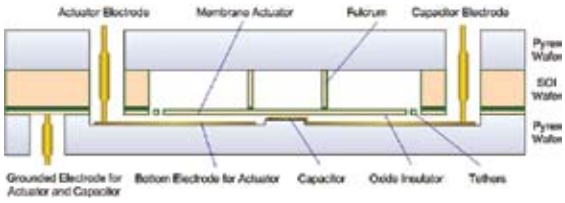

Figure 1: Cross-sectional view of the circular, zipping actuator device before actuation.

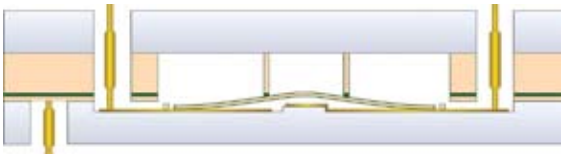

Figure 2: Cross-sectional view of device after actuation.

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A Low Contact Resistance MEMS Relay

A.C. Weber, A.H. Slocum, J.H. Lang
Sponsorship: ABB Corporate Research

An electrostaticaly driven, bulk micromachined, low contact resistance MEMS cross bar relay has been designed, and is currently under fabrication. This relay will be used to study and optimize the behavior of micro-scale contacts for power applications.

Many MEMS relays have been reported in the literature [1,2,3]; most, however, are not suited for practical power applications due to their high contact resistance. A contact resistance of 50 mΩ [4] has been achieved by our group using a bulk micromachined, externally actuated structure as a proof of concept for this design [4].

The electrostatic "zipper" actuators [4,5] are designed for low pull-in voltage (~100 V) and large contact travel (~40 µm) to prevent arcing as the load circuit (up to 600V) is switched on and off. Figure 1 shows the MEMS relay. Figure 2 shows a detailed view of the actuator. The two arms of the parallelogram flexure are used as the traveling electrodes of the electrostatic actuators. Each traveling electrode, or arm of the parallelogram flexure, is adjacent to a pair of stationary electrodes: an engaging and a disengaging stationary electrode. The relay is engaged by electrostatic attraction between the traveling electrodes and the engaging stationary electrodes. Similarly, the MEMS relay is disengaged through electrostatic attraction between the traveling electrodes and the disengaging stationary electrodes. Each stationary electrode is comprised of a stiff component and a compliant, cantilevered component. The cantilevered component reduces the pull-in voltage by reducing the distance between the electrodes. As the actuator is energized, the compliant end of the stationary electrode, having the lower stiffness, is attracted by and deflected toward the moving electrode, making initial contact at the loose end of the cantilever. As the actuation voltage is increased, the contact point between the electrodes is displaced along the stationary electrode over the stiff component of the electrode in a "zipping" motion.

Our group continues to develop these MEMS relays for power applications.

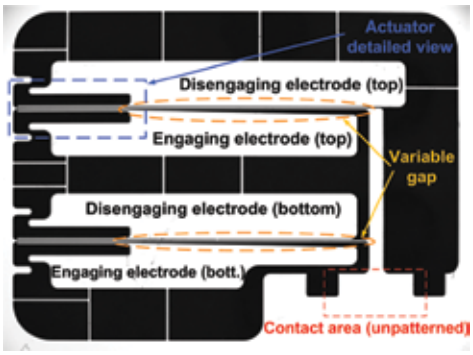

Figure 1: MEMS relay top view

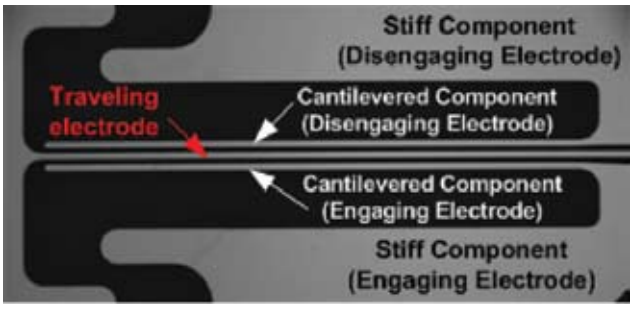

Figure 2: Actuator detailed view

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A Variable Capacitor Made from Single Crystal Silicon Fracture Surfaces

A. Sprunt, A. Slocum, J.H. Lang
Sponsorship: Center for Bits and Atoms

A process for the fracture fabrication of single crystal silicon surface pairs with nanoscale roughness has been developed, and a prototype variable capacitor, featuring fracture surfaces as the moveable parallel plates, has been fabricated. The surfaces are fabricated by notching a portion of a compliant structure with either potassium hydroxide (KOH) or Focused Ion Beam (FIB) milling to produce a stress concentration. The device is fractured by pulling on the compliant structure with a probe. Post-fracture, the compliant structure acts as a bearing so the two surfaces can be brought back into intimate contact without misalignment. Proper alignment ensures that nanometer scale gaps can be maintained with surfaces that are perfectly smooth or complementary. Complementary surfaces have been closed to gaps less than 20 nm. For a successful fracture, the notch must be very sharp and properly aligned to the crystal structure, and the compliant structure (typically etched into the device layer of a Silicon On Insulator (SOI) wafer) must attenuate stray forces and moments and withstand the trauma of fracture. Experiments with different specimens have shown 10 µm to be the optimal thickness (Figure 1).

An updated version of the device used for the surface fabrication experiments has been fabricated, assembled, and sealed (Figure 2). This device includes an integrated zipper actuator [1] for controlling the separation of the surfaces, as well as, provision for wirebonding the device into its hermetically sealed package. Testing has confirmed that the actuator functions properly and that the specimens survived the fabrication process. The device also validated the electrical model used to design the capacitance measurement circuitry. Unfortunately, fracturing of these new devices has been problematic: growing the actuator's thermal oxide has likely blunted the notches. The fabrication process has been debugged, and a new round of fabrication (with an improved design) is nearing fruition.

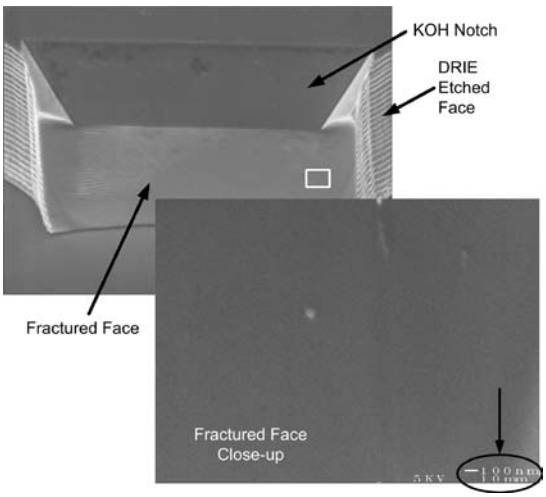

Figure 1: A high resolution SEM image of a fractured surface. Note the exceptionally good surface roughness.

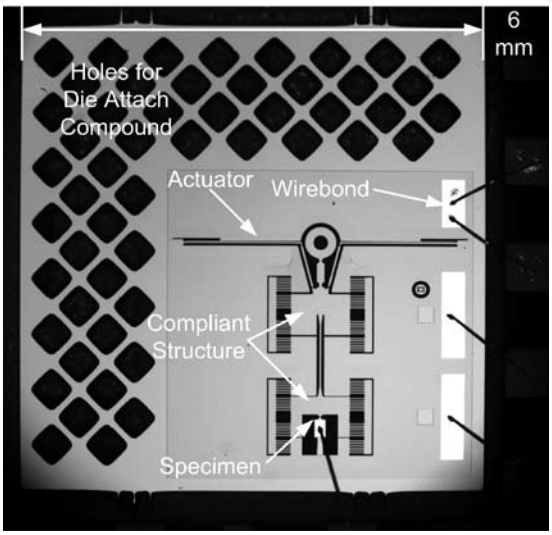

Figure 2: Integrated device for measuring the capacitance between pairs of fracture fabricated nanosurfaces.

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A High-*Q* Widely Tunable Gigahertz Electromagnetic Cavity Resonator

S.M. Hou, J.H. Lang, A.H. Slocum, A.C. Weber, J.R. White
Sponsorship: EECS, MechE

RF systems need high-frequency widely tunable high-*Q* bandpass filters for channel selection filters and local oscillators. Our work describes the design, fabrication, and testing of an electromagnetic cavity resonator designed for such applications. Alternative technologies provide wide tuning or high *Q*, but not both, and are generally not tunable. This resonator is distinguished by its simultaneous high *Q* near 200 and its wide high-frequency tuning range of 2.5 GHz to 4.0 GHz, which have been experimentally demonstrated. The resonator is fabricated using standard MEMS technologies and consists of a gold-lined capacitor and toroidal inductor cavity formed by etching silicon in potassium hydroxide (Figure 1). Frequency tuning is performed by compressing the cavity to close the capacitor gap. Testing was done with a piezoelectric actuator for this task. The match between the modeled and measured impedance is extremely good up to and beyond 5 GHz, with less than a 1% error in magnitude and phase.

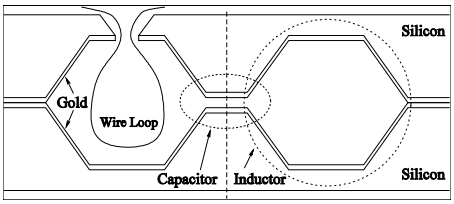

Figure: 1: Cross-sectional view of a cavity resonator with magnetic coupling.

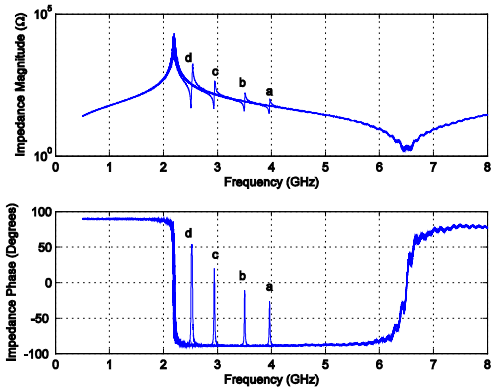

Figure 2: Superimposed impedances as functions of frequency when the capacitor gap is reduced by (a) 0 µm, (b) 5 µm, (c) 10 µm, and (d) 13.9 µm.

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Lateral, Direct Contact RF MEMS Switch with PZT Actuation

W. Choi, Y. Shi, S.-G. Kim
Sponsorship: Korean Institute of Machinery and Materials

A novel direct contact MEMS switch is developed with compliant lateral metal contacts to address the need for low contact resistance and long life cycles. The device is unique in its self-alignment of the contact surfaces, self-cleaning of particles generated at each contact cycle, and mechanical anchoring method of the contact metal to the side of the Su-8 beam structures. The fabricated device maintains less than 0.1Ω contact resistance for up to 10 billions of cycles of contact. A fabricated device is shown in Figure 1 (a). Each switching member consists of two parallel beams with angled contact surfaces. One side of the contacting surfaces is undulated with micro grooves, as shown in Figure 1 (b). When the movable member is actuated to meet the fixed one, the gold on each side of the contact creates a short circuit. When the movable member is on the other side, enough gap is maintained to open the circuit with high isolation. The angled contact orientation makes the undulated surface slide over the static surface, which pushes entrapped particles or generated micro-weldments into the micro-grooves. By cleaning the surface at every cycle of switching, the micro-undulated surface ensures a low contact resistance over long cycles of switching operation. The grooved contact surfaces show successfully that the self-cleaning concept works and that a low contact resistance below 0.1Ω has been maintained over 10 billion cycles. (Figure 2)

Applications of the self-cleaning MEMS switch, such as tunable antennas, are being investigated to assess the commercial potential of our switch.

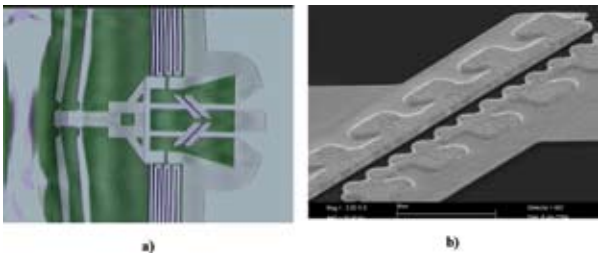

Figure 1: Fabricated device: a) Released device's layout, b) Contact metal at the later wall.

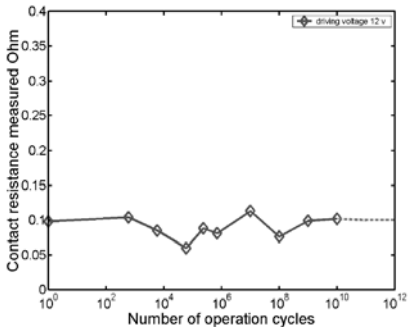

Figure 2: Contact resistance over operation cycles.

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Design and Fabrication of Nano-Tweezers

F. Hashemi, G. Chen
Sponsorship: MIT

Since the invention of atomic force microscopes (AFM) that provided researchers with a convenient tool to observe objects at nanoscale, manipulation tools at nanoscale have been in high demand. There have been several attempts to create nanomanipulation devices, such as nano-tweezers, to address this challenge. Most such attempts have amounted to single proofs of concepts rather than a practical, readily producible manipulation tool. The goal of this project was to further the current state of nanomanipulators, by producing nano-tweezers that are consistently producible, using batch microfabrication processes. In addition, given the regularity and practicality of the AFM as a nano-scale research tool, the nano-tweezers were intended to also serve as a scanning probe for the AFM. This way, the same tool can to be used to both image and manipulate samples, and the utility of the devices is increased.

A two-fold approach was used to tackle the problem. First, using complete batch fabrication methods, a process was created to generate nano-scale tweezer tips separated by a nano-scale gap. This process uses standard micron scale batch lithography to define pyramidal walls in silicon. It then produces an extremely thin cut that self-aligns to the apex of the pyramid. Thus far, tip separations of 358nm and tip widths of 50nm have been repeatably produced. The alignment of the process is within 35nm and is much smaller than that of the lithography tool. The second phase was to create free standing, protruding structures that can serve as the tweezing arms and move with nano-scale resolution. Cantilevered flexural members, coupled with electro-static actuation, were successfully fabricated. These slender cantilevered flexural components measure only 1-2 um in width. A novel process was developed that overcomes problems due to surface tension, and protects the released devices all the way through die separation.

The devices have shown actuation behavior that is consistent with theory and design intent. Resolution of motion of 40nm has been verified using SEM through the entire working range of the device. Resolution of less than 10nm is expected based on data but has not been verified due to the limits of this SEM.

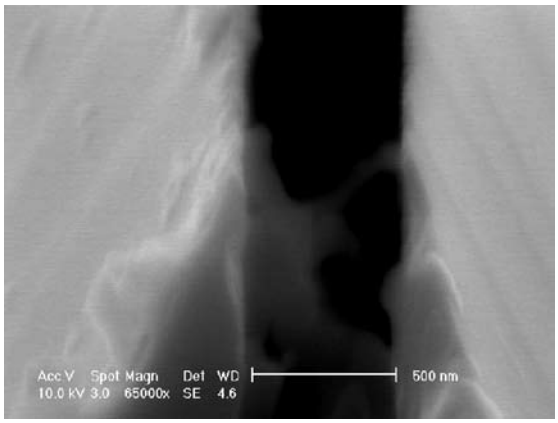

Figure 1: Close up cross-sectional view of the split pyramid showing tip separation.

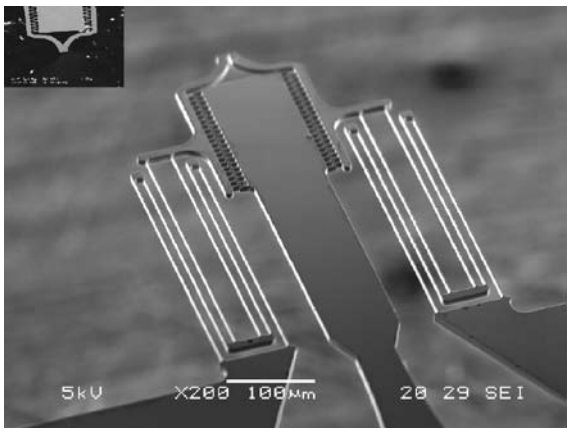

Figure 2: SEM image of the nano-tweezers. Image insert showing the nano-tweezers actuated, closed state.

Induced-Charge Electro-Osmotic Pumps and Mixers for Portable or Implantable Microfluidics

J.A. Levitan, Y. Ben, T. Thorsen, M.A. Schmidt, M.Z. Bazant
Sponsorship: Institute for Soldier Nanotechnologies, MIT-France Program

Microfluidic technology offers great promise in diverse fields such as bioinformatics, drug delivery, and analytical chemistry. In spite of involving microchannels, however, current lab-on-chip technologies are mostly limited to bench-top analysis due to various bulky external elements. For example, peristaltic pumping in soft-polymer channels requires complicated tubing and flow meters, and capillary electro-osmosis requires a high-voltage power supply. Miniaturizing and integrating the power source is a crucial next step toward portable or implantable devices for medical diagnostics, localized drug delivery, artificial organs, or pressure control to treat diseases such as glaucoma.

We are developing new kinds of pumps and mixers exploiting "induced-charge electro-osmosis" (ICEO) [1], as a potential platform for portable microfluidics. ICEO refers to the slip of a liquid electrolyte at a polarizable (metal or dielectric) solid surface, driven by an electric field acting on its own induced surface (double-layer) charge. Unlike classical (fixed-charge) electro-osmosis, which requires large DC voltages (>100V) applied down a channel, ICEO can be driven locally by small AC voltages (<10V). It is sensitive to the geometry, ionic strength, and driving frequency and scales with the square of the applied voltage. The effect generalizes "AC electro-osmosis" at planar electrode arrays [2] and offers some more flexibility.

We originally demonstrated ICEO flow in dilute KCl around a platinum wire by comparing flow profiles from micro-particle-image velocimetry (μPIV) to our theory [3]. We have also fabricated many devices involving electroplated gold structures on glass in PDMS microchannels, which exhibit mm/sec flow rates in 100 V/cm fields at kHz AC, and further optimization is underway. As a first application, we are developing a portable ICEO-powered biochip to detect blood exposure to toxic warfare agents by lysing cells and amplifying and detecting target genes.

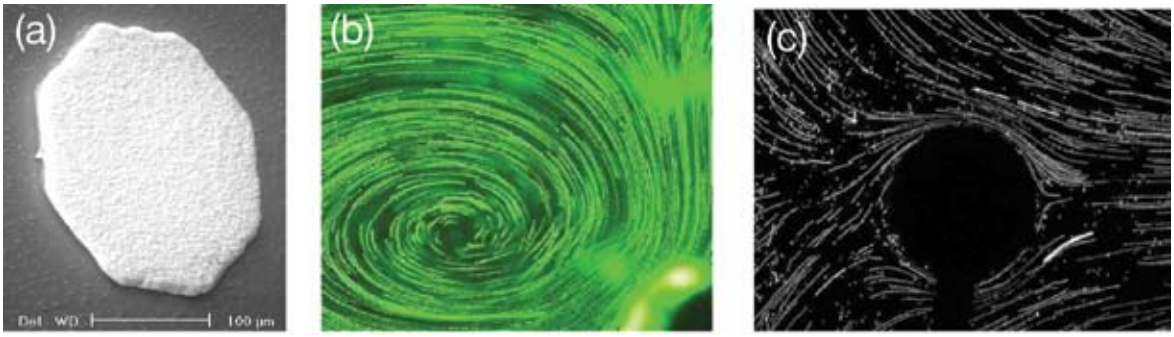

Figure 1: (a) SEM image of an electroplated gold post (12μm x 150μm). (b) ICEO convection around the post, visualized by streaks of fluorescent tracers used μPIV. (c) faster ICEO flow past a post held at fixed potential.

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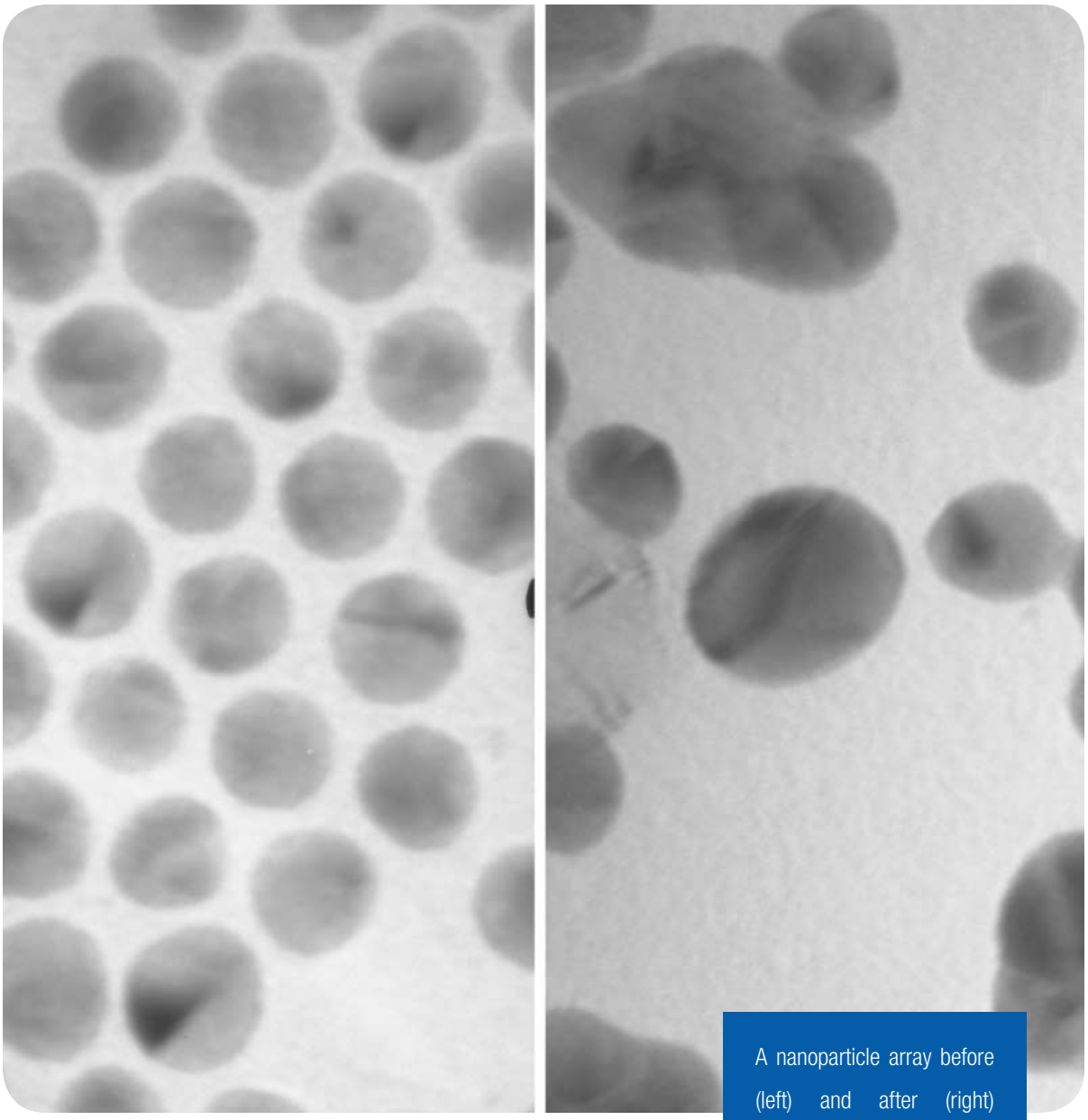

A nanoparticle array before (left) and after (right) heat treatment to induce particle sintering. Image by Thompson group.

MOLECULAR AND NANOTECHNOLOGY

TABLE OF CONTENTS

Nanostructured Origami™ Theory

P.S. Stellman, G. Barbastathis
Sponsorship: ISN, MARCO IFC

The Nanostructured Origami method [1] fabricates 3D devices first by patterning nanostructures (electronic, optical, mechanical, etc.) onto a 2D substrate, then by folding segments along pre-defined creases until the final design is obtained. This approach allows almost arbitrary 3D nanostructured systems to be fabricated using 2D nano-patterning tools exclusively.

We present two approaches to the kinematic and dynamic modeling of folding origami structures. The first approach addresses the kinematics of unfolding single-vertex origami structures. First, a unit positive "charge" is assigned to the creases of the structure in its folded state. Thus, each configuration of the structure as it unfolds can be assigned a value of electrostatic (Coulomb) energy [2]. Because of repulsion between the positive charges, the structure will unfold if its energy is allowed to decrease. We obtain the desired unfolding trajectory by numerical minimization using the steepest descent algorithm. If energy minimization can be carried out all the way to the completely unfolded state, we are simultaneously guaranteed the absence of collisions for the determined path. The electrostatic potential predicts the correct kinematics. However, this prediction is not physically realistic, and thus it does not give the correct dynamics of unfolding. The actual folding path is obtained by simply reversing the unfolding trajectories.

The second method achieves dynamic modeling of folding multi-segment (accordion style) origami structures. The actuation method for folding the segments uses a thin, stressed metal layer that is deposited as a hinge on a relatively stress-free structural layer. The strain energy induced by the internal reaction in the curling hinge is defined as a function of rotation angle, and the minimization of this potential energy results in the trajectory of the structure and its dynamic behavior. A computationally efficient collision-detection algorithm has also been implemented to check for self-intersections. Based on the trajectory and the collision-detection algorithm, we can iteratively design the actuation sequence for arbitrary accordion foldings.

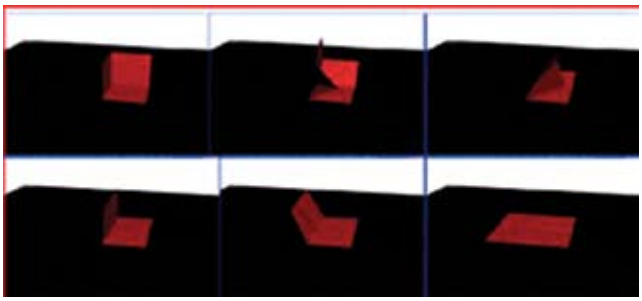

Figure 1: Kinematics of a single vertex origami (corner cube) using charge method.

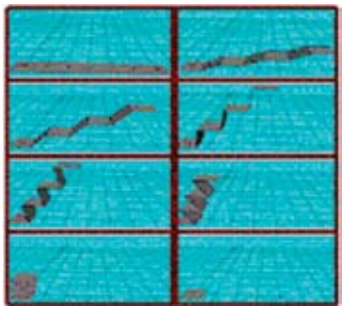

Figure 2: Dynamics of accordion style origami.

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Alignment Techniques for the Nanostructured Origami™ 3D Fabrication and Assembly Process

H.J. In, A. Nichol, W. Arora, H. Smith, G. Barbastathis
Sponsorship: MARCO IFC, ISN, NSF SGER

The Nanostructured Origami™ 3D Fabrication and Assembly Process enables the fabrication of nanostructured, 3D devices through the folding of micro- and nano-patterned membranes [1]. For a number of applications, such as electrochemical energy storage devices and 3D photonic crystals [2], a simple stacking-type folding is required. For such a folding scheme, lateral alignment among folded layers is crucial. We have folded SU-8 membranes with less than 1 μm lateral alignment error using patterned pyramids and corresponding square openings that couple during the assembly process. The pyramids are formed first by filling in KOH-etched trenches in the silicon with SU-8, then by etching away the silicon in a XeF_2 -etch. As the top SU-8 layer is folded on top of the bottom layer (Figure 1), the square openings fit precisely over the pyramids, thereby providing lateral alignment as well as vertical spacing between layers. The scanning electron microscopy (SEM) image in Figure 2 shows the centered tip of the pyramid in relation to the square opening.

Lateral alignment precision must be on the order of 10 nm for devices such as photonic crystals and 3D integrated circuits. Other possible alignment techniques include alignment via hydrophobic/hydrophilic surfaces and using electrostatic or magnetic forces. These alignment structures are patterned via high precision lithography techniques, such as e-beam lithography, and the alignment system must produce sufficient forces to overcome other factors at this size scale, such as van der Waal's forces and surface tension. Lateral alignment is further improved by "elastic averaging," which occurs when a large array of alignment mechanisms work in parallel for greater alignment precision. We are pursuing a variety of methods to analyze the precision of the passive and active alignment schemes as well. The first method is to pattern visual markings on the membranes, such as cross-hatches and moiré patterns, that show the post-assembly lateral alignment under an optical microscope or SEM. Furthermore, device functionality will serve as a precise measure for alignment (e.g., a photonic crystal's band properties).

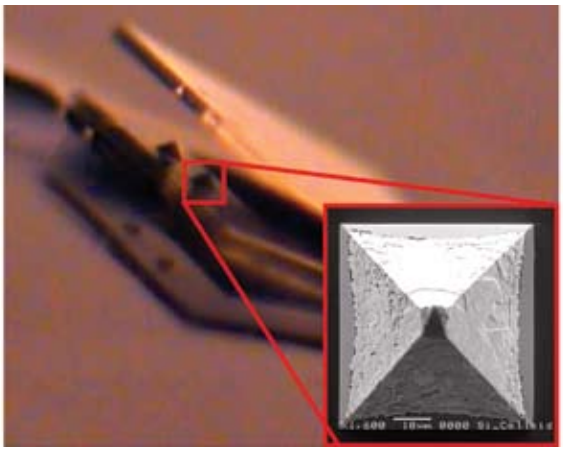

Figure 1: Partially folded SU-8 device with pyramid-shaped alignment features.

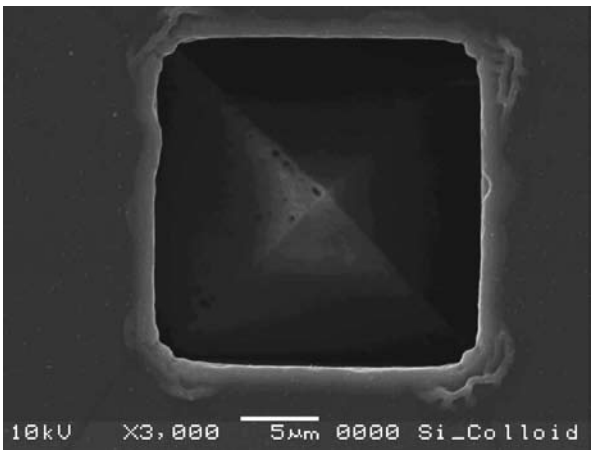

Figure 2: SEM image of a square opening fitted over a pyramid. Location of pyramid tip indicates sub-micron alignment.

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[2] In, H.J., W. J. Arora, S. Kumar, Y. Shao-Horn, H.I. Smith, G. Barbastathis, "Fabrication of 3D Nanostructures via Nanostructured Origami™ Process," *Second International Symposium on Nanomanufacturing*, Daejon, Korea, November 2004.

Nanostructured Origami™ 3D Fabrication and Assembly of Electrochemical Energy Storage Devices

H.J. In, S. Kumar, Y. Shao-Horn, G. Barbastathis
Sponsorship: MARCO IFC, ISN, NSF SGER

In the Nanostructured Origami™ 3D Fabrication and Assembly Process, 3D nanostructured devices can be made using exclusively 2D micro- and nano-fabrication tools [1]. The origami approach consists of first patterning 2D nanostructured membranes, then folding them to obtain the desired 3D shape. The fact that nanostructured surfaces can be oriented in any direction makes the Nanostructured Origami™ Process ideal for fabricating electrochemical energy storage devices, such as supercapacitors, [2] where it is desirable to have two nanostructured surfaces facing each other. In addition, because the origami method can be integrated with most existing fabrication processes, on-chip power supply integration becomes possible. Figure 1 shows the process flow for an origami supercapacitor. SU-8 serves as the structural material, and carbon paint deposited on top of gold acts as the electrode material. While the carbon paint itself is highly porous and can be considered a nanostructure, the gold surface underneath is patterned with small pyramids to further increase the total surface area (Figure 2). Initial electrochemical testing of the supercapacitor device shows that a large capacitance can be obtained from a device that takes up no more than 500 μm x 500 µm x 50 µm. Future work will include testing of multi-layered electrochemical devices that maintain a small areal footprint despite a very large surface area.

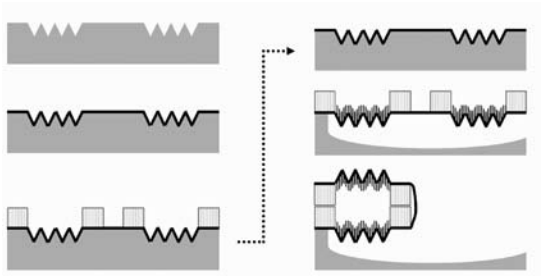

Figure 1: Process flow for SU-8 supercapacitors (gray = silicon, black = gold, light stripe = SU-8, dark stripe = carbon paint).

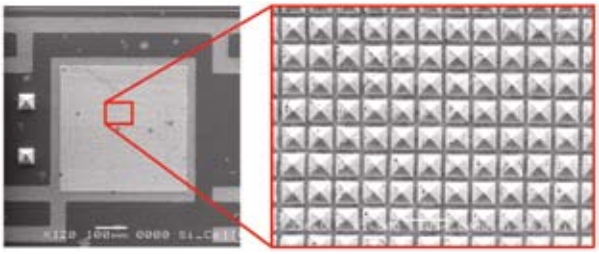

Figure 2: Scanning electron microscope image of 3 µm square pyramids that serve to increase the overall surface area of the electrode.

REFERENCES:

[1] In, H.J., W. Arora, T. Buchner, S.M. Jurga, H.I. Smith, G. Barbastathis, "The Nanostructured Origami™ 3D Fabrication and Assembly Process for nanomanufacturing," *Fourth IEEE Conference on Nanotechnology,* Munich, Germany, pp. 358-360, August 2004.

[2] In, H.J., W.J. Arora, S. Kumar, Y. Shao-Horn, H.I. Smith, G. Barbastathis, "Fabrication of 3D nanostructures via Nanostructured Origami™ Process," *Second International Symposium on Nanomanufacturing,* Daejeon, Korea, November 2004.

Stress Actuation Method for Folding Nanostructured Origami

W.J. Arora, H. Smith, G. Barbastathis
Sponsorship: MARCO IFC, DARPA, ISN

Nanostructured Origami describes a new idea for manufacturing 3D nanostructures on a silicon wafer. Nanometer-scale structures are best fabricated with various 2D lithography techniques. This project addresses the problem of how to build 3D structures using only 2D lithography. The general method of the Nanostructured Origami approach involves three steps: (1) lithographically define micrometer-scale membranes and hinges; (2) lithographically pattern nanostructures on these membranes; and (3) release the membranes and actuate the hinges to fold into a 3D shape.

We have developed a process to fold thin membranes of silicon nitride using stressed chromium hinges. The chromium is deposited with high tensile residual stress by vacuum evaporation, and the membranes are subsequently released with a KOH underetch. As the membrane is released, the chromium hinges self-actuate due to their stress. Figures 1 and 2 show experimental results of the folding process. For a given value of residual stress in the chromium, the hinge will curl with a predictable radius [1]. Therefore, the angle to which the membrane folds is proportional to the length of the chromium hinge (Figure 1). We have also demonstrated 180° folds (not shown).

Our current work is focused on nano-patterning the silicon nitride membranes with electron-beam lithography prior to releasing them. In addition, we plan to reduce the hinge radius of curvature by selectively thinning the silicon nitride at the hinge area. With these improvements, Nanostructured Origami becomes a tool well-suited for the fabrication of 3D nano-devices, including 3D photonic crystals and 3D ICs.

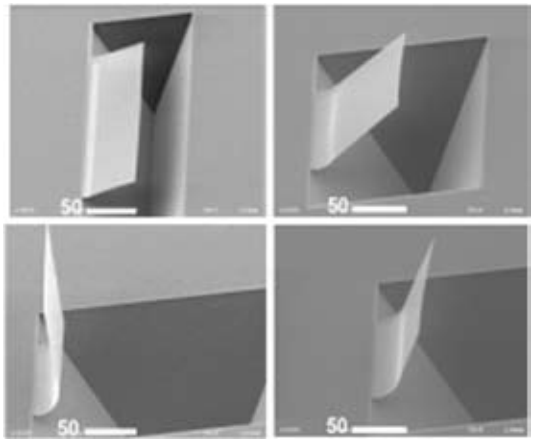

Figure 1: Clockwise from the top left, the lengths of the chromium hinges were (in μm):12, 27, 42, and 54. The angles at which they folded are approximately (in degrees) 20, 45, 70, 90.

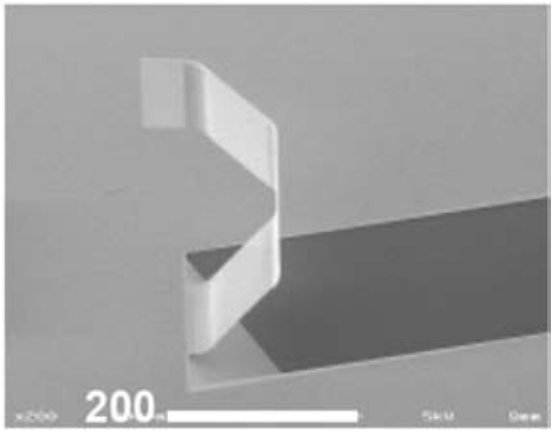

Figure 2: A device with four identical hinges.

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Mechanical Deformation of Neutrophils into Narrow Channels Induces Pseudopod Projection and Changes in Biomechanical Properties

B. Yap, R.D. Kamm

Sponsorship: National Heart, Lung, and Blood Institute (Program Project Grant)

Neutrophils traversing the pulmonary microcirculation are subjected to mechanical stimulation during their deformation into narrow capillaries. To better understand the time-dependant changes caused by this mechanical stimulus, we used microfabrication techniques to construct an *in-vitro* poly-dimethyl-siloxane (PDMS) system with dimensions comparable to the pulmonary capillaries. Because PDMS is optically transparent, it enabled direct observation of the neutrophil morphology, and simultaneously allowed us to employ the technique of multiple-particle-tracking microrheology to directly measure the viscoelastic properties of the cell. Above a threshold stimulus, mechanical deformation resulted in neutrophil activation with pseudopod projection. The activation time was inversely correlated to the rate of mechanical deformation experienced by the neutrophils. A reduction in shear moduli was observed within seconds after the onset of the mechanical stimulus, suggesting a sudden disruption of the neutrophil cytoskeleton when subjected to mechanical deformation. However, the magnitude of the reduction in moduli was independent of the degree of deformation. Recovery to nearly the initial values of viscoelastic moduli occurred within one minute. These observations confirm that mechanical deformation of neutrophils, similar to conditions encountered in the pulmonary capillaries is not a passive event; rather, it is capable of activating the neutrophils and enhancing their migratory tendencies.

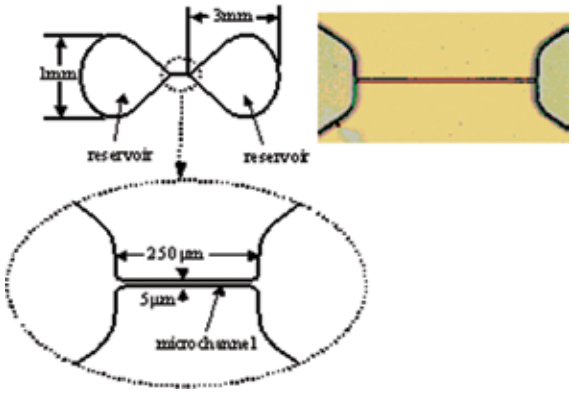

Figure 1: (Left) Schematic showing design of the PDMS microchannel and its connecting reservoirs. The microchannel section is enlarged to highlight the channel geometry, which has dimensions comparable to those of pulmonary capillaries. The microchannel height is about 1.5-2.5. Diagrams are not drawn to scale. (Right) Image of the microchannel as observed under a microscope.

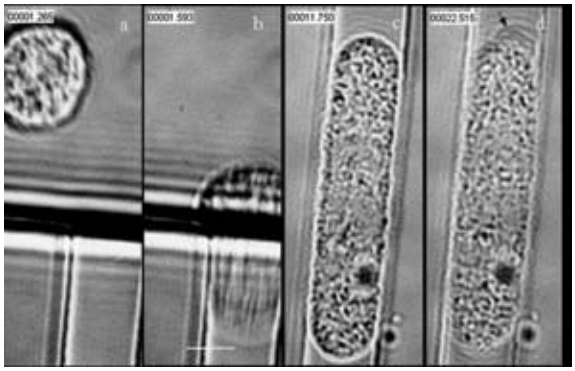

Figure 2: Image sequence showing a neutrophil flowing towards the microchannel entrance [panel (a)], the cell undergoing deformation [panel (b)], and subsequently, the neutrophil being trapped in the channel [panel (c)]. After some time, the cell can be seen to form pseudopod projection [panel (d)]. Arrow in panel (d) points to the location at the trailing edge of the cell where pseudopod protrusion was first seen. The granules in the cell were tracked to obtain the viscoelastic properties of the cytoplasm. Scale bar, 5.

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Field Ionization Array Micro-Gas Analyzer

L.F. Velásquez–García, L.Y. Chen, B. Andeoti, A.I. Akinwande
Sponsorship: DARPA

The Micro Gas Analyzer (MGA) project aims to develop the technology for real-time sensors intended for chemical warfare. The device is composed of four micro-fabricated subsystems: 1) an ionizer; 2) a mass filter based on a quadrupole [1]; 3) a species sensor based on a resonator [2]; and 4) a pump [3]. We are developing a field ionizer array based on gated CNTs. We plan to use arrays of CNTs because of their small radii, high aspect ratio, and gate proximity to ensure high fields at low voltage. State-of-the-art ionizers use electron impact ionization (thermionic cathodes), incurring in excessive power consumption, low current, current density, ionization efficiency, and short lifetime. Each of the proposed ionizer arrays - the impact and field - offer distinct advantages. The electron impact ionizer and field ionizer arrays both are more efficient and consume less power than thermionic cathodes, and variation of gate voltage in each improves specificity. The field ionizer, however, is based on the concept of electron tunneling (electrons tunnel in the outer shell of the molecule, due to the presence of high electric fields). Because of this, the field ionizer is able to soft-ionize species, thus achieving molecule ionization. The reliability and device lifespan of the field-tunneling ionizer is increased by biasing CNTs to the highest potential in the circuit, thus making it unlikely for ionized molecules to back-stream. In the case of the electron impact ionizer, the reliability and lifespan of the ionizer is improved by using a double gate.

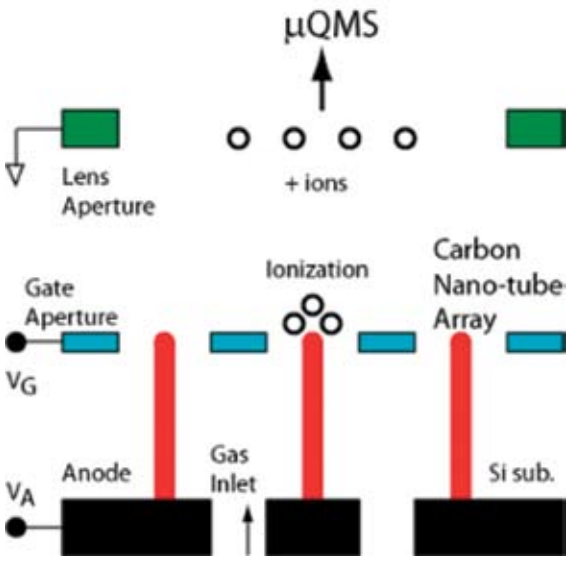

Figure 1: Schematic of a field ionizer array based on electron tunneling from the actual molecule to be ionized. Neutral molecules will lose an external electron if they get close enough to the CNT tip. The positive- biased CNT will repel the ion.

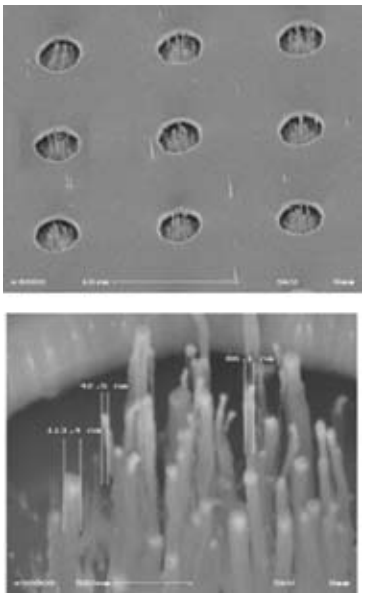

Figure 2: A single gated CNT array grown at MIT. The gate is made of poly-SSi, the insulator is thermal SiO_2. The CNT seed was Fe.

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Fast Separation of Biomolecules in a Nanofilter Array Chip

J. Fu, J. Han
Sponsorship: NSF-CTS, MIT Lincoln Laboratory

We report here the first microfabricated nanofilter array chip that can size-fractionate SDS-protein complexes and small dsDNA molecules based on the Ogston sieving mechanism [1] without using sieving matrices. Nanofilter arrays with a gap size of 40-180 nm were fabricated and characterized. Complete separation of SDS-protein complexes and small DNA molecules were achieved in several minutes with a separation length of 5 mm. The separation efficiency of the miniature nanofilter array chip is comparable to current state of the art systems (i.e., capillary gel electrophoresis). Our work here is the first direct experimental confirmation of Ogston sieving in a well-defined, regular nanopore system, and the nanofilter array chip is the first microfabricated, regular sieving system that can size-separate small biomolecules, such as proteins.

The nanofilter array chip is chemically and mechanically robust, and can be used over a long period without degradation of its characteristics. The nanofilter array chip allows the use of different buffer systems, and this opens up possibilities for integrating different biomolecule sensors and separation and reaction chambers in one single chip, without the concern of sieving matrix crosstalk and contamination. Therefore, the nanofilter array chip presented here is an important milestone toward a truly integrated proteomic sample-preparation microsystem that includes fully-integrated multiple separation and purification steps.

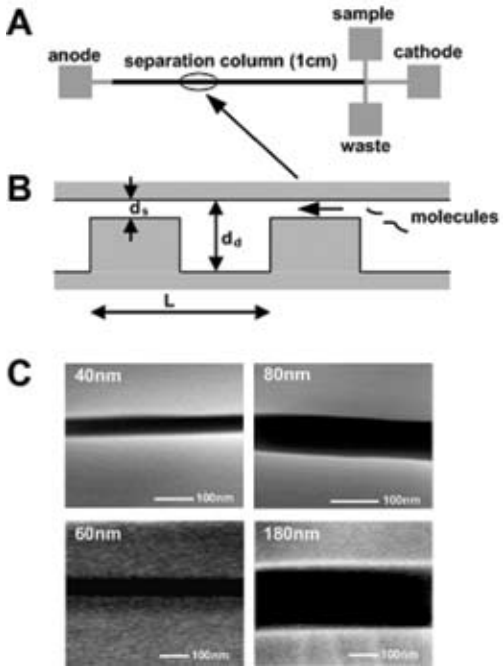

Figure 1: (A) Layout of the nanofilter array chip. (B) Schematic diagram of the nanofilter array. (C) Scanning electron microscope images of thin regions with different depths.

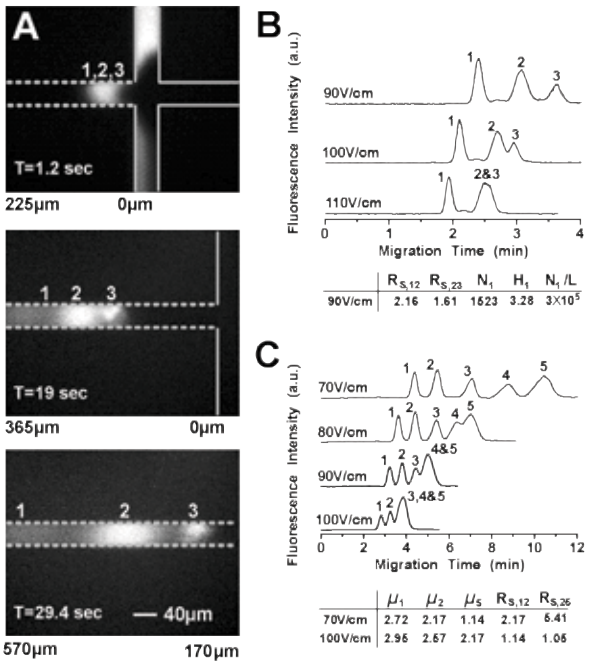

Figure 2: Fast separation of SDS-protein complexes (A) and (B) 1: cholera toxin subunit B, 11.4kDa; 2: lectin phytohemagglutinin-L, 120kDa; 3: low density human lipoprotein, 179kDa and small dsDNA molecules (C, PBR marker, 1: 50bp, 2: 150bp, 3: 300bp, 4:500bp, 5:766bp).

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Fabrication and Characterization of Nanofluidic Channels for Studying Molecular Dynamics in Confined Environments

P. Mao, J. Han, M. Previte, P.T.C. So, A.G. Balducci, P.S. Doyle
Sponsorship: MIT Lincoln Lab, NSF NSE and CAREER program

Hindered transport of macromolecules in liquid-filled pores is important to biological membrane processes associated with cell biology and medical physiology, chromatography, separation, and heterogeneous catalysis [1]. It is highly desirable to conduct well-controlled, model-based studies of molecular and fluidic transport process in a confined space. Compared to nanoporous track-etched membranes, micromachined nanofluidic structures offer unique advantages, including well-controlled physical and chemical properties, compatibility with various single molecule detection (SMD) methods, and easy integration to μTAS [2]. We characterized glass-glass and glass-Si bonding processes for the fabrication of nanofluidic channels as thin as 20 nm (Figure 1). We demonstrated that glass-glass nanofluidic channels as thin as 25 nm, with a high aspect ratio of 2000 (width to depth), can be achieved with this glass-glass bonding technique. We also found that silicon-glass nanofluidic channels, as thin as 20 nm, with an aspect ratio of 250, can be reliably obtained with the anodic bonding technique. Cross-sectional scanning electron microscopy (SEM) analysis after bonding was performed to prove that there is no significant change in the depth of the nanofluidic channels due to anodic bonding and glass-glass fusion bonding processes [3]. We examined the conformation and diffusion of a single λ-DNA molecule confined in a slit glass nanochannel using epifluorescence video microscopy (Figure 2(A)) [4]. The diffusivity is characterized as a function of the degree of chain confinement (depth of the channel). In addition, the effects of spatial confinement and surface boundary layer on the diffusivity of small biomolecules within a nanochannel are being investigated by two-photon fluorescence correlation spectroscopy (FCS), shown in Figure 2(B). The potential impact of this research would be significant, both scientifically and technologically, by offering a better understanding of molecular diffusion and transport in confined environments, as well as generating new concepts of molecular sorting and manipulation technology.

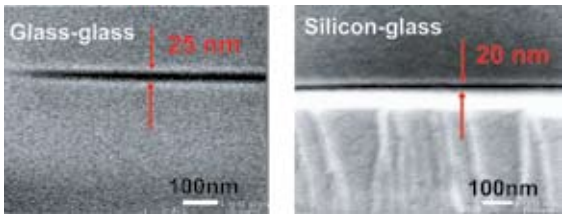

Figure 1: Cross-sectional SEM images of the 25 nm glass-glass channel (A) and 20 nm silicon-glass channel (B).

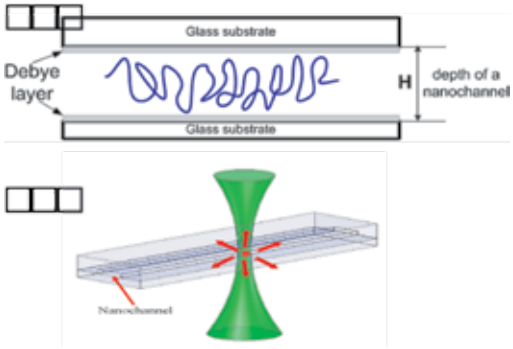

Figure 2: (A) Schematic diagram of a large DNA molecule confined to a slit glass nanochannel with a depth of H. (B) Schematic diagram of detecting single, small molecules by two-photo FCS in a slit nanochannel with vertical confinement.

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Millionfold Biomolecule Pre-Concentration Using Nano-fluidic Filters

Y.-C. Wang, J. Han
Sponsorship: NSF, MIT Lincoln Lab

In all biomolecule-sensing technologies, detection becomes increasingly difficult or impossible when the analyte concentration is lower than a certain level (the detection limit). However, in complex blood-serum samples, most of the important biomolecule markers are available only in trace amounts (fM to nM). Therefore, the detection (or identification) of these markers after pre-fractionation and separation is extremely difficult. To solve this problem, numerous efforts have been made to develop a pre-concentration process before or after separation. So far, the single pre-concentration method with the highest concentration factor among all the strategies is micellar electrokinetic sweeping, which can achieve a concentration factor of 500-to 7000-fold [1,2].

Here, we present a novel way to achieve rapid pre-concentration for a charged biomolecule that can achieve an up to 10 millionfold sample pre-concentration within 30 minutes. Ionic charge separation will happen once the electrical field is applied across the nanofilter. It has been reported that a flow several times stronger than general electroosmotic flow, caused by induced-charge layer, will present with confined geometry [3,4]. As a consequence, a barrier that can trap both positively and negatively charged molecules is formed by extending the Debye layer (non-equilibrium charge polarization) into the microfluidic channel with a stronger carrier flow. This device can concentrate a sample without a complex buffer concentration variation (such as in electrokinetic focusing), any additional additive (such as SDS in micellar sweep techniques), and/or any other complex structure that will make the downstream analysis difficult. Because of the device's simple structure, various integrations and applications are possible, including sample pre-concentration for advanced blood proteome analysis, sample injection for microchip electrophoresis/chromatography, and environmental trace analysis.

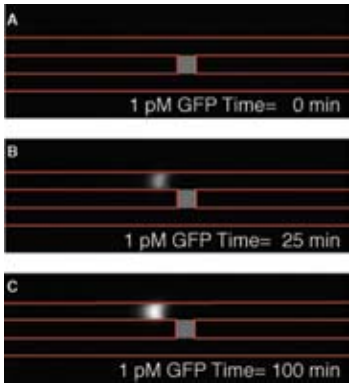

Figure: 1: Pre-concentration phenomena for 100 minutes, starting from highly diluted 33 pM (10-12M) GFP solution. The detection condition barely detects the 33 μM GFP concentration, which means at 25 minutes or later, the concentration of the plug exceeds 1 μM. Voltage applied across top-down channel is 10 volts, while 4 volts along the top channel (pictures were taken by CCD camera with 1 second exposure).

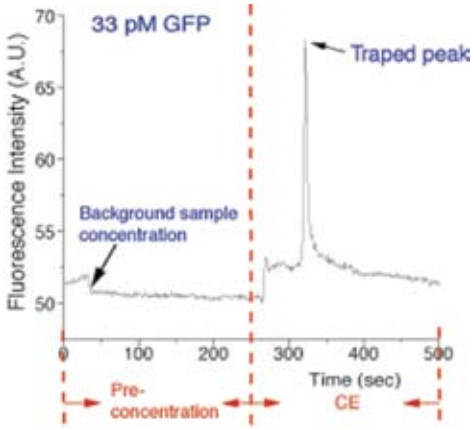

Figure: 2: Picture showing the electrokinetic capture/release profiles. After 250 seconds, the waster channel was floated to perform an EOF-driven CE in the top channel. Shown between 300 and 350 seconds is the releasing of captured proteins.

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A Nanoscanning Platform for Biological Assays

S. Kim, C. Muller-Falcke, S. Gouda, S.-G. Kim (Peter So group)
Sponsorship: IMC

Despite its success as an imaging tool for nanostructures, the existing atomic force microscopy (AFM) system does not reflect functionalities needed for biological applications well. One major problem with existing AFMs is slow imaging speed. Another problem is poor compatibility of the tip to the soft surface of biological specimens [1]. A nanoscanning platform is being developed at the Micro & Nano Systems Laboratory (MNSL). It has an in-plane structure with variable stiffness and a carbon nanotube tip (MWNT). Because of their superior mechanical and chemical properties, CNTs not only are ideal candidates for AFM tips, but they also are ideal for tip-enhanced raman spectroscopy (TERS). The variable-stiffness AFM can work as a tool for imaging and for placing the tip at the sub-nanometer proximity to a soft molecular-scale biological sample to enhance the Raman signals. The metal-coated CNT, or CNT filled with silver, gold or copper, which has a small diameter tip and high aspect ratio, is ideal for TERS. It is expected that the CNTs' plasmonic behavior with photons and the variable stiffness of the in-plane probe can further enhance Raman signals, thereby providing a high-enough sensitivity for the imaging of single molecular structures, such as proteins.

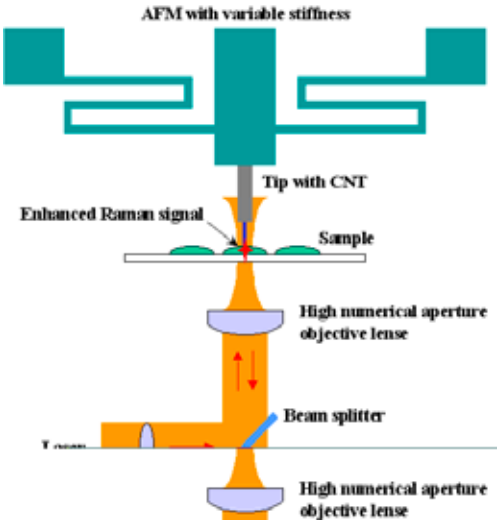

Figure 1: Schematic of TERS using an AFM with a CNT tip.

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Microfluidic Synthesis and Surface Engineering of Colloidal Nanoparticles

S.A. Khan, A. Günther, F. Trachsel, M.A. Schmidt, K.F. Jensen
Sponsorship: Microchemical Systems Technology Center

Metal oxide colloidal particles such as silica (SiO_2) and titania (TiO_2) have many diverse applications ranging from optical displays, catalysis, pigments, and photonic band-gap materials to immunological assays and health-care products. There has also been considerable research interest over the last decade in fabricating core-shell materials with tailored optical, structural, and surface properties. Core-shell particles such as titania-coated silica often exhibit improved physical and chemical properties over their single-component counterparts, and hence, are potentially useful over a broader range of applications. Newer methods of engineering such materials with controlled precision are required to overcome the difficulties with conventional production techniques, which are limited to multi-step batch processes. We have developed microfluidic routes for synthesis, separation, and surface modification of colloidal silica and titania particles. The two chief advantages of a microfluidic particle-engineering platform are: (1) precise control over reactant addition; and (2) mixing and continuous operation. Figure 1 shows a microfluidic chemical reactor for the continuous synthesis of colloidal silica particles [1]. We have also developed a microfluidic device for the electrophoretic separation of charged colloidal particles [2]. Figure 2(a) is a scanning electron micrograph of silica particles synthesized in the micro-reactor of Figure 1, operated in segmented gas-liquid flow mode. Figure 2(b) shows a silica nanoparticle coated with a thick shell of titania. Our ultimate goal is to enable continuous, multi-step colloid processing, with applications including synthesis and surface modification with biological macro-molecules or optical coatings.

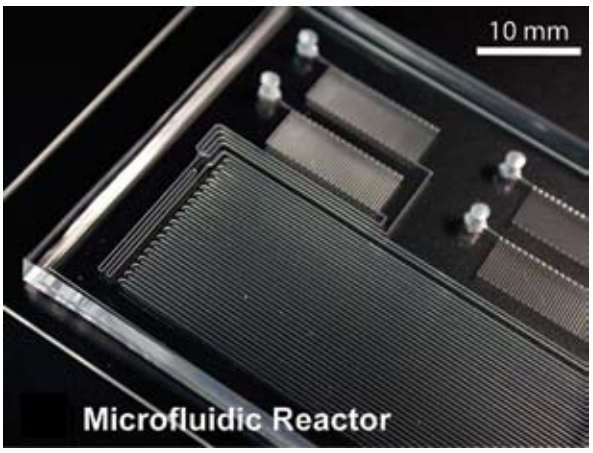

Figure 1: Microfluidic reactor for synthesis of colloidal silica, fabricated in PDMS.

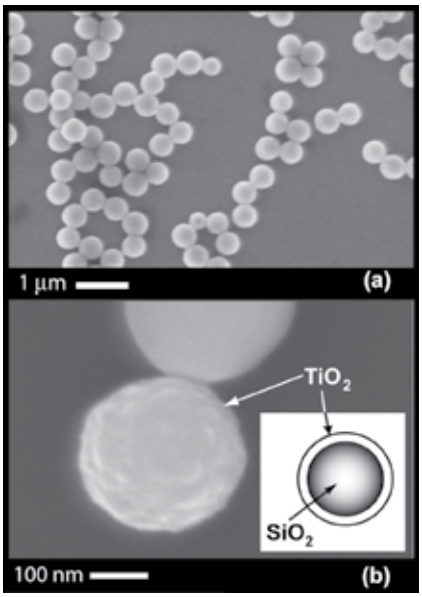

Figure 2: (a) Silica synthesized in micro-reactor and (b) titania-coated silica.

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Microreactors for Synthesis of Quantum Dots

B.K.H. Yen, A. Günther, M.A. Schmidt, M.G. Bawendi, K.F. Jensen
Sponsorship: Microchemical Systems Technology Center, NSF, ISN

We have fabricated a gas-liquid segmented flow reactor with multiple temperature zones for the synthesis of quantum dots (QDs). In contrast to the single-phase flow approach, the segmented flow approach enables rapid mixing and narrow residence time distributions – factors that have a strong influence on the ultimate QD size distribution. The silicon-glass reactor accommodates one reaction channel approximately one meter in length (hydraulic diameter ~400 μm), and two shallow side channels for collecting reaction aliquots (Figure 1). Two temperature zones are maintained, a heated reaction region (260°C) and a cooled quenching region (<70°C). As a model system, CdSe quantum dots with high quantum yields and low polydispersity are prepared using the reactor. Cadmium and selenium precursor solutions are delivered separately into the heated section. An inert gas stream is introduced further downstream to form a segmented gas-liquid flow, thereby rapidly mixing the precursors and initiating the reaction. The reaction is stopped when the fluids enter the cooled outlet region of the device. Under conditions for a typical synthesis, the gas and liquid segments are very uniform, and the QDs produced possess narrow size distributions, as indicated by the narrow line-widths in the photoluminescence spectra (Figure 2). The enhanced mixing and narrow residence time distributions offered by the segmented flow approach are generally desirable for nanoparticle synthesis, and we intend to apply the reactor to the preparation of other material systems.

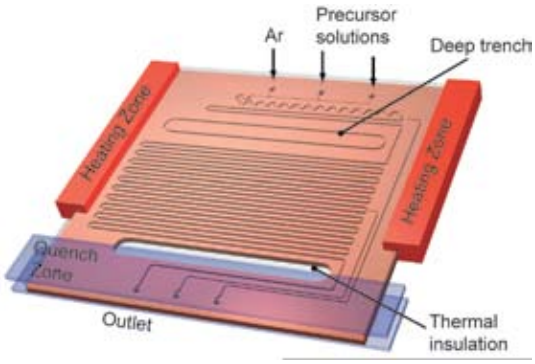

Figure 1: Diagram of the reactor with heated reaction and cooled outlet regions. A through-etch section ensures that the two regions are thermally isolated.

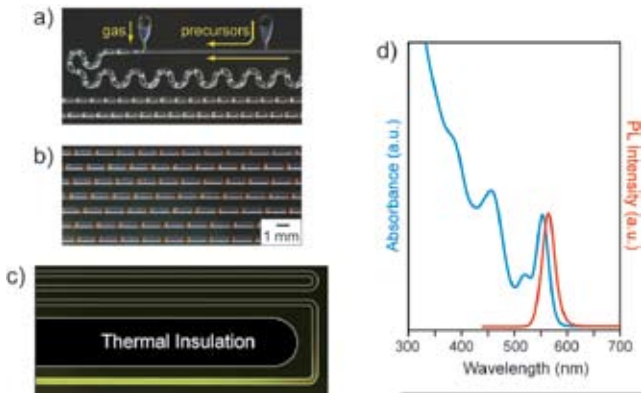

Figure 2: (a) and (b) Images of the heated inlet main channel sections of device during synthesis. Red segments: CdSe QD reaction solution. Dark segments: Ar gas. (c) Time-exposure image of the cooled outlet region under UV irradiation. At reaction temperature (260°C), the QD photoluminescence (PL) is completely quenched, but once the fluid reaches the cooled region (<70°C), yellow PL is observed. (d) Absorbance (blue) and photoluminescence (red) spectra of a typical QD sample prepared in the reactor.

Combinatorial Sensing Arrays of Phthalocyanine-based Field Effect Transistors

M. Bora, T. Heidel, M.A. Baldo, in collaboration with D. Schut (Hewlett-Packard)

Of the millions of molecular species floating in the air or dissolved in water, a substantial fraction can be smelled and uniquely discriminated [1]. Biological systems achieve this functionality with a multitude of non-specific receptors. In this project, we are developing gas sensors based on combinatorial arrays of organic transistors. The combinatorial approach reduces the need to develop specific receptors for each and every molecule of interest. Rather, our sensors are based on exploiting the wide variation in interactions between molecules and metal ions [2], an approach previously employed in colorimetric sensors [3].

We have fabricated gas-sensitive organic transistors each consisting of an approximately 10nm-thick polycrystalline layer of a metallophthalocyanine (MPC) with a gold source and drain contacts. The width and length of the channel for each transistor is 2mm and 50μm, respectively. The current-voltage characteristics of a typical MPC transistor are shown in Figure 1. The charge carrier mobility is typically between 10^{-3} and 10^{-4} cm^2/Vs but the transconductances of various MPC transistors (CoPC, CuPC, ZnPC, and NiPC) are observed to vary when exposed to different gases (acetone and methanol), generating a characteristic response signature for each gas. On interaction with the gas molecules, the energy levels of a given MPC may decrease, disrupting charge transport and possibly forming charge traps in the channel. In some cases, however, the current is observed to increase, possibly due to morphological changes in the channel or doping. Morphological changes in the channel may also lead to drain current instabilities that are typically observed in the first few minutes of operation. Since the sensors can be manufactured simply by inkjet printing on a patterned substrate, these sensors may find application as single-use diagnostic aids.

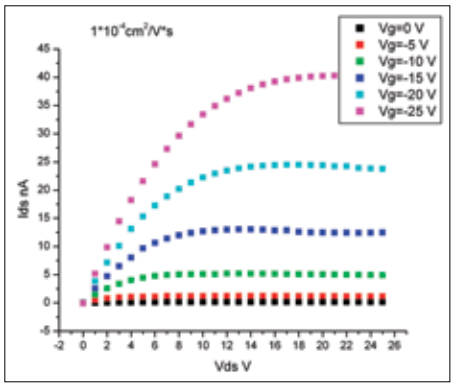

Figure 1: The current-voltage characteristics for a metallophthalocyanine (CoPC) transistor.

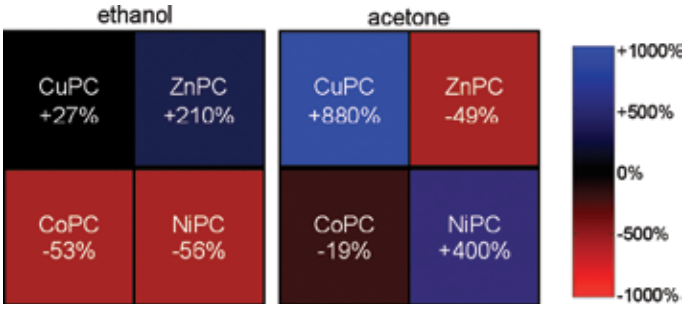

Figure 2: Changes in drain current for phthalocyanine-based organic transistors with V_{GS} = -25V when exposed to saturated vapors of ethanol (left) and acetone (right). The differing patterns are signatures of each gas.

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Electrical and Optical Characterization of Photosynthetic Complexes

M. Segal, M.A. Baldo
Sponsorship: DARPA/AFOSR, NSF Nanoscale Interdisciplinary Research Team

Photosynthetic protein complexes employ molecular components positioned with a precision beyond the limits of contemporary fabrication technologies [1] and achieve internal quantum efficiencies approaching 100%. We are optically and electrically characterizing reaction center complexes from R. sphaeroides to evaluate their usefulness in solid-state devices. The complexes are self-assembled into nanofabricated structures in an oriented fashion by selective binding of polyhistidine tags to Ni^{2+}-functionalized gold [2].

We have fabricated a field-effect transistor geometry (Figure 1) using a combination of photolithography, electron beam lithography, and electroplating to achieve source-drain separations comparable to the size of the complex. Complexes form the channel of the device. This geometry may provide insight into the transport that occurs inside the complex. We are also constructing a transparent, two-terminal structure using a poly(dimethylsiloxane) stamp for use in ultrafast optical pump and pump-probe measurements of self-assembled complexes under electrical bias. These measurements should yield the open circuit voltage and fill factor of these biological photovoltaic structures.

Once a test platform has been constructed, the protein complexes can be genetically engineered and the effects on performance and function quantitatively measured. For example, the complexes from R. sphaeroides have been modified to remove the H protein subunit as in Figure 2, allowing close contact to be made to the terminal electron acceptor in the internal electron pathway. This data will allow us to assess the prospects for functional molecular electronic devices based on biological models.

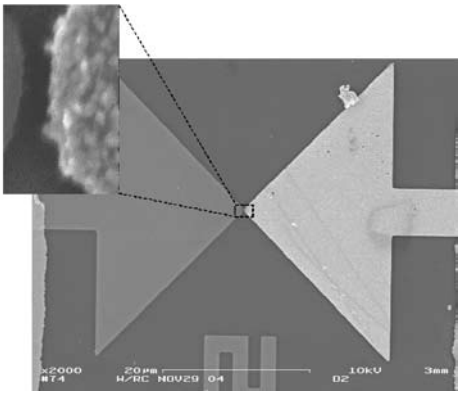

Figure 1: A field-effect transistor geometry test bed for studying protein complex function. The complexes are self-assembled into the channel.

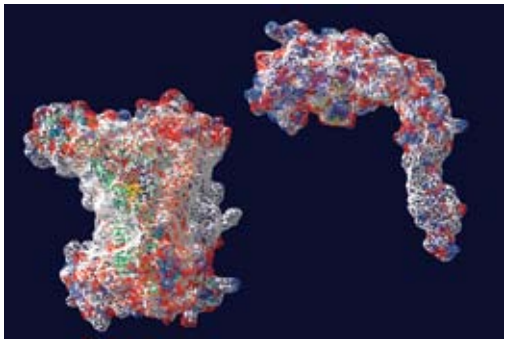

Figure 2: The protein complex from R. sphaeroides can be genetically engineered to remove the H protein subunit (right). Image courtesy of Nikolai Lebedev.

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Integration of Photosynthetic Protein Molecular Complexes with Organic Semiconductors

J. Mapel, M. Singh, M.A. Baldo
Sponsorship: DARPA/AFOSR, NSF Nanoscale Interdisciplinary Research Team

Over two billion years of evolutionary adaptation have optimized the functionality of biological photosynthetic complexes. Plants and photosynthetic bacteria, for example, contain protein molecular complexes that harvest photons with nearly optimum quantum yield and an expected power conversion efficiency exceeding 20%. The molecular circuitry within photosynthetic complexes is organized by a protein scaffold, at a density that cannot be matched by alternate technology. Indeed, if integrated with solid-state electronics, photosynthetic complexes may offer an attractive architecture for future generations of circuitry.

Stabilizing the complexes in an artificial environment is the key barrier to successful device integration [1]. We used novel surfactant peptides [2] to stabalize an oriented, self-assembled monolayer of reaction centers (RCs) found in *R. sphaeroides* (Figure 1). The same process worked with Photosystem I taken from spinach. Subsequently, an organic semiconducting protective coating was deposited as a buffer to prevent damage during fabrication of the top metal contact. Fabricating solid-state photodetectors and photovoltaic devices verified the functionality of the complexes. The internal quantum efficiency of the first generation of devices was estimated to be 12%. Successful integration was conclusively demonstrated by comparisons of the absorption spectrum and photocurrent spectra shown in Figure 2. Further work will harness the full (up to 1.1V) open circuit voltage of complexes, such as Photosystem I, and enhance the optical cross section of these devices.

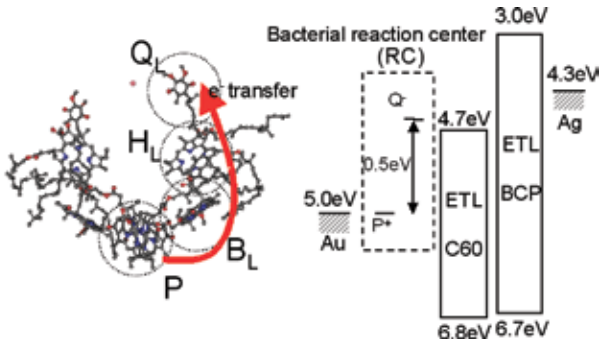

Figure 1: (left) The internal molecular circuitry of a photosynthetic bacterial reaction center with the protein scaffold removed for clarity. The complex is only a few nanometers top-to-bottom. After photoexcitation, an electron is transferred from the special pair, P, to the quinone, Q_L. The process occurs within 200 ps, at nearly 100% quantum efficiency, and results in a 0.5V potential across the complex. (right) Energy level diagram of an RC photovoltaic cell.

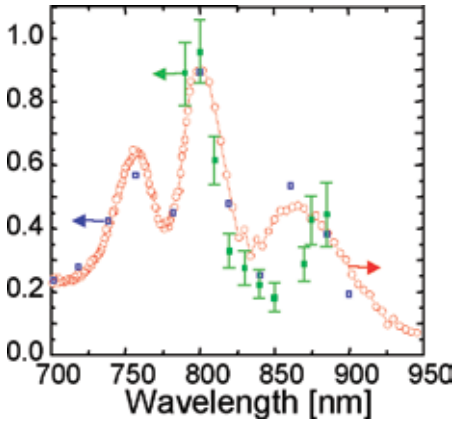

Figure 2: The photocurrent spectrum of solid-state photovoltaic devices employing bacterial reaction centers (RCs). A comparison between the photocurrent spectrum of solid-state (in green) and wet electrochemical cell devices (in blue), and the solution absorption spectrum of the bacterial reaction centers (in red), demonstrates that the observed photocurrent originates in the RCs.

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Interface Disorder and Charge Injection into Organic Semiconductors

B.N Limketkai, M.A. Baldo
Sponsorship: MARCO MSD

In this project, we examine the effect of structural disorder at the injection interface on the current-voltage (IV) characteristics of organic semiconductors. We find that structural disorder at the injection interface creates energetic disorder, which effectively generates deep interface traps that are observed to dominate the IV characteristics of these materials. For metal electrodes, interfacial energetic disorder is due primarily to variation in the image charge effect on a rough metal surface. Modeling the metal surface as self-affine fractal, we find that the standard deviation in the energy levels of the semiconductor is: $\sigma(z_0) \approx q^2 w/8\pi\varepsilon_r\varepsilon_0 z^2$, where z is the distance from the metal interface, w is the global rms roughness of the metal interface, q is the electron charge and $\varepsilon_r\varepsilon_0$ is the permittivity [1]. Most notably, for equally spaced molecular layers, the $1/z^2$ decay yields the ratio of standard deviations of transport energy levels in the first and second molecular layers, σ_1 and σ_2, to be 4. This result is *independent* of material parameters such as the surface roughness. The current density is determined by the rate of charge hopping from the interfacial layer to less disordered sites in the second molecular layer [2] as shown in Figure 1. Using the Marcus expression for charge hopping between Gaussian distributions gives a master equation: $J=J_0(V+\Delta V)^m/V_0^m$, where ΔV is the cathode doping-dependent voltage shift, and J_0 and V_0 are constants [1]. The power law slope $m=1+\sigma_1^2/(\sigma_2^2+2\lambda kT)$, where λ is the reorganization energy of the molecule. At low temperatures, the decay of energetic disorder gives a constant $m=1+\sigma_1^2/\sigma_2^2 \approx 17$.[1] In order to demonstrate the universality of the model, the IV characteristics of a wide variety of electron injection contacts are shown in Figure 2. The power law slope is constant at $m = (20\pm1)$ at 10K, independent of the choice of cathode or organic material.

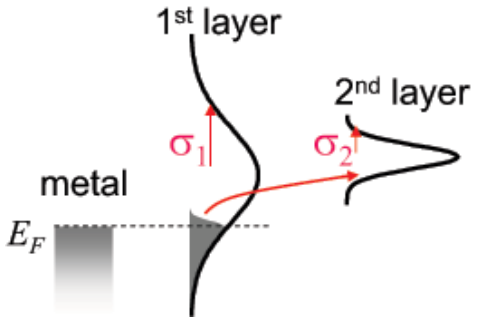

Figure 1: Charge injection when dominated by interface traps.

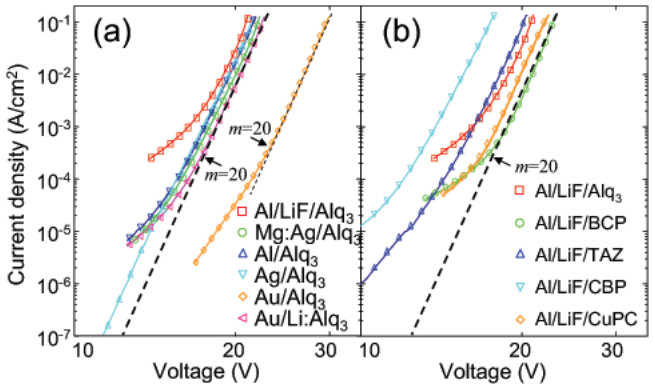

Figure 2: The IV characteristics at T = 10K for (a) Alq_3 interfaces, and (b), a comparison of Al/LiF contacts to Alq_3, BCP, TAZ, CBP, and CuPC. All cathodes exhibit similar power law behavior, i.e. $J \sim V^m$, where $m = (20\pm1)$, demonstrating that electron injection at these interfaces is not controlled by an energy barrier between the metal and organic semiconductor.

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Nanopattern-assisted Growth of Organic Materials for Device Applications

D. Mascaro, R. Tabone, V. Bulovic
Sponsorship: NSF, MARCO MSD

The challenge of generating crystals of organic materials has been pursued by many research groups who aim to develop materials sets for active electronic and optoelectronic devices, including field-effect transistors, photodetectors and optical modulators. We developed a method for in-plane growth of millimeter-scale crystalline organic needles from initially amorphous thin films of the molecular organic semiconductor tris(8 hydroxyquinoline)aluminum (Alq_3). The needles form when the vacuum-deposited amorphous films are exposed to chloroform vapor at room temperature and pressure, and can be as large as several microns thick, several microns wide, and one centimeter long (limited in length by the substrate dimensions). As such, the Alq_3 needles are more than 100 times longer than any previously reported organic crystals formed in the plane of the substrate. Moreover, the Alq_3 needles are spatially separated from one another and oriented with their long axes parallel to lithographically pre-defined periodic submicron grooves in the substrate surface.

The distinct facets (Figure 1b) and diamond-shaped cross sections (Figure 1c) of the fabricated Alq3 needles are indicative of crystallinity. The optical smoothness of the needle facets is evidenced in fluorescence micrographs that show waveguiding of the Alq3 fluorescence with outcoupling occurring at the needle edges and defects (Figure 1a). Polarized fluorescence measurements show a change in luminescence intensity with polarization angle, with a maximum at ~15 degrees from the long axis of the needle (Figure 2a). Fluorescence spectra of the crystal needles, obtained via confocal microscopy, peak at energy of 2.36 eV (peak wavelength of 525 nm) in agreement with the previously reported spectrum of polycrystalline Alq_3 (Figure 2b).

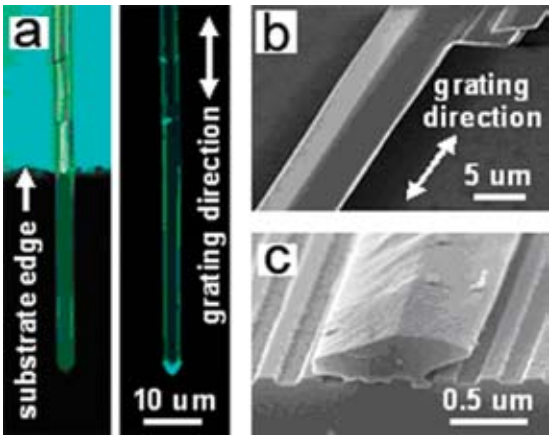

Figure 1: Alq_3 crystalline needles formed by exposure of amorphous Alq_3 thin films to chloroform vapor at room temperature. (a) Optical micrograph (left) and fluorescence micrograph (right, 365 nm excitation wavelength) of an Alq_3 needle that extends ~35 µm beyond the substrate edge. (b) Scanning electron micrograph (SEM) showing the distinct facets of an Alq_3 needle. (c) SEM showing the typical diamond-shaped cross section of an Alq_3 needle.

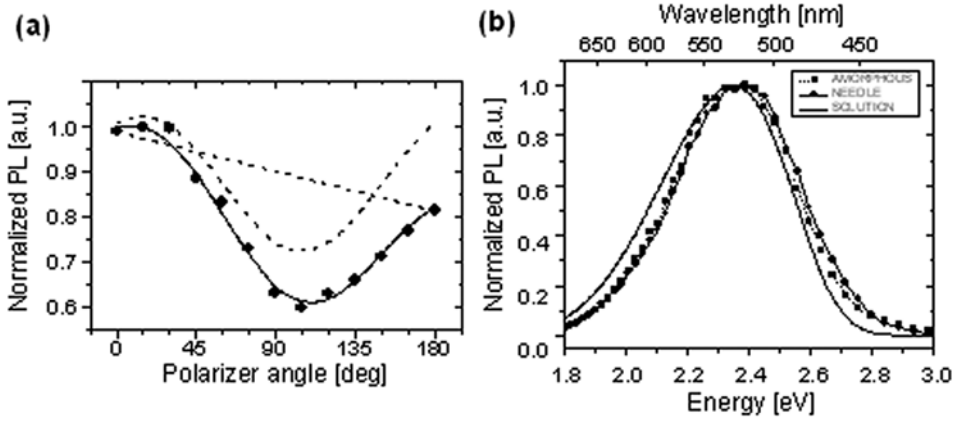

Figure 2: Fluorescence of Alq_3 needles. (a) Plot of the normalized photoluminescence (PL) intensity (365 nm excitation wavelength) as a function of polarizer angle, where 0 degrees corresponds to the polarizer aligned with the long axis of the needle. The decrease in fluorescence intensity from 0 to 180 degrees is due to gradual photooxidation of the Alq_3 during the measurement as indicated by the straight dashed line. The sinusoidal response of PL with polarizer angle and the composite of the PL response and the gradual oxidation are plotted in dashed and solid lines, respectively. (b) Fluorescence spectra (365 nm excitation wavelength) of an as-deposited Alq_3 thin film and an Alq_3 crystal needle, obtained via confocal microscopy. The solution fluorescence spectrum (408 nm excitation wavelength) of Alq_3 in chloroform is also plotted.

Fabrication of Polysilicon Electrode Pattern for Growing Aligned, Single-Wall Carbon Nanotubes

H. Son, Y. Hori, S.G. Chou, D. Nezich, G.G. Samsonidze, G. Dresselhaus, M.S. Dresselhaus
Sponsorship: NSF, Intel

Single-wall carbon nanotubes (SWNTs) are envisioned for a new form of electronic, optical, and chemical sensing devices. Two of the greatest challenges in integrating SWNTs with standard silicon technology are positioning them and aligning them. In this work, we present a new way of aligning and positioning the SWNTs in a regular array. The SWNTs are grown across two poly-Si electrodes, which serve both as electrical contacts and as elevated structures for suspending the SWNTs. The poly-Si electrodes are fabricated using standard silicon technology [Figure 1(a)]. First, a 1-μm-thick poly-Si film is grown by chemical vapor deposition (CVD) on top of a thermally-grown 1-μm-thick SiO_2 film on a silicon substrate. Then, photolithography and a reactive-ion etching are used to pattern the poly-Si film and the oxide film. The electrodes contain two regions: the narrow trench region (1~4μm wide) and the wide trench region (10μm wide), as Figure 1(b) shows. During the SWNT growth, a high electric field on the order of 10^6V/m can be selectively applied across the narrow trenches only. A high electric field is known to enhance the growth rate of SWNTs and to align them [1,2]. Moreover, controlling the maximum length of the SWNTs can guarantee that no suspended SWNTs grow across the wide trench [Figure 1(c)]. The SWNTs are grown directly on the sample by a methane-CVD process. Samples were prepared both with and without applied electric fields between the electrodes, as Figures 1(d) and 1(e) show. Using the presented electrode structure along with the electric field during the SWNT growth produces well-aligned SWNTs in a regular array.

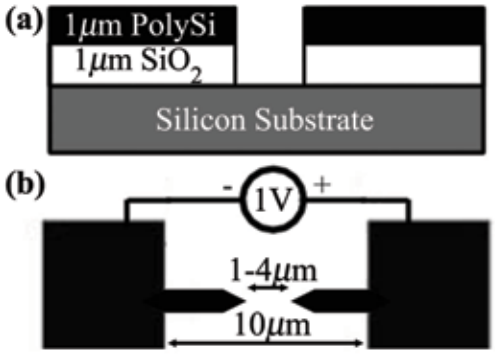

Figure 1: The schematic of (a) the side view and (b) the top view of the electrode structure.

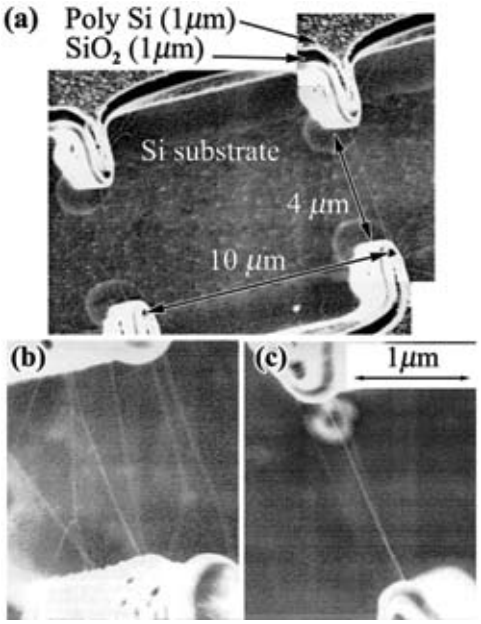

Figure 2: (a) and (c) Suspended SWNTs grown with an applied electric field. (b) Suspended SWNTs grown without an applied electric field. The magnification is the same for (b) and (c).

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Carbon Nanotube Machine Elements: Components of Small-scale, Compliant Mechanisms and Positioning Equipment

K. Lin, M. Culpepper

Sponsorship: Rockwell International Career Development Chair, NSF Nanomanufacturing Program

We are investigating the design and fabrication challenges that must be overcome to enable the use of carbon nanotubes (CNTs) as flexure hinges in small-scale compliant mechanisms (CMs) and machines. In CMs, motion is guided by the compliance of some or all of the mechanism's members. The CMs are not beam-like springs; rather, they are systems of compliant-rigid elements that combine to produce a mechanism capable of large and controlled motions in multiple degrees-of-freedom (DOF). These CMs do not require sliding, rolling, or other types of contact bearings (e.g., pin-in-hole prismatic joints) often found in rigid mechanisms. Therefore, CMs provide three unique advantages: 1) eliminate position inaccuracy due to friction; 2) eliminate joint wear and its affect on longevity; and 3) eliminate joint clearance that affects the mechanism's accuracy. The CNTs are attractive as flexure hinges, due to their large rotational capabilities and their high strain-strength characteristics in a kinked mode. Figure 1 shows the simulated shape of a kinked CNT [1]. The CNTs' deformation characteristics would enable CNT-based CMs to experience large deformations and, therefore, exhibit a range of motion that is much larger than that which could be obtained by traditional materials (e.g., silicon). CNT flexure hinges may then be combined with structural elements and nano-scale sensors, actuators, and electronics to form the core of next generation nanomechanical systems such as nano-scale positioners [2] and nano-scale end effectors [3, 4]. Figure 2 shows a concept for a single DOF device that is being examined. In Figure 2, CNTs form the rotational joints between the links of a mechanism. In the nascent stages of this work, we are generating a design theory, fabrication processes and testing processes required to develop small-scale, CNT-based machines for precision positioning.

Figure 1: Simulated bending of single wall CNT [1].

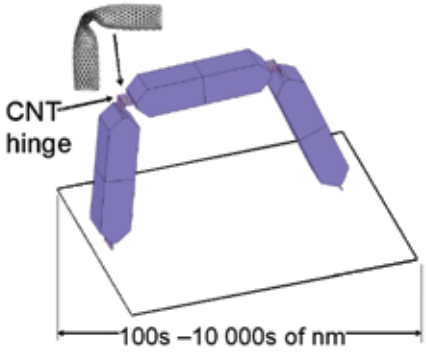

Figure 2: A CNT-based, four bar mechanism.

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[2] Chen, S., M.L. Culpepper, "Compliant Mechanisms for Micro-scale Spatial Manipulators: Applications in Nanomanipulation," *Nineteenth Annual American Society for Precision Engineering Meeting*, Orlando, FL, pp. 293-296, October 2004.

[3] Akita, S., Y. Nakayama, "Manipulation of Nanomaterial by Carbon Nanotube Nanotweezers in Scanning Probe Microscope," *Japaneese Journal of Applied Physics*, vol. 41, part 1, no.6B, pp. 4242-4245, Jun. 2002.

[4] Lee, J., S. Kim, "Manufacture of a Nanotweezer Using a Length-Controlled CNT Arm," *Sensors and Actuators A: Physical*, vol. 120, no. 1, pp. 193-198, April 2005.

Nanoelectromechanical Memories and Switches

K. Milaninia, M.A. Baldo
Sponsorship: MARCO MSD, ISN

The ability to change shape is a compelling attraction of molecular semiconductors. Compared to rigid inorganic materials, molecules are soft and malleable, and their conformational changes are essential to the functionality of biological systems. Applications of nano-electromechanical (NEM) molecular devices include memories and transistors. Information can be stored in the conformation of molecules, potentially leading to very high density memories, and molecular transistors that change shape under bias could exhibit subthreshold slopes of << 60 mV/decade [1]. Indeed, as an example of the potential of NEMs, voltage-gated ion channels possess subthreshold slopes of approximately 15 mV/decade [2].

Although many materials are available for NEM applications, carbon nanotubes exhibit low resistance and good mechanical properties. In this project, we are constructing a NEM testbed. The proposed design for our relay is shown in Figure 1. Nanotubes are directly grown at the bottom of a electron-beam defined trench etched in Si. This offers better control over the nanotubes and removes the need for additional steps that are required for the removal of surfactants and organics from the surface of the nanotubes. Because the nanotubes are vertically oriented, we are able to take advantage of the smallest size feature of the carbon nanotube: its diameter. This allows us to create dense arrays of relays for applications such as memory or logic devices. The vertical orientation allows NEM structures with very large aspect ratios. Theoretical results [3] have shown that increasing the aspect ratio of a carbon nanotube reduces the voltage needed to pull in the nanotube, thereby reducing the power requirement. Furthermore, because of the ability to easily functionalize the surface of nanotubes, we can functionalize the tube with charge to lower the pull-in voltage even further.

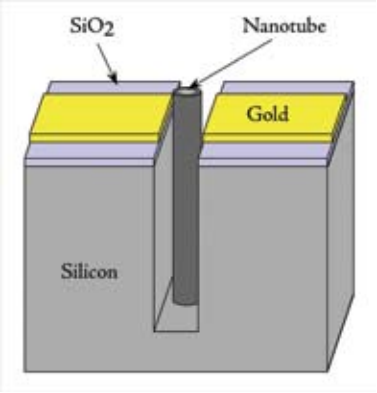

Figure 1: Schematic of the proposed device.

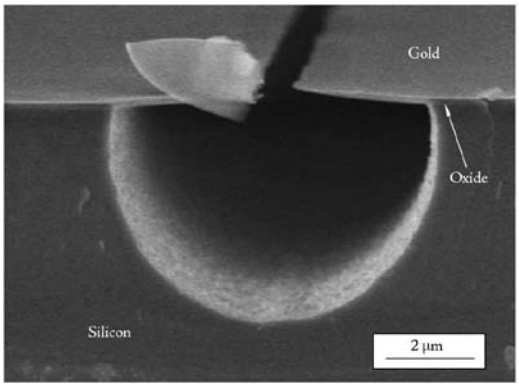

Figure 2: Actual device without nanotube.

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[1] Ghosh, A.W., T. Rakshit, S. Datta, "Gating of a Molecular Transistor: Electrostatic and Conformational," *Nano Letters*, vol. 4, no. 4, pp. 565-568, 2004.

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[3] Dequesnes, M., S.V. Rotkin, N.R. Aluru, "Calculation of Pull-in Voltages for Carbon-Nanotube-Based Nanoelectromechanical Switches," *Nanotechnology*, vol. 13, no. 1, pp. 120-131, February 2002.

Carbon Nanotube Rings for Interconnect and Device Applications

B. Wunsch, T.M. Wu, F. Stellacci, R. Reif
Sponsorship: NSF, MARCO IFC

Carbon nanotube rings have potential applications for both CMOS interconnects and devices. As copper interconnect dimensions shrink, the copper bulk resistivity is expected to increase due to surface scattering effects. An alternative to standard copper interconnects is to use carbon nanotubes, which have demonstrated ballistic transport properties and high achievable current densities.

We are currently investigating a method by which pre-grown carbon nanotubes are assembled onto a surface to form an interconnect structure. One of the key steps to achieving carbon nanotube interconnects through this self-assembly method is a suitable purification procedure. The fact that carbon nanotube rings demonstrate magnetic behavior provides us with a relatively simple and undamaging way to separate the magnetic, nanotube-containing fraction of a particular sample from the nonmagnetic, undesirable material. In addition, we are investigating the possibility of using these carbon nanotube rings as inductors in CMOS circuits. We have observed carbon nanotube rings with diameters in the range of hundreds of nanometers. Because current state-of-the-art CMOS metal inductors are generally tens to hundreds of microns in size, if these nanotube rings are suitable for inductor applications, we can achieve a dramatic improvement in device density.

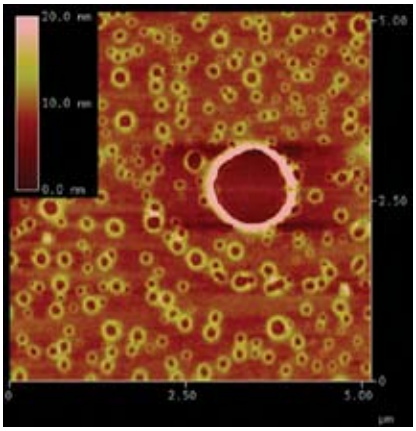

Figure 1: Tapping-mode atomic force microscope height image of single-walled carbon nanotube rings.

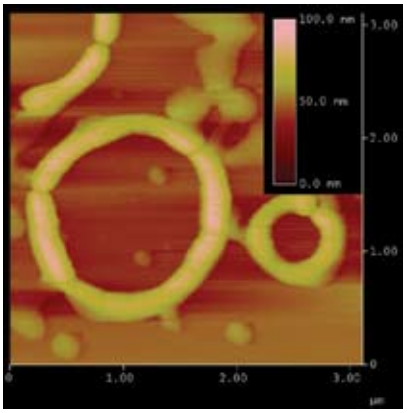

Figure 2: Tapping-mode atomic force microscope height image of multi-walled carbon nanotube rings.

Measuring Thermal and Thermoelectric Properties of Single Nanowires

C. Dames, C.T. Harris, G. Chen, in collaboration with M.S. Dresselhaus (MIT), Z.F. Ren (Boston College), J.P. Fleurial (JPL)
Sponsorship: Department Of Energy

Knowledge of nanowire thermal and thermoelectric properties will be important for the thermal management of nanowire devices (optoelectronic, sensing, and computing) and essential for the design of nanowire thermoelectric materials. For nanowire diameters smaller than the bulk mean free path of heat carriers, theory predicts that the thermal conductivity of nanowires will be reduced when compared to similar bulk materials [1, 2]. To experimentally verify these predictions, we are exploring several systems to measure the physical properties of single nanowires.

Our current work includes a basic platform to measure the thermal conductivity and specific heat of electrically conducting nanowires, such as the microfabricated metal lines shown below in Figure 1. Joule heating of a suspended nanowire with thermally clamped ends results in a temperature rise of the nanowire due to its finite thermal resistance. This temperature rise can be measured by resistance thermometry (again using the nanowire) and used to calculate its thermal conductivity and specific heat. This technique is being adapted for an in-situ transmission electron microscopy (TEM) measurement. If successful, this method will permit high-throughput physical property measurements of many nanowires of various geometries and morphologies, and allow correlations with their atomic structure as determined by TEM.

Microfabricated metal lines can also be employed to measure electrically insulating nanowires. Using electron beam lithography, a metal heater line is fabricated such that a target nanowire crosses the center of the line. With the nanowire and heater thermally anchored, the nanowire removes a fraction of heat from the heater line. This reduces the heater's temperature rise, and thus makes it possible to calculate the thermal resistance of the nanowire.

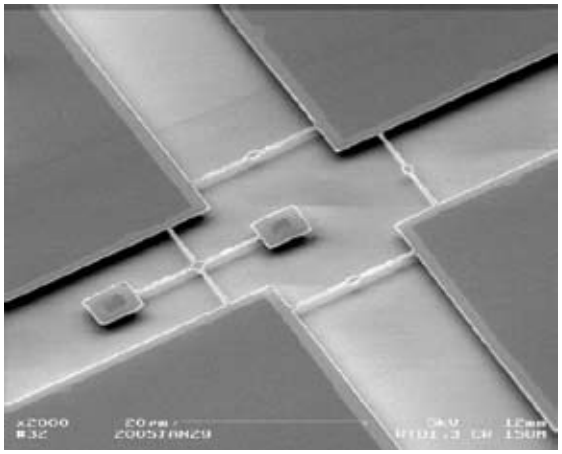

Figure 1: Microfabricated metal heater lines suspended 1.0 μm above the substrate, for thermal property measurements.

REFERENCES:

[1] Dames, C., G. Chen, "Theoretical Phonon Thermal Conductivity of Si/Ge Superlattice Nanowires," *Journal of Applied Physics*, vol. 95, no. 2, pp. 682-693, January 2004.

[2] Chen, G., Nanoscale Energy Transport and Conversion, New York: Oxford University Press, 2005.

Growth of High-quality Single-walled Carbon Nanotube Films on Flat and Microstructured Silicon Substrates

A.J. Hart, A.H. Slocum

Sponsorship: MIT Deshpande Center, Fannie and John Hertz Foundation

With the outstanding mechanical, electrical, thermal, and optical properties of carbon nanotubes (CNTs) now widely established [1,2], there is an emerging need for materials and methods that integrate carbon nanotubes as thin-films in standard microelectronic and micromechanical fabrication processes. We have developed a simple, versatile, and repeatable method for growing high-quality CNTs on silicon substrates by atmospheric pressure thermal chemical vapor deposition (CVD), from an $Mo/Fe/Al_2O_3$ catalyst film that is deposited entirely by electron beam evaporation. High-density single-walled CNT films having a Raman G/D ratio of at least 20 are grown over a temperature range of 750-900 °C. Within a broad parametric study, the highest yield is obtained from a mixture of approximately 20%/80% H_2/CH_4 at 825 °C. We also observe a novel growth behavior on long samples in pure CH_4, where the quality and density of the CNTs change distinctly as the chemistry of the gas evolves with the flow of the boundary layer along the sample. We demonstrate that simply placing another piece of silicon wafer as a "cap" over the catalyst-coated sample further increases the yield and quality of CNTs and enables uniform growth over large substrate areas, where the gas flow is limited by diffusion between the cap and the sample.

Using the same catalyst deposition and CVD processes, we also grow uniform CNT films on a variety of silicon microstructures, including vertical sidewalls fabricated by reactive ion etching and angled surfaces fabricated by anisotropic wet etching. Comparative experiments suggest that molybdenum (Mo) is critical for high-yield SWNT growth from Fe in H_2/CH_4, yet leads to poor-quality multi-walled CNTs (MWNTs) in H_2/C_2H_4. An exceptional yield of vertically-aligned MWNTs is obtained using Fe/Al_2O_3 in H_2/C_2H_4. These results emphasize the synergy between the catalyst and gas activity in determining the morphology, yield, and quality of CNTs grown by CVD, and enable direct growth of CNTs in microsystems for a variety of applications.

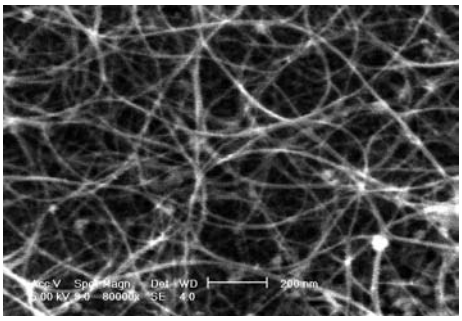

Figure 1: A CNT film grown using 80%/20% CH_4/H_2 at 825 °C, from $Mo/Fe/Al_2O_3$ catalyst deposited on polished (100) Si.

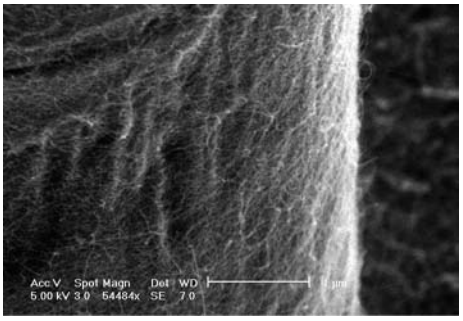

Figure 2: A CNT film grown on vertical sidewall of silicon post etched in STS-DRIE.

REFERENCES:

[1] Baughman, R.H., A.A. Zakhidov, W.A. de Heer, "Carbon Nanotubes - The Route Toward Applications," *Science*, vol. 297, pp. 787-792, 2002.

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Carbon Nanotube Modification and Characterization

T.M. Wu, F. Stellacci, R. Reif
Sponsorship: MARCO IFC

We are currently investigating the modification and characterization of carbon nanotubes for CMOS interconnect applications. Due to surface scattering effects, the amount of copper increases dramatically as interconnect dimensions shrink the bulk resistivity of the state-of-the-art material. As a result, efforts are being made to find alternative interconnect solutions. One promising candidate is carbon nanotubes because of to their potential ballistic transport properties and resistance to electromigration. However, many obstacles must be overcome for carbon nanotube interconnects to become viable. One of these obstacles is the formation of the actual interconnect structure.

There are two methods to form a carbon nanotube structure on a surface (Figure 1). The first method is to directly grow the nanotubes on the surface in the desired pattern. The second method is to assemble already-grown nanotubes into a pattern on the surface. Our work focuses on developing a process for the second method, self-assembly of nanotubes onto a patterned surface (Figure 2). The proposed process consists of four steps: purification, modification, patterning, and self-assembly. In the first step, we purify the raw as-grown nanotubes by removing amorphous carbon and metal catalyst particles. Next, we modify the purified nanotubes with a chemical handle. Thirdly, we use a complementary chemical handle to write a pattern on the surface. Finally, the nanotubes are assembled onto the surface, driven by the interaction between the chemical handles. We are currently developing a suitable nanotube purification technique and testing different chemical reactions for the nanotube modification and handle-surface interactions.

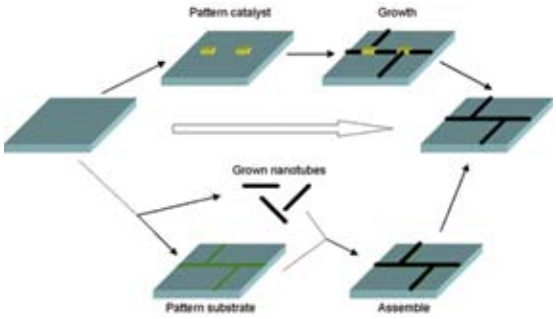

Figure 1: Two routes to carbon nanotube interconnects: direct growth (top) and directed assembly (bottom).

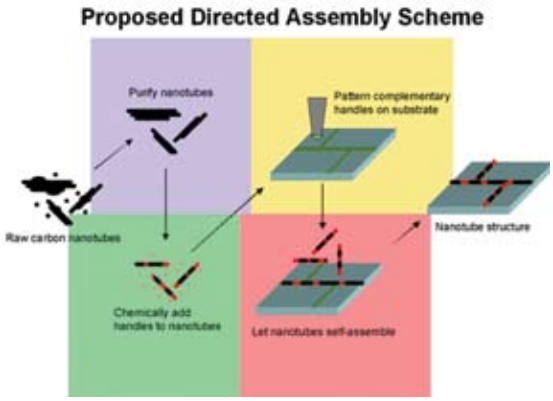

Figure 2: Our proposed four-step assembly scheme.

High-concentration Dispersion of Single-wall Carbon Nanotubes

Y. Sabba, E.L. Thomas
Sponsorship: Cambridge-MIT Institute

We report a novel method to exfoliate and disperse single-wall carbon nanotubes (SWNTs) into organic and aqueous solutions. The method is based on treatment of SWNTs with a solution of hydroxylamine hydrochloric acid salt [$(NH_2OH)(HCl)$] and does not require truncation of the tubes or surface absorption of organic molecules. The solution-dispersed tubes can easily be incorporated into an organic matrix in order to obtain a nanocomposite. We illustrate the method by forming PMMA-SWNT and PS-SWNT nanocomposites. One percent of the SWNT-PMMA nanocomposites, having a draw ratio of ~6, showed a dramatic six times increase in the strain to fracture, compared to fibers of similar draw ratio made from pure PMMA [1].

REFERENCES:

[1] Sabba, Y., E.L. Thomas, "High-Concentration Dispersion of Single-Wall Carbon Nanotubes," *Macromolecules*, vol. 37, no. 13, pp. 4815-4820, 2004.

Catalyst Engineering for Controlled Growth of Carbon Nanotubes

G.D. Nessim, R. Krishnan, C.V. Thompson
Sponsorship: MARCO IFC

A major challenge in carbon nanotube (CNT) growth is the ability to control the density, type, and position of the nanotubes. One possible approach to obtain CNTs with the desired properties is to engineer the catalyst. We are developing various techniques for templated assembly of ordered arrays of metallic nanodot catalysts. In one technique, perfectly ordered porous alumina is used to create nanodots at the bases of the pores, and nanotubes are grown in a porous alumina scaffold. This process allows production of large ordered arrays of dots and tubes in a scaffold that prevents tube agglomeration and provides a platform for testing of tubes in devices. With this and other techniques, we are prepared to investigate the variations of the properties of the dots themselves, as well as correlate them with corresponding variations in tube properties. We have developed a versatile system for thermal chemical vapor deposition (CVD), and we are investigating growth on patterned and unpatterned catalysts. Catalysts are characterized using X-ray analysis and electron microscopy techniques, and nanotubes are characterized using electron microscopy and Raman spectroscopy. We are also investigating the thermal chemical pretreatment of the catalysts, both with and without nanotube growth.

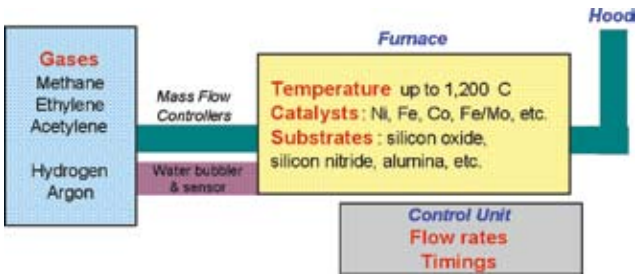

Figure 1: Thermal CVD apparatus for study of carbon nanotube growth with engineered catalysts.

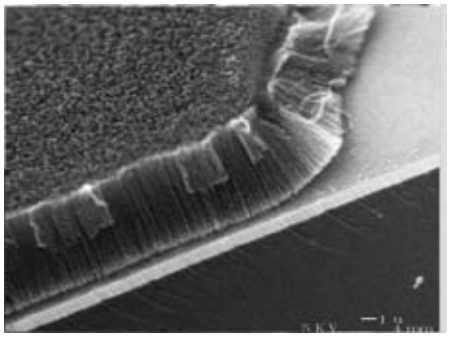

Figure 2: CNT "carpet," grown with thermal CVD. Substrate: Si/SiO_2. Catalyst: Al_2O_3/Fe (100 nm/1 nm). CNT growth at 750°C for 15 minutes. Gases: Ar/H_2 600/400 sccm (through water bubbler). [1]

REFERENCES:

[1] Hata, K., D.N. Futaba, K. Mizuno, T. Namai, M. Yumura, S. Iijima, "Water-Assisted Highly Efficient Synthesis of Impurity-free Single-walled Carbon Nanotubes," *Science*, vol. 306, no. 5700, pp. 1362-1364, November 2004.

Multiple Transistor Devices and Functional Building Blocks on a Single Carbon Nanotube

D.A. Nezich, J. Kong
Sponsorship: EECS

Single-walled carbon nanotubes are promising for future high performance electronics owing to their unique properties, including ballistic transport and compatibility with high-*k* dielectrics. High performance p-type and n-type nanotube field effect transistors (FETs) have been demonstrated [1,2]. So far, most of these studies are based on one transistor per nanotube. We plan to take this research a step further by building multiple devices on one single tube, then eventually building a functional block with complementary tube FET devices. With all the devices made from the same nanotube, we will systematically compare their performance dependence on gate dimensions, contact area, and other parameters. Device characteristics based on nanotube size and chirality will also be evaluated.

REFERENCES:

[1] Javey, A., J. Guo, Q. Wang, M. Lundstrom, H. Dai, "Ballistic Carbon Nanotube Field Effect Transistors," *Nature*, vol. 424, no. 6949, pp. 654-657, August 2003.

[2] Javey, A. *et al.*, "High Performance N-type Carbon Nanotube Field Effect Transistors with Chemically Doped Contact," *Nano Letters*, vol. 5, no. 2, pp. 345-348, February 2005.

Investigation of the Synthesis of Carbon Nanotubes

A.R. Cecco, J. Kong
Sponsorship: MARCO IFC

The unique electrical and structural properties of single-walled nanotubes (SWNT) make them very good alternative candidates for interconnect applications. In this project, we will carry out systematic studies on nanotube chemical vapor deposition (CVD) synthesis, with the goal of using nanotube CVDs as interconnects for integrated circuits in the future. Due to the large kinetic inductance in nanotubes, bundles of densely packed SWNTs are more suitable for this application instead of individual SWNTs [1]. However, successfully synthesizing bundles of SWNTs of uniform sizes, as well as controlling their location and orientation, is currently a challenge. The recent result of growing well-aligned SWNTs with H_2O as a weak oxidizer seems very promising [2]. We plan to investigate the H_2O-assisted synthesis of SWNT bundles, first in the vertical geometry, then in the planar geometry on the surface. In addition, we will study the synthesis of individual nanoparticles to understand the growth mechanism of nanotube synthesis.

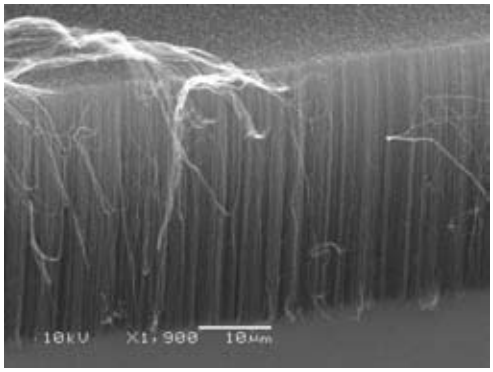

Figure 1: Scanning electron microscope image of vertically aligned nanotubes by H_2O-assisted CVD synthesis.

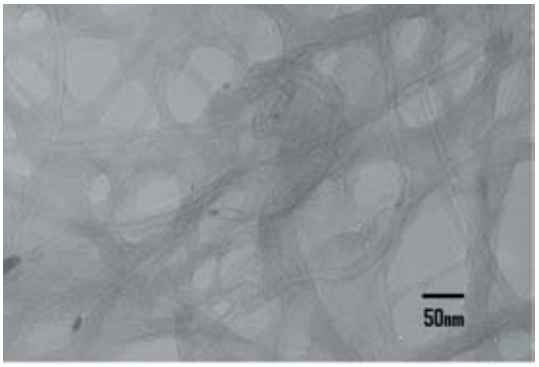

Figure 2: Transmission electron microscope image indicating that these nanotubes are mainly SWNTs; however, there is a significant amount of amorphous carbon present in the sample at the current stage.

REFERENCES:

[1] Naeemi, A., R. Sarvari, and J.D. Meindl, "Performance Comparison between Carbon Nanotube and Copper Interconnects for Gigascale Integration," *IEEE Electron Device Letters,* vol. 26, no. 2, pp. 84-86, February 2005.

[2] Hata, K. *et al.*, "Water-Assisted Highly Efficient Synthesis of Impurity-free Single-walled Carbon Nanotubes," *Science,* vol. 306, no. 5700, pp. 1362-1364, November 2004.

Carbon Nanotube Assembly by Nanopelleting

S.D. Gouda, S.-G. Kim
Sponsorship: Intelligent Microsystems Center

We have developed a manufacturing process termed nanopelleting [1,2], which enables large-scale handling and long-range order assembly of individual carbon nanotubes (CNTs). This technique includes vertically growing single-strand CNTs, embedding a CNT into a polymeric pellet, separating the pellet, and transplanting a CNT. CNTs are grown vertically, both individually and in bunches, on the patterned catalytic metal using a Plasma Enhanced Chemical Vapor Deposition (PECVD) machine built by us at MIT (Figure 1). The machine's key feature is the control of the substrate temperature during the growth process. Three thermocouples are connected at the bottom of the ceramic heater to measure the temperature, which is controlled by the heater controller. Plasma is formed between an anode and cathode by applying a DC voltage, which then decomposes acetylene into carbon that deposits below the Ni catalyst and leads to the formation of carbon nanotubes. The process sequence to make pellets containing single strand CNTs is shown in Figure 2. The steps involved in pellet-making process include: (1) coating the silicon wafer with polymethyl methacrylate (PMMA); (2) exposing the photo resists using Raith 150 to obtain the desired patterns (by varying the aperture size, dose, electric field, and developing photo resist); (3) depositing Ti/Ni (25nm) then lifting-off the resist to obtain Ni catalyst nanodots; (4) growing single-stranded CNTs in the PECVD machine with optimized process conditions; (5) spin-coating SU-8 to form a thickness of 25μm on the isolated CNTs; and (6) exposing this SU-8 layer to UV light using an appropriate mask, which forms the nanopellets. The nanopellets are released from the silicon substrate by manually breaking them with a spark needle. We are also developing an in-plane Atomic Force Microscope (AFM) probe with CNT tips assembled mechanically to aid in this process.

Figure 1: PECVD Machine for growing CNTs at MIT

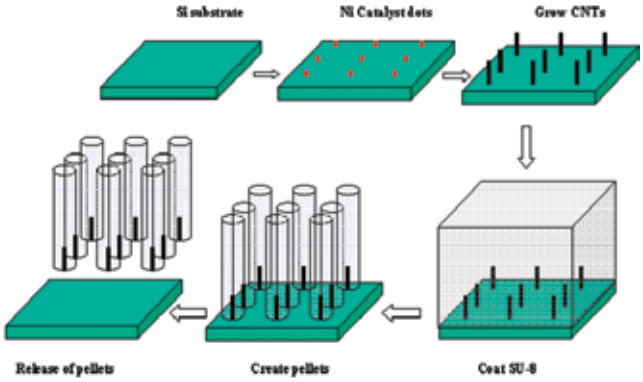

Figure 2: Additive process for nanopellets (single stranded CNT)

REFERENCES:

[1] El-Aguizy, T., S.-G. Kim, "Large-Scale Assembly of Carbon Nanotubes," *ASME Conference on Integrated Nanosystems: Design, Synthesis & Applications*, Pasadena, CA, September 2004.

[2] El-Aguizy, T., J.-H. Jeong, Y.B. Jeon, W.Z. Li, Z.F. Ren, S.-G. Kim, "Transplanting Carbon Nanotubes," *Applied Physics Letters*, vol. 85, no. 24, pp. 5995-5997, December 2004.

Combined Electron Transport with Resonant Raman Spectroscopy Characterization of Carbon Nanotubes

H. Farhat, J. Kong
Sponsorship: CMSE

We plan to study the electron transport in single-walled carbon nanotubes using the Raman spectroscopy technique as a complementary tool to characterize the nanotubes. The work will be carried out in two parts. First, we will perform electrical measurements, so the nanotube type can be identified as semiconducting or metallic. The lineshape of G-band mode with the nanotube type then can be correlated by taking the Raman spectra. The chirality of a nanotube will be identified with Raman spectroscopy and this identification will provide more information toward understanding the electron transport characteristic of the nanotube. Secondly, Raman spectra will be taken while running an electrical current through a nanotube. Stokes and anti-Stokes spectra from Raman will be compared to derive information on the electron-phonon scattering in the nanotubes, which will be important for nanotube interconnect applications.

Nanomagnets and Magnetic Random Access Memories

F.J. Castaño, W. Jung, D. Morecroft, H. Smith, C.A. Ross
Sponsorship: Cambridge-MIT Institute, NSF, Outgoing Marie Curie Fellowship

We are using a variety of lithography techniques (electron-beam lithography, interference lithography, zone-plate-array lithography, photo-lithography and X-ray lithography) to fabricate devices based on arrays of pillars, as well as bar-shaped and ring-shaped 'nanomagnets'. These small structures have thicknesses of a few nanometers and lateral dimensions typically smaller than 100 nm. Arrays of these elements are made with spatial periods of 100 nm and above, using evaporation/sputtering and liftoff, or by etching sputtered film. We are exploring the switching mechanisms of these particles, the thermal stability of their magnetization, and interparticle interactions, and we are assessing their suitability for various data-storage schemes. The behavior of individual particles can be measured using magnetic-force microscopy (MFM), while the collective behavior of arrays of particles can be measured using magnetometry. Data comparison shows how the behavior of one magnet is affected by its neighbors, and how much intrinsic variability there is between the particles as a result of microstructural differences. Small particles have near-uniform magnetization states, while larger ones develop more complex structures such as magnetization vortices or domain walls.

These nanomagnets have potential uses in magnetic random-access memories (MRAM), magnetic logic devices and other magneto-electronic applications. Current MRAM devices rely on bar-shaped multilayered nanomagnets, containing two magnetic layers separated by a thin layer of either a non-magnetic metal (Spin-valves) or an isolator (Magnetic tunneling junctions). The resistance of such elements depends on the relative orientation between the magnetization in the read-out (free) and storage (pinned) layers, allowing for a non-volatile bit of data to be stored in each element. As an alternative bit shape, MRAMs based on ring-shaped multilayered magnets have been recently proposed. We have used a multilevel lithography process to fabricate ring devices made from NiFe/Cu/Co pseudo-spin-valves (PSVs) with non-magnetic contact wires (Figure1). The rings display room temperature giant-magnetoresistance with distinct resistance levels, some of which occur at low applied fields. This feature makes PSV ring attractive for magnetoelectronic applications, such as memories or logic devices. We are currently pursuing a deeper understanding of the magnetization reversal in these multilayered rings using micromagnetic simulations and finite-element analysis.

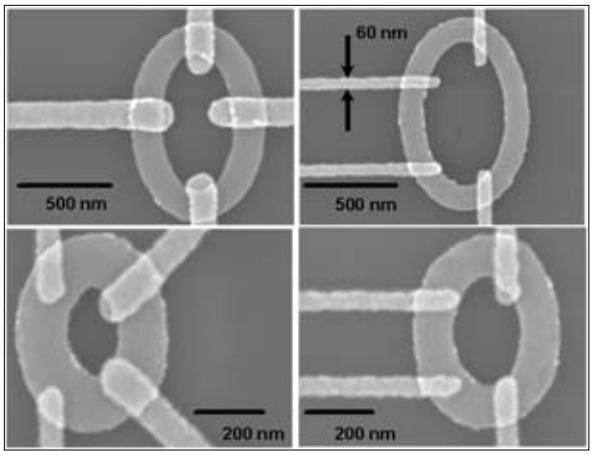

Figure 1: Scanning electron micrographs corresponding to multilayered elliptical-ring devices with different ring dimensions and contact wire configurations. The rings shown are fabricated from a NiFe (6 nm)/ Cu (4 nm)/ Co (4 nm)/ Au (3 nm) multilayer and the contact wires from a Ti (4 nm)/ Au (40 nm) bilayer.

Metal Nanoparticles for Electronic Applications

R. Barsotti, A. Jackson, G. DeVries, P. Djurianovic, F. Stellacci
Sponsorship: NSF, Hewlett-Packard

Ligand-coated AU (gold) nanoparticles have exciting applications in nanoelectronics due to their unique properties derived both from the small size of the metallic core (1-5 nm in diameter) and the ligand molecules that are attached to the nanoparticle by the thiol-gold bond. The ability to alter the composition of these ligands allows for control over the solubility and chemical reactivity of the nanoparticles. Thin films of ligand-coated metal nanoparticles offer the potential for tunable electron-transport properties. Organic ligands coating the nanoparticles act as insulating barriers through which electrons tunnel as they move between metallic cores. The length of the ligands, the degree of conjugation in the ligand shells, and the chemical functionality of the ligands affect the characteristics of that tunneling barrier, allowing a range in the film conductivity from insulating to semi-conducting to metallic. Ligand-coated gold nanoparticles also have shown single-electron charging effects and can be used in the fabrication of a single electron transistor (SET). Bottom-up directed assembly of gold nanoparticles is possible due to the large number of functional groups that can form the head group of a thiolated molecule attached to a gold nanoparticle. This assembly allows for a variety of co-valent or ionic bonding chemistries with molecules patterned on a substrate. An insulating gap is cut in conductive gold wires (fabricated with ebeam lithography) using a focused ion beam. The ends of the gold wires are then functionalized with dip pen nanolithography (DPN), patterning molecules with terminal carboxylic acid or alcohol functionalities. Nanoparticle assembly occurs selectively on the patterned regions. Preliminary results show a 100-times decrease in resistance after nanoparticle assembly. Improved resolution in gap formation and DPN will allow for the assembly of a single nanoparticle in the gap, which will serve as an SET whose electronic properties can be tuned by the choice of surrounding ligands.

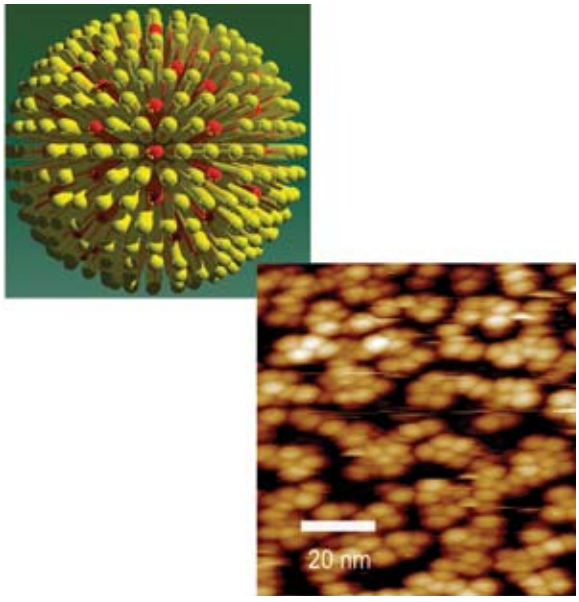

Figure 1: Schematic of ligand-coated gold nanoparticles; (upper left) scanning tunneling microscopy (STM) image of ligand-encapsulated gold nanoparticles showing hexagonal packing.

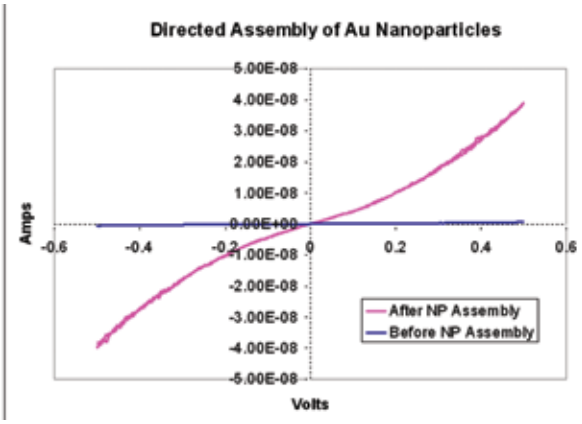

Figure 2: Current-Voltage (I-V) measurements show a 100-times increase in conductivity after the directed assembly of gold nanoparticles in a ~10 nm insulating gap.

Stress Evolution During Growth of Metal Thin Films

R. Moenig, J. Leib, A.R. Takahashi, C.V. Thompson
Sponsorship: NSF

Mechanical stress strongly influences the reliability and performance of highly miniaturized devices, therefore control of stresses in deposited structures and films is of general interest. Obtaining this control requires an understanding of the physical processes involved, as well as a quantitative knowledge of their contributions to total stress of a system. Our work focuses on the stresses that evolve during e-beam evaporative growth of high mobility metals on different amorphous substrates. Figure 1 shows a typical stress curve obtained by measuring substrate bending with a capacitive displacement sensor during film deposition. During early stages, islands nucleate and grow on a surface, causing a compressive stress thought to be related to the surface state of the growing islands [1,2]. As deposition continues, islands begin to coalesce and form a continuous layer. During this process, the stress becomes increasingly tensile while surface energy of the islands is transferred into grain boundary and elastic energy. After the film becomes continuous, the stress reverses and approaches a constant compressive value (again, thought to be related to the state of the film surface during deposition). One possible method of modifying the observed stress thickness behavior is to vary the size of islands using growth interrupts before island coalescence. Figure 2 shows the coarsening of islands during an interrupt which occurs on timescales corresponding to the mobility of an atom on the substrate. Upon resumption of growth the resulting larger islands coalesce at greater thicknesses and therefore lead the tensile peak in Figure 1 to shift towards higher thickness values. Flash depositions of Ta on the surface of deposited films allow for atomic force microscopy imaging of "frozen" films as shown in Figure 2 and provide a method for correlating the island size after a given length of interrupt with corresponding changes in measured stress curves. The ability to lock in a surface state at any stage of deposition or to interrupt growth also provides the means for exploring several other fundamental film stress generators, including the relaxation of stress due to coarsening of grains and islands and due to surface roughness.

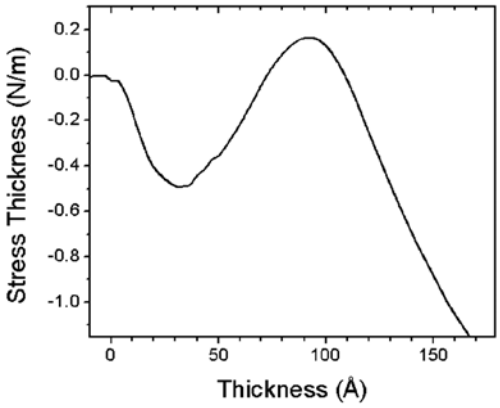

Figure 1: Stress measurement during deposition of Au on borosilicate glass. Deposition occurred at 1 Å/s, substrate was held at RT.

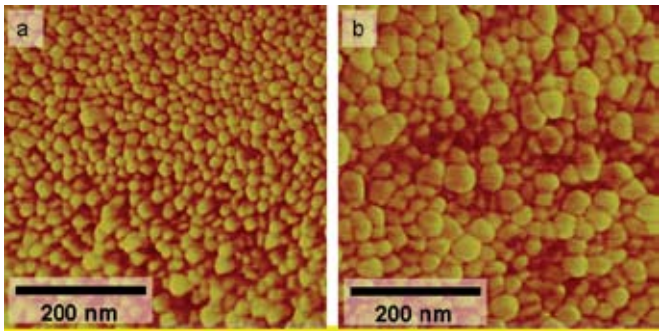

Figure 2: Atomic force microscope phase images of 40 Å Cu films deposited on SiO2. (a) Ta deposition immediately after Cu growth, mean particle diameter 15 nm. (b) Ta deposition 15 min after Cu growth, mean particle diameter 21 nm.

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Bonding and Boundary Formation Resulting from the Contact of Metallic Nanoclusters

A.R. Takahashi, R. Moenig, J. Leib, C.V. Thompson
Sponsorship: NSF

The properties of ultra-thin metallic films are heavily dependent on the transition from discontinuous islands to continuous films. Additionally, devices assembled from nano-crystallite building blocks are also beginning to show promise for implementing novel applications. In some applications, the nanoclusters must remain isolated from one another, while in other applications, selective electrical contact is required. This research project focuses on the bonding and boundary formation process when nanoclusters are placed in contact with one another. This process is analogous to island impingement during thin film formation. The high surface curvatures of the islands provide a very strong driving force for bonding. An increase in strain energy is compensated by the reduction in surface energy. The intrinsic tensile stress generated by this process is measurable and expected to affect the thin film device properties.

The boundary formation process is being investigated primarily through the use of computer models. These computer models incorporate semi-empirical inter-atomic potentials and molecular dynamics to evolve a system of clusters in time. Through these calculations, we find that the times required for nanometer sized islands to form boundaries can be on the order of nanoseconds (see Figure 1) and that the boundary areas are consistent with predictions from continuum theory. Based on these findings, we are also implementing a finite element model, which incorporates the orientation and contact angle dependencies seen in the atomistic calculations.

In connection with the computational studies, we are using transmission electron microscopy (TEM) to investigate the coalescence and sintering behavior of model systems generated from colloidal suspensions and from pre-coalescence metallic thin films (see Figure 2). Defect structures observed in the TEM will be directly compared to computationally generated defects.

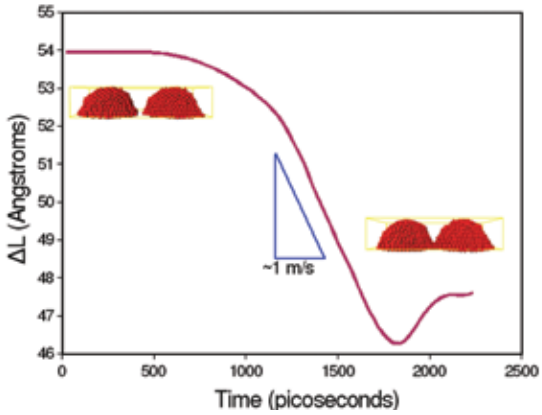

Figure 1: Distance between centers of mass evolution over time showing the completion of the boundary formation process in approximately 2 ns.

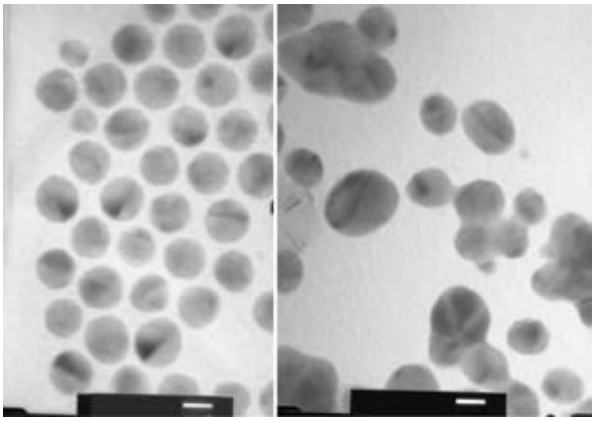

Figure 2: A nanoparticle array before (left) and after (right) heat treatment to induce particle sintering. The scalebars are 10 nm.

Templated Assembly by Selective Removal

S. Jung, F. Eid, C. Livermore
Sponsorship: NSF, 3M

In this project, an effective technique for site-selective, multicomponent assembly on the nano- and microscale has been developed. Creation of practical nanosystems using this technique is underway. This approach offers great promise for assembling arbitrary (not necessarily periodic) systems of different types of nanoscale components, such as electronics (memory, logic, interconnects, displays) and sensor systems.

The key elements of the approach are as follows. First, the topography of the substrate is modified to match the components' 3D shapes. Then, the substrate and components are coated with an adhesion promoter, such as a hydrophobic SAM, for adhesion in a water-based environment. The components and substrate are placed in a fluid environment for the assembly process then megahertz-frequency ultrasound is applied to the fluid bath. Components contact the substrate randomly and adhere wherever they land; however, components that are not in shape-matched sites are removed by fluid forces initiated by the high-frequency ultrasound. Components in shape-matched sites are selectively retained because their adhesive force is stronger than the removal forces. Figure 1 is an optical micrograph showing the successful assembly of 1.6 μm diameter microparticles into designated sites on the substrate. Figure 2 shows how measured assembly yield of microparticles into holes of slightly different sizes increases with the contact area between particles and substrate.

This approach to assembly is inherently selective. Since each component will adhere only in a shape- and size-matched site, geometrically distinct components will assemble only into their designated assembly sites. Therefore, the organizing information is allowed to be stored in the template initially, and components that may not be compatible with top-down manufacturing techniques can be added to the system later, with high positional precision. Work is in progress to demonstrate this approach in smaller- size scales and to create practical nanosystems using this technology.

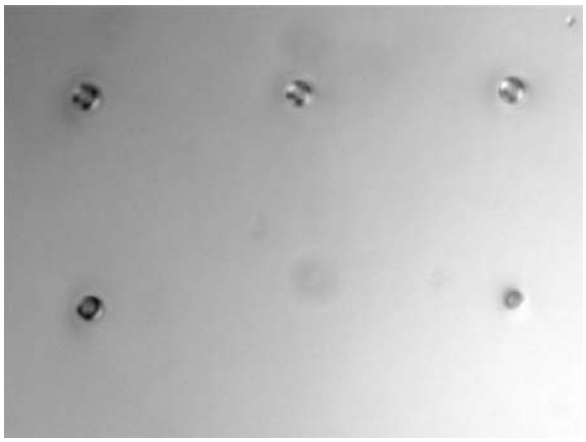

Figure 1: Optical micrograph showing four particle-filled holes and one empty hole.

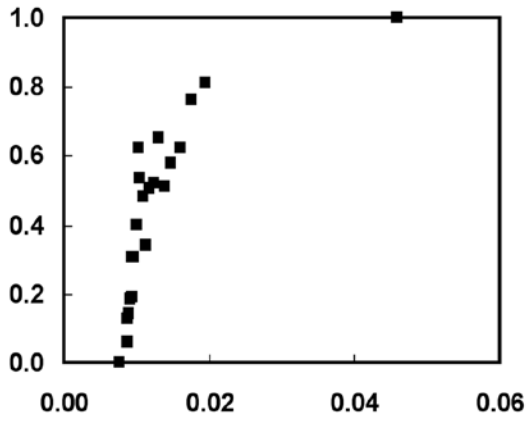

Figure 2: Plot of assembly yield (number of particle-filled holes/total number of holes) vs. contact area between particle and hole. Assembly yield increases from 0% to 100% as quality of the shape match improves.

Block Copolymer Lithography

F. Ilievski, G.J. Vancso, C.A. Ross, H. Smith, E.L. Thomas
Sponsorship: NSF, CMSE

Fabrication of large-area periodic nanoscale structures using self-organizing systems is of great interest because of the simplicity and low cost of the process. Block copolymers consist of polymer chains made from two chemically distinct polymer materials. The chains can self-assemble to form small-scale domains whose size and geometry depend on the molecular weights of the two types of polymer and their interaction [1]. The domains have a very uniform distribution of sizes and shapes. We have been using block copolymers as templates for the formation of structures such as magnetic particles, by selectively removing one type of domain and using the resulting template to pattern a nanostructured magnetic film. An example is shown in Figure 1, where perpendicularly magnetic CoCrPt dots have been made using ion milling to pattern a CoCrPt film. The dots maintain the out-of-plane magnetization of the film, and the out-of-plane coercivity of the array is increased tenfold as compared to the as-deposited film (Figure 2). Additionally, the magnetic switching volume of the array is approximately equal to the physical volume of one dot, suggesting that the dots are magnetically as well as physically decoupled and switch coherently. The patterning process has been successfully applied to the fabrication of magnetic dots from Co, $NiFe^2$ and multilayer CoFe/Cu/NiFe films. The arrays of Co and NiFe dots show strong magnetostatic interactions and exhibit collective switching of 2-6 dots [2]. The multilayer dots maintain the magnetoresistance present in the as-deposited multilayer film. Furthermore, the separate reversal of the two magnetic layers is visible in both patterned and unpatterned films [3]. Work is now concentrated on producing ordered arrays with perpendicular magnetization by templating the block copolymer using shallow grooves for storage media applications.

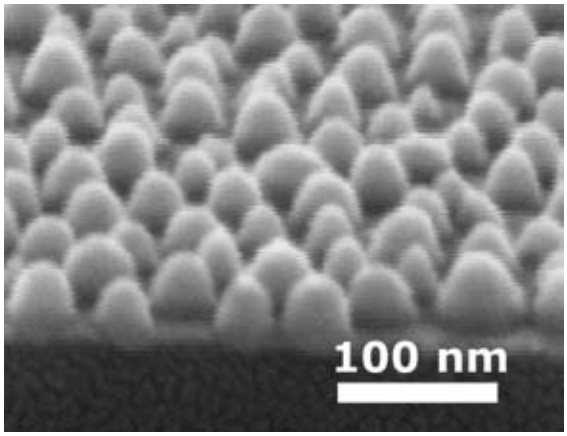

Figure 1: Tilted Scanning Electron Micrograph cross-section of a 15 nm thick CoCrPt dot array. The magnetic particles appear taller than the CoCrPt film thickness due to the presence of a W-etch mask capping each particle.

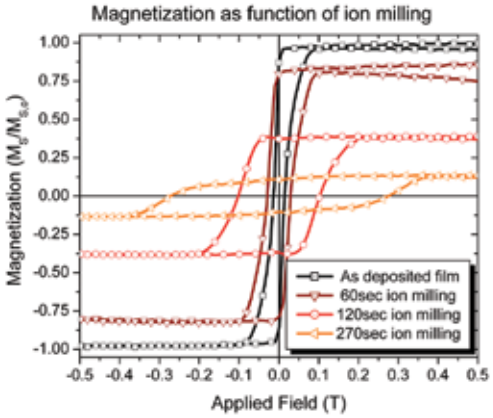

Figure 2: The out-of-plane magnetization curves for the sample shown in Figure 1 as a function of the ion-milling step. The moment has been normalized to the moment of the as-deposited film and it decreases monotonously as material is removed. The coercivity increases due to separation of the film in separate domains.

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[3] Ross, C.A., F.J. Castaño, E. Rodriguez, S. Haratani, B. Vögeli, H.I. Smith, "Size-Dependent Switching of Multilayer Magnetic Elements," *Journal of Applied Physics*, vol. 97, no. 5, pp. 053902: 1-6, 2005.

Proximity Effects in Self-organized Binary Particle-block Copolymer Blends

M.R. Bockstaller, E.L. Thomas
Sponsorship: ARO, Alexander von Humboldt Foundation

Depending on the surface chemistry of gold nanocrystals of equal metal core size, two morphological types of self-organized block copolymer–particle blends are observed: (1) the segregation of the nanocrystals to the interfacial areas; or (2) the preferential uniform distribution within one of the respective polymer domains. The confinement of the nanocrystals to the narrow interfacial regions of the microstructure in type one blends results in high local particle filling fractions and gives rise to electromagnetic coupling upon light irradiation, accompanied by a pronounced increase in absorbance.

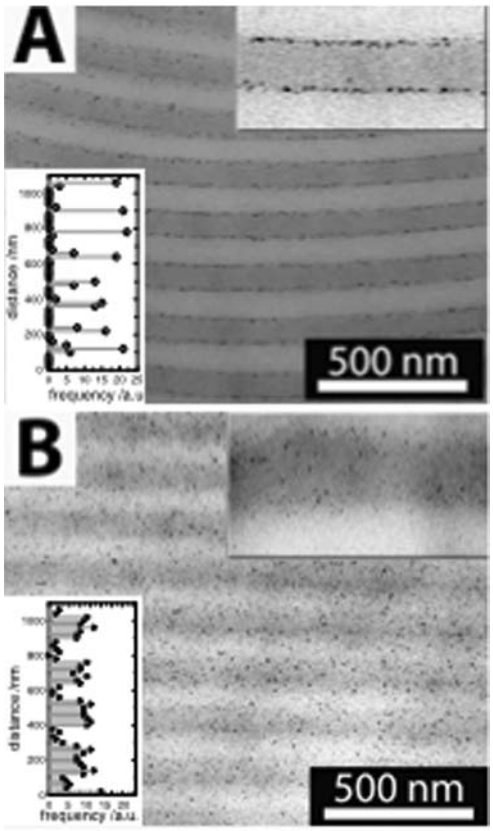

Figure 1: Bright field transmission electron micrographs of the unstained block copolymer/nanocrystal composite material after microsectioning *normal* to the layer direction demonstrating particle deposition at the IMDS (PS-PEP/AuSC$_{12}$H$_{25}$, type 1) in panel A, and homogeneous selective-layer morphology (PS-PEP/AuSPS, type *U*) in panel B, respectively. PEP domains appear as brighter regions in the micrograph. The volume-filling fraction of gold for both samples is $\phi \cong 0.01$. The lower insets in panel A and B depict the respective particle frequencies in 001 direction obtained by particle counting in equally sized area elements of 20 nm width. In panel B, a small amount of tilt of the IMDS with respect to the electron beam direction results in a somewhat smeared appearance of the PS-PEP interface.

Templated Self-Assembly of Nanoporous Alumina: A Wafer-level Methodology for Ordered and Aligned Nanostructures (Nano-wires, -rods, -dots and -tubes)

R. Krishnan, J. Oh, B. Hsu, C.V. Thompson
Sponsorship: MARCO IFC, SMA, NSF

Nano-sized materials are core building blocks for advanced functional devices, such as interconnects, logics, memories, sensors, and displays. Due to their size-sensitive electrical, optical, magnetic and chemical properties, fabricating these devices with controlled size and distribution on the device-applicable substrates is of importance. As a strategy, we are developing templated self-assembly methods that combine top-down (lithography) and bottom-up (self-assembly) approaches for fabricating and assembling metallic nano-wires, -rods, and -dots for new applications including nano-contacts for devices and interconnects for mixed-material and multifunctional micro- and nano-systems.

Anodic aluminum oxide (AAO) is a self-ordered, nano-structured material that is well-suited for use as a template in magnetic, electronic and opto-electronic devices. Under proper anodization conditions, aluminum oxidizes as a porous structure with aligned pores that have close-packed (hexagonal) order at short range and with pore sizes that can be varied from 4 nm-300 nm. The excellent mechanical and thermal stability of porous alumina makes it suitable both as physical masks for deposition of nanodot catalysts, as well as a supporting template for catalyzed growth of semiconductor nanowires and carbon nanotubes. While short-range pore ordering can be achieved during anodization, domains (<5 μm) of different repeat directions, which occur at longer ranges, limit further implementation of novel devices. We have developed a technique to obtain single-domain, porous alumina with sub-30 nm pore diameter and high aspect ratio (>50:1) on silicon substrates [1]. Anodization of aluminum films deposited on substrates with lithographically defined periodic topography lead to templated self-assembly of alumina pores that are perfectly ordered over large areas. The template controls the pore spacing and ordering symmetry, while the anodization conditions independently control the pore diameters to sub-lithographic length scales. Topographic templating of long-range order in AAO allows independent control of the pore size, spacing, and order symmetry in ranges not achievable without templating. Using the perfectly-ordered AAO templates, we have fabricated ordered metallic nanodots, nanorods, and nanotubes as well as well-aligned, multi-walled carbon nanotubes on silicon [2]. We are exploring the use of metal/CNT-filled alumina templates as electrical nano-breadboards using dip-pen nanolithography for applications in molecular electronics. These results demonstrate a wafer-scale approach to the control of the size, pitch, ordering symmetry, and position of nanomaterials in a rigid insulating scaffold.

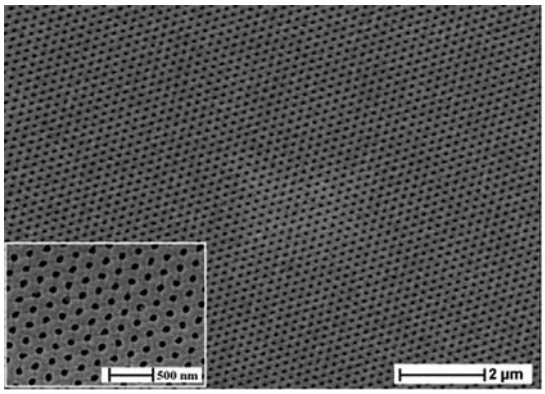

Figure 1: Scanning electron micrograph of perfectly ordered porous alumina with hexagonal symmetry on silicon over wafer-scale areas with pore diameter of 80 nm and pore spacing of 180 nm [1].

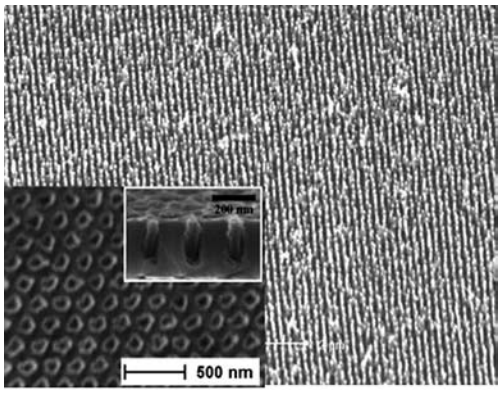

Figure 2: Scanning electron micrograph of ordered and well-aligned carbon nanotube arrays on silicon. Inset shows aligned CNT arrays in ordered porous alumina after ion-milling the surface [2].

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[2] Krishnan, R., H.Q. Nguyen, C.V. Thompson, W.K. Choi, Y.L. Foo, "Wafer-level Ordered Arrays of Aligned Carbon Nanotubes with Controlled Size and Spacing on Silicon," *Nanotechnology*, vol.16, no. 6, pp. 841-845, Jun. 2005.

Templated Self-Assembly of Metal Particles: Controlled Dewetting of Thin Films

A.L. Giermann, C.A. Ross, H. Smith, C.V. Thompson
Sponsorship: NSF

We are exploring templated self-assembly (TSA) as a tool for producing ordered arrays of metal nanodots over large areas via dewetting of thin solid films. Such arrays may be interesting in memory or plasmonic applications, and for use as catalysts for the growth of carbon nanotube or semiconductor nanowire arrays.

TSA is an attractive tool for patterning nano-scale materials. Use of physical templates to alter the surface environment can initiate self-forming and self-ordering processes in materials systems that have little or no inherent order. TSA is particularly attractive if we can obtain sub-lithographic assembly, or assembly of objects with sub-lithographic sizes.

As an initial demonstration of templated dewetting, we achieved one-to-one self-assembly of gold particles less than 100 nm in diameter and ordered over large areas [1]. We deposited gold films on di-periodic arrays of pits on oxidized silicon substrates, thereby modulating the curvature of the films and generating a well-ordered solid-state dewetting process. Compared to dewetting on flat substrates, the templates impose a significant decrease in average particle size, as well as ensure a narrow size and spatial distribution (Figure 1). This templating technique uniquely results in crystallographic ordering (i.e., graphoepitaxy) of the particles, imposing an in-plane texture, and changing the out-of-plane texture (Figure 2). Particles formed in topographic features are expected to be stable with respect to agglomeration during tube or wire growth.

Our current efforts include investigating the templating phenomena in other metals, particularly those that are known to catalyze nanotube and nanowire growth. We are also exploring methods for further scaling down the process and seeking topographies that will enable self-assembly on sub-lithographic length scales. In addition, we are developing phase field and numeric models of topographic dewetting in order to fully characterize the mechanism.

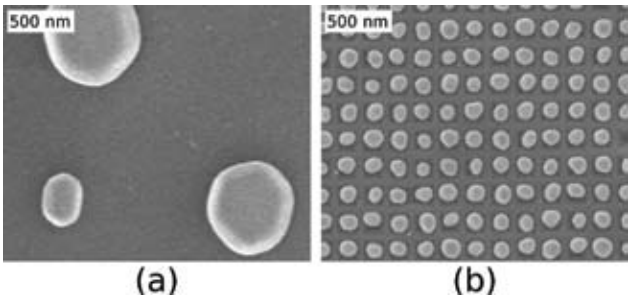

Figure 1: The effect of topography on particle morphology. The results of dewetting a 21 nm thick Au film on (a) a flat substrate and (b) a topographic substrate. Micrographs are displayed at the same magnification to emphasize the effect of topography on particle size. Scale bars are 500 nm in length.

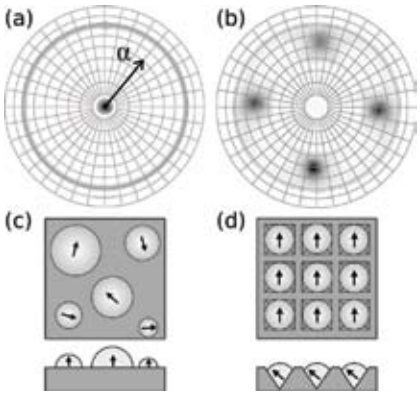

Figure 2: The effect of topography on particle orientation. (a) and (b) show Au (111) X-ray pole figures ($37.4^\circ < 2\theta < 38.6^\circ$), (a) for particles on a flat substrate and (b) for particles on a topographic substrate. (c) and (d) schematically illustrate the particle orientation on flat and topographic substrates, respectively. The arrows indicate the (111) projection.

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Templated Self-Assembly

J.Y. Cheng, H. Smith, A.M. Mayes, C.A. Ross
Sponsorship: NSF

Self-organized materials have been used to pattern large-area nanometer-scale periodic structures. However, typical self-assembled materials have only short-range ordered limiting their usefulness in nanodevices. With the guidance of lithographically defined templates, the templated self-assembly (TSA) method creates high-precision and high-density nanostructures by combining advantages of both self-assembled materials and lithography techniques. Templates made from electron-beam lithography have been employed to study TSA effect of block copolymers. Based on a simple free energy model describing the layering behavior of block copolymers in a one-dimensional topographical confinement (Figure 1a) and experimental data (Figure 1b), we are able to predict the design window (Figure 2a) for templates to make a particular arrangement of polymer domains (Figure 2b). The understanding of templated self-assembled block copolymers will facilitate the design of hybrid systems combining top-down and bottom-up processing, enabling new nanofabrication technologies based on these self-assembling materials.

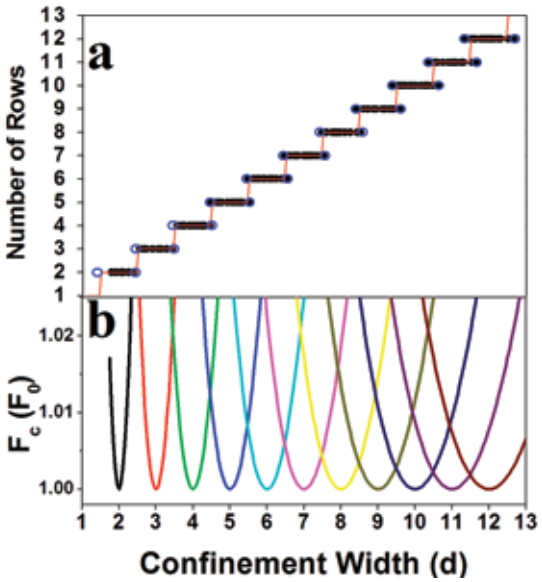

Figure 1: (a) The number of rows in the groove, *N*, vs. confinement width, *W*, showing the widths at which arrays with *N* rows are stable. (b) Energy vs. confinement width of block copolymer system. The confined block copolymer system, of given *W*, will ideally select the value of *N* with the lowest free energy. A transition in the number of rows from *N* to *N*+1 occurs when $W \sim (N+0.5)d$, in agreement with the experimental data of Figure 1(a).

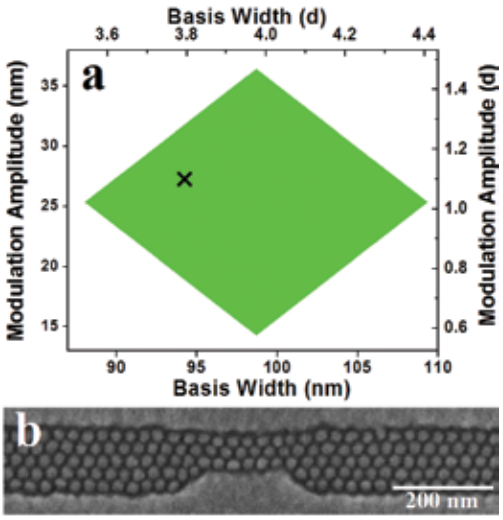

Figure 2: The creation of a specific block copolymer array geometry using a modulated template. (a) The modulation conditions that are expected to produce an array consisting of 5*p*-long 3-row arrays interspersed with 20*p*-long 5-row arrays. (b) Scanning electron micrograph of a section of an ordered array with 3 and 5 rows of domains, created using a template with dimensions indicated with a cross on part a.

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[2] Cheng, J.Y., C.A. Ross, E.L. Thomas, H.I. Smith, G.J. Vancso "Templated Self-Assembly of Block Copolymers: Effect of Substrate Topography", *Advanced Materials*, vol. 15, no. 19, pp. 1599-1602, October 2003.

Nanofabricated Diffraction Gratings

C.-H. Chang, R.C. Fleming, R.K. Heilmann, J. Montoya, M.L. Schattenburg, H. Smith
Sponsorship: NASA, XOPT, Inc., Plymouth Grating Laboratory

Diffraction gratings and other periodic patterns have long been important tools in research and manufacturing. Grating diffraction is due to the coherent superposition of waves—a phenomena with many useful properties and applications. Waves of many types can be diffracted, including visible and ultraviolet light, X-rays, electrons, and even atom beams. Periodic patterns have many useful applications in fields such as optics and spectroscopy, filtering of beams and media, metrology, high-power lasers, optical communications, semiconductor manufacturing, and nanotechnology research in nanophonics, nanomagnetics and nanobiology.

The performance of a grating is critically dependent on the geometry of individual grating lines. Lines can have rectangular, triangular, or other geometries, depending on the application. High efficiency requires control of the geometric parameters that define individual lines (e.g., width, height, smoothness, sidewall angle, etc.) in the nanometer or even sub-nanometer range. For some applications, control of grating period in the picometer to femtometer range is critical. Traditional methods of fabricating gratings, such as diamond tip ruling, electron and laser beam scanning, or holography, generally result in gratings that fall far below theoretical performance limits due to imperfections in the grating line geometry. The main goal of our research is to develop new technology for the rapid generation of general periodic patterns with control of geometry measured in the nanometer to sub-nanometer range in order to achieve near-theoretical performance and high yields.

The fabrication of gratings is generally accomplished in two main steps: (1) lithographic patterning into a photosensitive polymer resist; and (2) pattern transfer. A companion research program in this report entitled *Advanced Interference Lithography Technology* describes progress in advanced grating patterning technology. In this section, we report on research in pattern transfer technology. The development of a variety of grating geometries and materials is ongoing. Advanced gratings have been fabricated for ten NASA missions, and further advances are sought for future missions [1]. Figure 1 depicts a gold wire-grid transmission grating designed for filtering deep-UV radiation for atom telescopes, while Figure 2 depicts a nano-imprinted saw tooth reflection grating for X-ray spectroscopy.

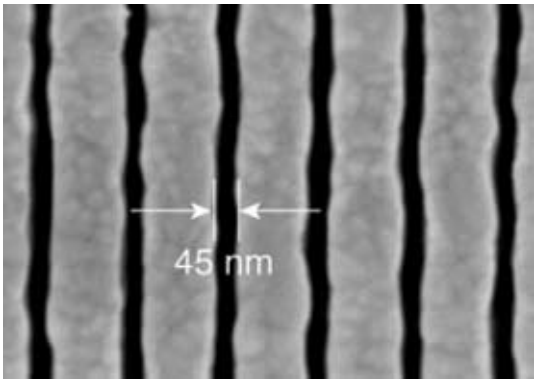

Figure 1: Scanning electron micrograph of a deep-UV blocking grating used in atom telescopes on the NASA *IMAGE* and *TWINS* missions. The grating blocks deep-UV radiation while passing energetic neutral atoms.

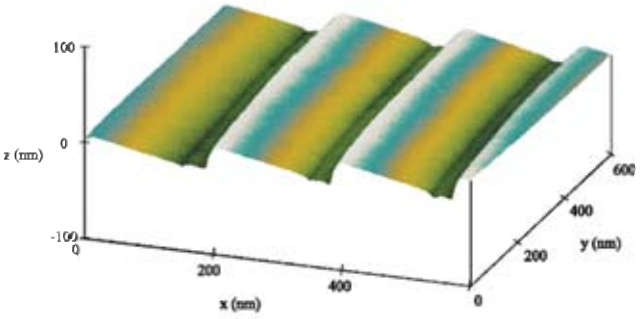

Figure 2: Atomic force microscope image of ~200 nm-period thermal-nano-imprint grating with 7° blaze angle developed for the NASA *Constellation X* mission. The grooved surfaces are extremely smooth with a root mean square (RMS) surface roughness of <0.2 nm.

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Advanced Interference Lithography Technology

C.-H. Chang, R.C. Fleming, R.K. Heilmann, J. Montoya, M.L. Schattenburg, Y. Zhao
Sponsorship: NASA, Plymouth Grating Laboratory

Traditional methods of fabricating gratings, such as diamond tip ruling, electron and laser beam scanning, or holography, are generally very slow and expensive, and they result in gratings with poor control of phase and period. More complex periodic patterns, such as gratings with chirped or curved lines, or 2D and 3D photonic patterns, are even more difficult to pattern. This research program seeks to develop advanced interference lithography tools and techniques to enable the rapid patterning of general periodic patterns with much lower cost and higher fidelity than current technology.

Interference lithography (IL) is a maskless lithography technique based on the interference of coherent beams. Interfering beams from an ultra-violet laser generate interference fringes that are captured in a photo-sensitive polymer resist. Much of the technology used in modern IL practice is borrowed from technology used to fabricate computer chips. Traditional IL methods result in gratings with large phase and period errors. We are developing new technology based on interference of phase-locked scanning beams, called scanning beam interference lithography (SBIL). The SBIL technique has been realized in a tool called the MIT Nanoruler (Figure 1), which recently won an R&D 100 award. By using the Nanoruler, large gratings can be patterned in a matter of minutes, with a grating phase error of only a few nanometers and a period error in the ppb range (Figure 2). Current research efforts seek to generalize the SBIL concept to pattern more complex periodic patterns, such as variable period (chirped) gratings, 2D metrology grids, and photonic patterns [1]. Important applications of large, high fidelity gratings include high-resolution X-ray spectrometers on NASA X-ray astronomy missions, high-energy laser pulse compression optics, and length metrology standards.

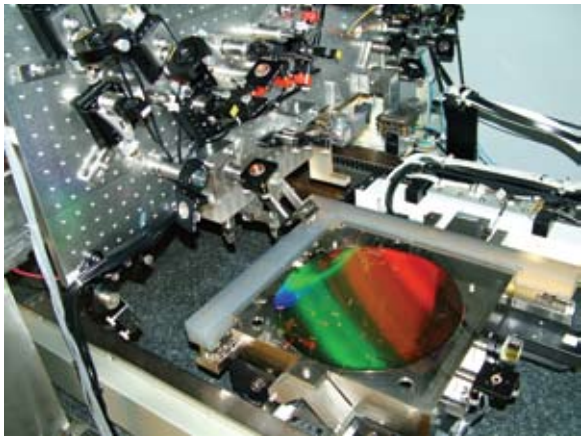

Figure 1: Photograph of the Nanoruler lithography and metrology system built by MIT students. This unique tool is the most precise grating, patterning, and metrology system in the world.

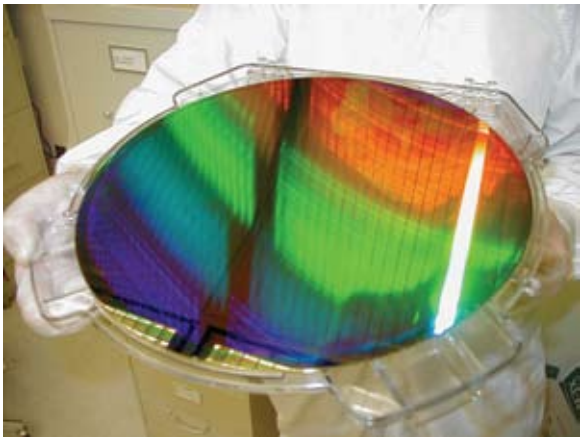

Figure 2: A 300 mm-diameter silicon wafer patterned with a 400 nm-period grating by the Nanoruler. The grating is diffracting light from the overhead fluorescent bulbs.

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[1] Pati, G.S., R.K. Heilmann, P.T. Konkola, C. Joo, C.G. Chen, E. Murphy and M.L. Schattenburg, "Generalized Scanning Beam Interference Lithography System for Patterning Gratings with Variable Period Progressions," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 20, no. 6, pp. 2617-2621, November 2002.

An Approach to Realizing Index Enhancement without Absorption for Immersion Lithography

V. Anant, M. Rådmark, T.C. Killian, K.K. Berggren
Sponsorship: AFOSR

In this work, we propose and evaluate a scheme for refractive index enhancement that achieves the following objectives: (1) an index of refraction greater than unity in an atomic vapor; and (2) optical amplification rather than absorption of the propagating probe beam. The scheme achieves the first of these objectives by tuning the probe beam close to an atomic resonance. The second is achieved by using an additional incoherent optical pump beam that inverts population between the two levels with which the near-resonant probe beam interacts. This scheme is simple and is shown to be tolerant to temperature-related broadening effects. However, it is susceptible to intensity-related broadening effects and background noise, due to amplified spontaneous emission. Such a scheme may find applications in the fields of immersion microscopy and immersion photolithography, where the high-index material could replace lower-index immersion liquids, as well as in applications such as all-optical switching, where an optically controlled refractive index is desirable.

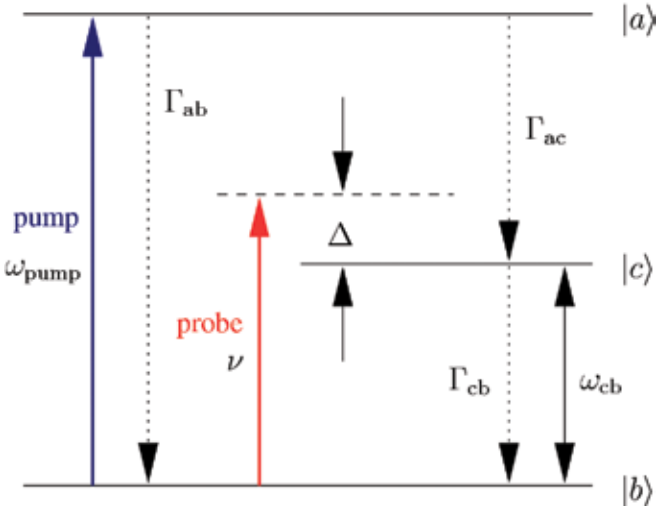

Figure 1: Energy level diagram showing incoherent decay rates and driving fields for the index-enhanced medium. A two-level system with ground state $|b\rangle$ and excited state $|c\rangle$ interacts with a coherent oscillating electromagnetic probe field at frequency ν detuned by Δ from the energy difference (ω_{cb}) between $|c\rangle$ and $|b\rangle$. An incoherent oscillating electromagnetic pump field at frequency $\omega_{pump} = \omega_{ab}$ promotes population from $|b\rangle$ to upper lying level $|a\rangle$. $|a\rangle$ is an upper level that decays at rate Γ_{ac} to level $|c\rangle$.

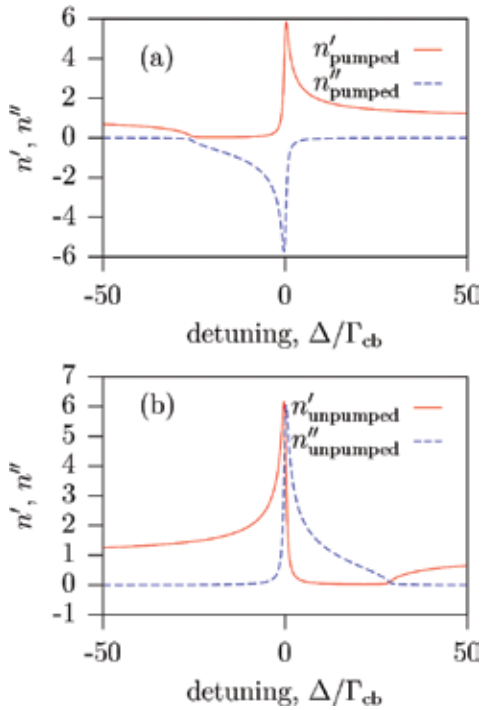

Figure 2: Plot of the refractive index n'' and absorption coefficient n'' as a function of Δ for the 4^1S_0 to 4^1P_1 transition in Ca: (a) pumped case, and (b) un-pumped case. For the pumped case, we see that $n'' < 0$, resulting in amplification (rather than absorption) of the probe laser. The maximum value of n' occurs slightly off resonance ($n_{max} \approx 6$ at $\Delta \approx 0.3\Gamma_{cb}$).

Sub-Resolution Lithography Using Quantum State Quenching

M. Rådmark, K.K. Berggren
Sponsorship: MIT

A way to improve spot size and resolution in optical projection lithography has been demonstrated in atomic beams using quantum state quenching near the node of an optical field [1]. Recently an extension of this technique has been proposed to directly control the exposure of photo-resist molecules [2]. The exposure sequence consists of three steps. In the first step, a diffraction-limited spot of the photo-resist would be excited. Immediately thereafter, a second incident pulse containing a node at its center would quench the outer parts of this spot, decreasing the spot size below the diffraction limit. In the third step, the remaining excited molecules would react to expose the resist.

To obtain the node in the quenching pulse, one could let the driving field of this pulse be a standing wave. A key property of this standing wave is that its maximum intensity should be much higher than the saturation intensity for de-excitation. With such a high intensity, the region where the intensity of the standing wave is too low to effectively quench excited molecules will be very narrow, and the remaining excited spot will be much smaller than the diffraction limit. The distribution of excited molecules, after quenching by the second pulse, will depend on the intensity of this pulse. Figure 1 shows calculations of point spread functions (PSFs) given by a quenching pulse with a standing wave of different intensities as driving field. With a wavelength of the standing wave on the order of 400 nm and a high maximum intensity (~ 10 W/μm^2), the PSF of excited molecules could be made very narrow and spot sizes on the order of tens of nanometers could possibly be achieved. Such a narrow PSF could be applied to achieve continued scaling of optical lithography into the sub-50-nm regime.

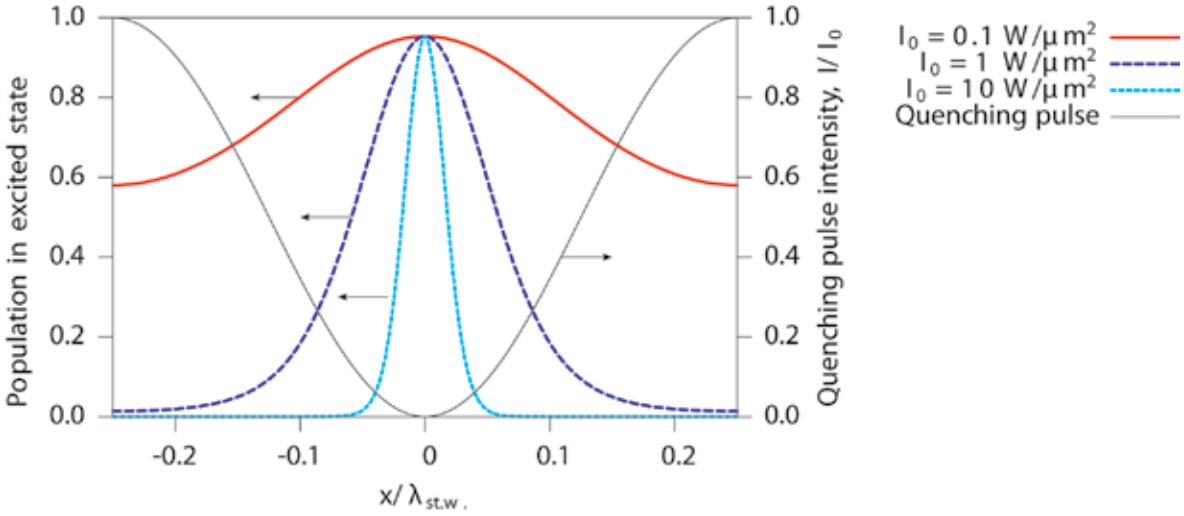

Figure 1: Distribution of molecules in the excited state, after the effects of a quenching pulse. The I_0 is the maximum intensity of the quenching pulse and $\lambda_{st.w}$ is the wavelength of the standing wave. The molecular cross-section for stimulated emission is assumed to be 10^{-16} cm^2. The higher the intensity of the quenching pulse, the more effectively it will quench excited molecules around the node, leading to a narrower PSF.

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Fabrication Methods for Adiabatic Quantum Computing Devices

B. Cord, W. Kaminsky, T.P. Orlando, K.K. Berggren
Sponsorship: Quantum Computing Graduate Research Fellowship, AFOSR

Adiabatic quantum computing devices (AQCs) have been implemented successfully in several types of systems, including ion traps, nuclear spins, and photon cavities. However, we find implementing AQCs in superconductive circuits offers several key advantages. Primarily, using standard techniques adapted from the semiconductor industry, we can fabricate very large numbers of superconductor-based qubits in CMOS-compatible materials, [1].

The stringent resolution and uniformity requirements for AQC devices present an interesting fabrication challenge. In order to perform certain AQC experiments, Josephson junctions with diameters of ~ 50 nm are useful. While previous quantum computing experiments at MIT used devices fabricated using optical projection lithography, sub-100 nm dimensions require alternate techniques, such as electron-beam lithography and suspended shadow-mask evaporation. Additionally, the uniformity of these nanoscale junctions must be high and the areas of the Josephson junctions within a single device must exhibit very low variation.

No readily-available lithographic technology meets these requirements, so research is being conducted on methods of defining arbitrary features as small as 50 nm with the precision required for adiabatic quantum computing. Current experiments have focused on improving the resolution and uniformity of the scanning electron-beam lithography (SEBL) system in the Nanostructures Laboratory, particularly in investigating the effects of different pattern geometries on the uniformity of very small features. Parallel work is also being done on a reliable, automated method of measuring the dimensions of very small structures for the purposes of determining uniformity, using scanning electron microscope (SEM) images and image-processing software.

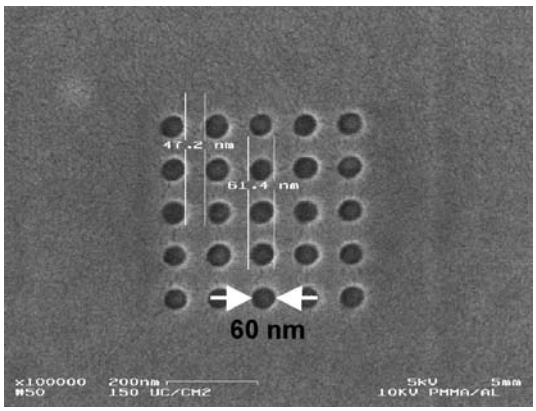

Figure 1: SEM of an array of 60nm diameter features in photoresist

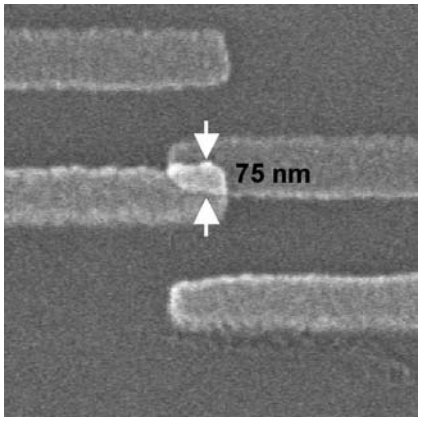

Figure 2: SEM of an 0.007μm^2 Al/AlO$_x$/Al Josephson junction fabricated via shadow-mask evaporation

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[1] Berggren, K.K., "Quantum Computing with Superconductors," *Proceedings of the IEEE,* vol. 92, no. 10, pp. 1630-1638, October 2004.

Superconducting Persistent Current Qubits in Niobium

Y. Yu, J. Habif, D. Nakada, J.C. Lee, D. Berns, B. Cord, T.P. Orlando, K.K. Berggren, L. Levitov, S. Lloyd,
in collaboration with S. Valenzuela, M. Tinkham (Harvard)
Sponsorship: DURINT, ARDA

Quantum Computation combines the exploration of new physical principles with the development of emerging technologies. We are beginning this research with the hope to accomplish the manipulation, control, and measurement of a single two-state quantum system, while maintaining quantum coherence between states. This process requires a coherent two-state system (a qubit) along with a method for control and measurement. Superconducting quantum computing could accomplish this in a manner that can be scaled to a large numbers of qubits. We are studying the properties of a two-state system made from a niobium (Nb) superconducting loop, which can be incorporated on-chip with other superconducting circuits for control and measurement. The devices we study are fabricated at MIT Lincoln Laboratory, which uses a Nb-trilayer process for the superconducting elements and optical projection photolithography to define circuit features. While our system is inherently scalable, we are challenged to demonstrate appreciable quantum coherence.

The particular device under study is made from a loop of Nb interrupted by three Josephson junctions (Figure 1a). The application of an external magnetic field to the loop induces a circulating current whose magnetic field either enhances (circulating current in the clockwise direction) or diminishes (counterclockwise) the applied magnetic field. When the applied field is near one-half of a flux quantum Φ_0, quantum superposition of both the clockwise and counterclockwise current states is possible. Thus the system behaves as a two-state system. The potential energy versus circulating current is a so-called double-well potential, with the two minima representing the two states of equal and opposite circulating current as shown in Figure 1c. The flux produced by the circulating currents can be measured by the sensitive flux meter provided by the dc SQUID.

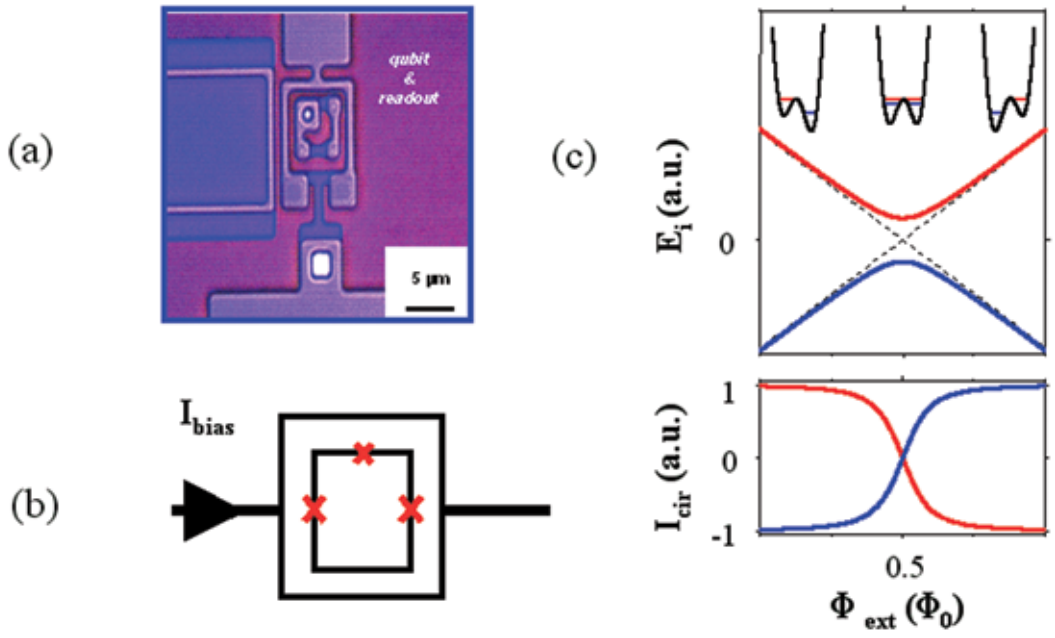

Figure 1: (a) Scanning electron microscope image of the persistent current qubit (inner loop) surrounded by the measuring dc SQUID. (b) a schematic of the persistent current qubit and measuring SQUID; the x's mark the Josephson junctions. (c) the energy levels for the ground state (dark line) and the first excited state of the qubit versus applied flux Φ_{ext}. The double well potentials are shown schematically in the above graph. The lower graph shows the circulating current in the qubit for both states as a function of applied flux (in units of flux quantum Φ_0).

Rapid Measurements in Superconducting Persistent Current Qubits

Y. Yu, W.D. Oliver, T.P. Orlando
Sponsorship: DURINT, ARDA

We installed a rapid measurement setup with a band width of about 1 GHz on a dilution refrigerator. By using an ultra-fast measurement scheme, we investigated the spectroscopy of superconducting Nb persistent current (PC) qubits. The time-resolved experiments showed that the energy relaxation time between the macroscopic quantum states is about 10 μs [1, 2]. We also demonstrated the superposition of macroscopic quantum states and Rabi oscillations between two macroscopic quantum states with microwave irradiations. The long-time macroscopic quantum coherence, together with the advanced fabrication technique, suggests the strong potential of realizing the quantum computing with Nb-based superconducting qubits.

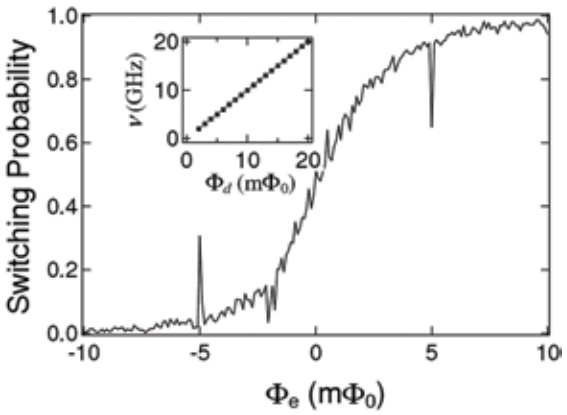

Figure 1: Switching probability vs. external magnetic field with 10 GHz microwave irradiation. The resonant peak and the dip are caused by photon induced transition between two macroscopic quantum states. Inset: microwave frequency vs. the distance between the peak and the dip (symbols). The solid line is the theoretical calculation using qubit parameters.

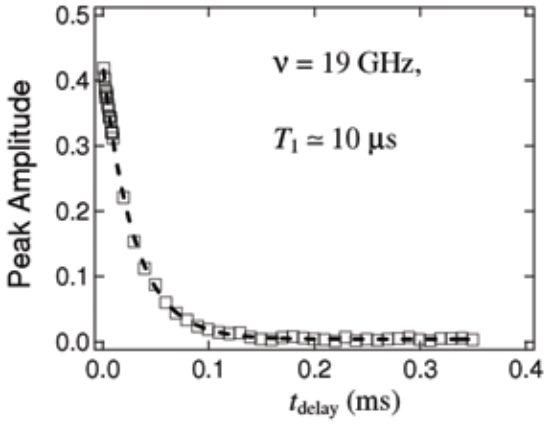

Figure 2: Normalized resonant peak amplitude as a function of readout delay time t_{delay}. The dashed line is the best fit to exponential decay with a time constant $T_1 = 10\ \mu s$. The experimental data show remarkable agreement with the theory prediction.

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[1] Yu, Y., D. Nakada, J. C. Lee, B. Singh, D. S. Crankshaw, T. P. Orlando, K. K. Berggren, W. D. Oliver, "Energy relaxation time between macroscopic quantum levels in a superconducting persistent-current qubit," *Physical Review Letters.*, vol. 92, no. 11, pp. 117904, March 2004.

[2] Yu, Y., W.D. Oliver, D. Nakada, J.C. Lee, K.K. Berggren, T.P .Orlando, "Energy relaxation times in a Nb persistent current qubit," submitted to *IEEE Transactions on AppliedSuperconductivity*, 2005.

Resonant Readout of a Persistent Current Qubit

J.C. Lee, W.D. Oliver, T.P. Orlando
Sponsorship: DURINT, ARDA, NSF

The two logical states of a persistent current (PC) qubit correspond to oppositely circulating currents in the qubit loop. The induced magnetic flux associated with the current either adds to or subtracts from the background flux. The state of the qubit can thus be detected by a DC superconducting quantum interference device (SQUID) magnetometer inductively coupled to the qubit. We have implemented a resonant technique that uses a SQUID as a flux-sensitive Josephson inductor for qubit readout. This approach keeps the readout SQUID biased at low currents along the supercurrent branch. Because the low bias reduces the level of decoherence on the qubit, it is more desirable for quantum computing applications. We also incorporated the SQUID inductor in a high-Q on-chip resonant circuit. This enabled us to distinguish the two flux states of a niobium PC qubit by observing a shift in the resonant frequency of the readout circuit. The nonlinear nature of the SQUID Josephson inductance, as well as its effect on the resonant spectra of the readout circuit, was also characterized.

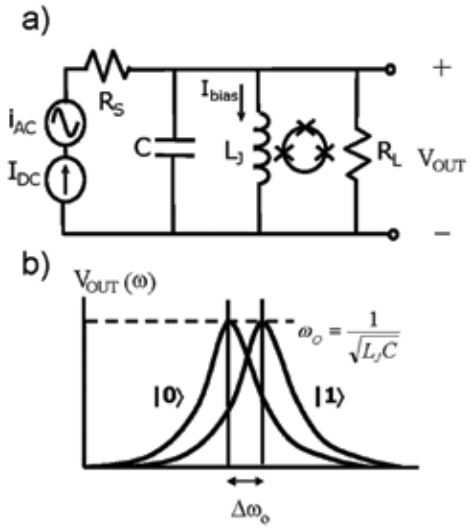

Figure 1: (a) The SQUID inductor is incorporated in a resonant readout circuit. It is inductively coupled to a PC qubit to detect its state. (b) A transition of the qubit state changes the Josephson inductance of the SQUID, and can be sensed as a shift in the resonant frequency of the readout circuit.

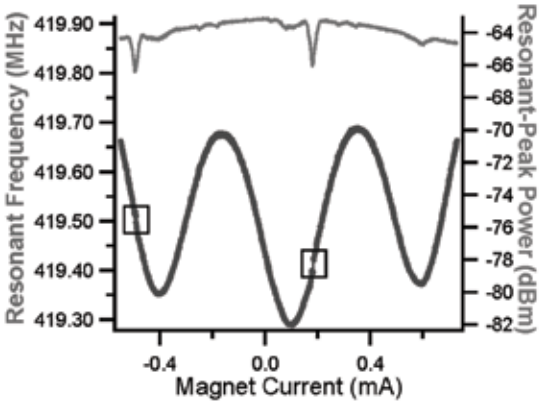

Figure 2: Experimental results at 300 mK: the lower plot (left axis) shows the modulation of the resonant frequency with external magnetic field. Qubit steps corresponding to transitions between opposite flux states were observed at every 1.3 periods of the SQUID lobe. The upper plot (right axis) shows the corresponding peak amplitude of the resonant spectrum. The dip in peak power coincides with the qubit step.

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Probing Decoherence with Electromagnetically Induced Transparency in Superconductive Quantum Circuits

K. Murali, W.Oliver, T.P. Orlando, in collaboration with Z. Dutton (Naval Research Laboratory)
Sponsorship: DURINT, ARDA

Superconductive quantum circuits (SQCs), comprising mesoscopic Josephson junctions, quantized flux, and/or charge states, are analogous to the quantized internal levels of an atom [1]. This SQC-atom analogy can be extended to the quantum optical effects associated with atoms, such as electromagnetically induced transparency (EIT) [2].

The three-level Λ-system for our S-EIT system (Figure1a) is a standard energy level structure utilized in atomic EIT. It comprises two meta-stable states $|1\rangle$ and $|2\rangle$, each of which may be coupled to a third excited state $|3\rangle$. In an atomic EIT scheme, a strong "control" laser couples the $|2\rangle \rightarrow |3\rangle$ transition, and a weak resonant "probe" laser couples the $|1\rangle \rightarrow |3\rangle$ transition. By itself, the probe laser light is readily absorbed by the atoms and thus the transmittance of the laser light through the atoms is very low. However, when the control and probe laser are applied simultaneously, destructive quantum interference between the atomic states involved in the two driven transitions causes the atom to become "transparent" to both the probe and control laser light [2,3,4]. Thus, the light passes through the atoms with virtually no absorption. In this work we propose to use EIT in SQCs to sensitively probe decoherence.

The SQC (Figure 1b) can be biased to result in an asymmetric double well potential as shown in Figure 2. The three states in the left well constitute the superconductive analog to the atomic Λ-system [5]. States $|1\rangle$ and $|2\rangle$ are "meta-stable" qubit states, with a tunneling and coherence time much longer than the excited "readout" state $|3\rangle$. State $|3\rangle$ has a strong inter-well transition when tuned on-resonance to state $|4\rangle$. Thus, a particle reaching state $|3\rangle$ will tend to tunnel quickly to state $|4\rangle$, causing the circulating current to switch to the other direction, an event that is detected with a SQUID. Knowing how long the SQC remains transparent (i.e., does not reach state $|3\rangle$) in the S-EIT experiment provides an estimate for decoherence time.

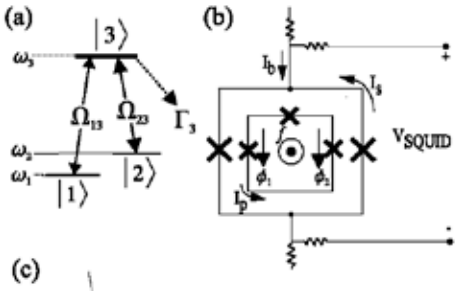

Figure 1: (a) Energy level diagram of a three-level Λ system. EIT can occur in atoms possessing two long-lived states |1>, |2>, each of which is coupled via resonant laser light fields to a radiatively decaying state |3>. (b) Circuit schematic of the persistent –current qubit and its readout SQUID.

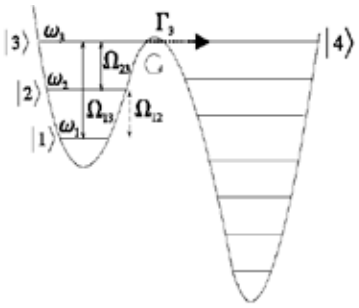

Figure 2: One-dimensional double-well potential and energy-level diagram for a three-level SQC.

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Type-II Quantum Computing Using Superconducting Qubits

D. Berns, W.M. Kaminsky, B. Cord, K.K. Berggren, W. Oliver, T.P. Orlando, in collaboration with
J. Yepez (Air Force Laboratories)
Sponsors: AFOSR, Fannie and John Hertz Foundation

Most algorithms designed for quantum computers will not best their classical counterparts until they are implemented with thousands of qubits. For example, the factoring of binary numbers with a quantum computer is estimated to be faster than a classical computer only when the length of the number is greater than about 500 digits [1]. In contrast, the Factorized Quantum Lattice-Gas Algorithm (FQLGA) [2] for fluid dynamics simulation, even when run on a quantum computer significantly smaller than the one just discussed, has significant advantages over its classical counterparts.

The FQLGA is the quantum version of classical lattice-gases (CLG)[3]. CLG are an extension of classical cellular automata with the goal of simulating fluid dynamics without reference to specific microscopic interactions. The binary nature of the CLG lattice variables is replaced for the FQLGA by the Hilbert space of a two-level quantum system. The results of this replacement are similar to that of the lattice-Boltzmann model, but with a couple of significant differences [4]. The first is the exponential decrease in required memory. The second is the ability to simulate arbitrarily small viscosities.

We have recently developed two implementations of the algorithm for the 1D diffusion equation using the PC qubit. The first consists of initializing the qubits while keeping them in their ground state, and then performing the collision by quickly changing their flux bias points and then performing a single $\pi/2$ pulse (Figure 1). This initialization technique could prove quite useful, since relaxation effects are avoided, but the way we have implemented the collision is not easily generalized to other collisions. A more general collision implementation was then developed by decomposing the unitary collision matrix into a sequence of single qubit rotations and coupled free evolution. The single qubit rotations then also serve to initialize the fluid's mass density.

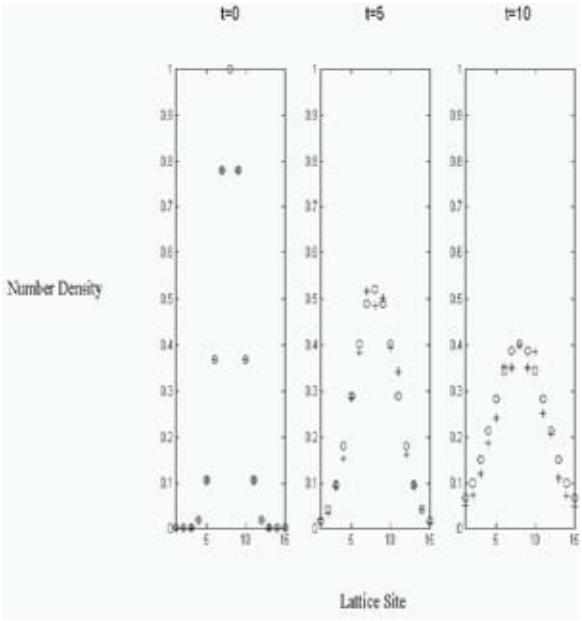

Figure 1: Simulation of the FQLGA for 1D diffusion is pictured(o) alongside simulation of the first proposed implementation(+). The expected diffusion of a gaussian is observed.

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Scalable Superconducting Architecture for Adiabatic Quantum Computation

W.M. Kaminsky, S. Lloyd, T.P. Orlando
Sponsorship: Fannie and John Hertz Foundation

Adiabatic quantum computation (AQC) is an approach to universal quantum computation in which the entire computation is performed in the ground state of a suitably chosen Hamiltonian [1]. As such, AQC offers intrinsic protection against dephasing and dissipation [2,3]. Moreover, AQC naturally suggests a novel quantum approach to the classically intractable constrained minimization problems of the complexity class NP. Namely, by exploiting the ability of coherent quantum systems to follow adiabatically the ground state of a slowly changing Hamiltonian, AQC promises to bypass automatically the many separated local minima occurring in difficult constrained minimization problems that are responsible for the inefficiency of classical minimization algorithms. To date, most research on AQC [4-8] has focused on determining the precise extent to which it could outperform classical minimization algorithms. The tantalizing possibility remains that---at least for all practical purposes---AQC offers at least a large polynomial, and often an exponential, speedup over classical algorithms. However, it may be the case that in the same way the efficiency of many practical classical algorithms for NP problems can only be established empirically, the efficiency of AQC on large instances of classically intractable problems can only be established by building a large-scale AQC experiment.

To make feasible such a large-scale AQC experiment, we have proposed a scalable architecture for AQC based on the superconducting persistent-current (PC) qubits [9,10] already under development here at MIT. As first proposed in [11], the architecture naturally incorporates the terms present in the PC qubit Hamiltonian by exploiting the isomorphism [12] between antiferromagnetic Ising models in applied magnetic fields and the canonical NP-complete graph theory problem Max Independent Set. Such a design notably removes any need for the interqubit couplings to be varied during the computation. Moreover, since Max Independent Set remains NP-complete even when restricted to planar graphs where each vertex is connected to no more than 3 others by edges, a scalable programmable architecture capable of posing any problem in the class NP may simply take the form of a 2D, hexagonal, square, or triangular lattice of qubits. Finally, the latest version of the architecture [13] permits interqubit couplings to be limited to nearest-neighbors and qubit measurements to be inefficient.

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6.152J students receive instruction on fabrication processes in EML.

EDUCATIONAL ACTIVITIES

TABLE OF CONTENTS

MIT Device Simulation Weblab: An Online Simulator For Microelectronics Education

A. Solis, J.A. del Alamo
Sponsorship: Microsoft Corporation

In the field of microelectronics, a device simulator is an important engineering tool with enormous educational value. With a simulator, a student can examine the characteristics of a microelectronic device described by a particular model. This ability makes it easier to develop intuition for the general behavior of that device and to

examine the impact of particular device parameters on device characteristics. In this project, we designed and implemented the MIT Device Simulation WebLab (WeblabSim), an online simulator for exploring the behavior of microelectronic devices [1]. WeblabSim makes a device simulator readily available to users on the web anywhere, at any time.

The WeblabSim system uses a three-tier design based on the iLab Shared Architecture (Figure 1). It consists of a client applet that lets users configure simulations, a laboratory server that runs them, and a generic service broker that mediates between the two through SOAP-based web services. We have implemented a graphical Java client applet, based on the client used by the MIT Microelectronics WebLab [2]. Our laboratory server has a distributed, modular design consisting of a data store, several worker servers that run simulations, and a master server that acts as a coordinator. On this system, we have successfully deployed WinSpice, a circuit simulator based on Berkeley Spice3F4.

Our initial experiences with WeblabSim indicate that it is feature-complete, reliable, and efficient. At this point, it is ready for beta deployment in a classroom setting, which we hope to carry out in the Fall of 2005.

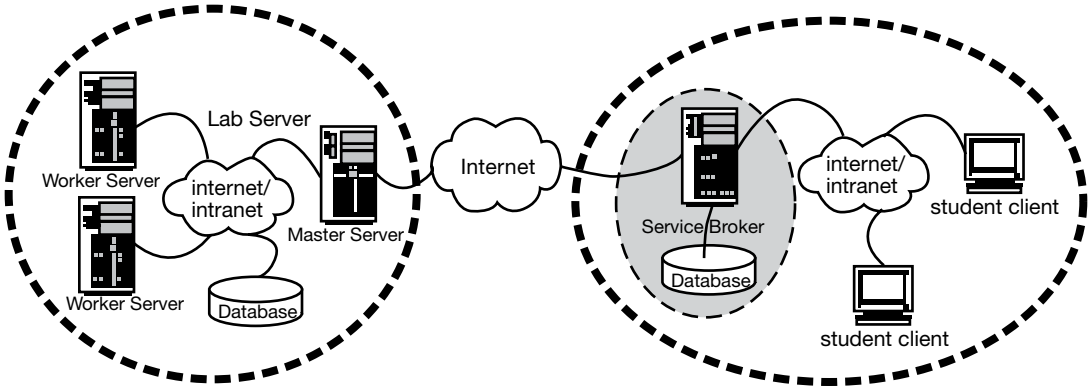

Figure 1: Topology of the MIT Device Simulation WebLab.

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The Microelectronics WebLab 6.0: An Implementation Using Web Services and the iLab Shared Architecture

J. Hardison, D. Zych, J.A. del Alamo, V.J. Harward, S.R. Lerman, S.M. Wang, K. Yehia, C. Varadharajan
Sponsorship: Microsoft Corporation

A new version of the MIT Microelectronics WebLab, an online semiconductor characterization laboratory, has recently been deployed. While WebLab is primarily of interest in microelectronics education, it also represents a testbed for new pedagogical and technological concepts associated with online laboratories.

WebLab 6.0, our latest release, is constructed around the newly developed iLab Shared Architecture – a three-tier framework designed at MIT to expedite the development and simplify the management of online laboratories [1]. The iLab Shared Architecture introduces a piece of middleware (termed the "Service Broker") between the Client application and the Lab Server. This Service Broker uses Web Services to provide functionality, such as user authentication and data storage, that is generic and common to all labs as well as to facilitate lab-specific communication between a given Client – Lab Server pair. WebLab 6.0 is the first lab deployed using this architecture [2].

The WebLab 6.0 Client is implemented using Java technology. It features a more polished User Interface and has been designed to be more modular and extensible than previous versions. The WebLab 6.0 Lab Server was completely redesigned as a highly modular, data-driven web application that is an improvement both in terms of performance and reliability. Additionally, the basic design of the Lab Server, as well as certain implemented components, can be reused to develop new online labs.

WebLab 6.0 was deployed and successfully tested during the Spring 2004 semester in an undergraduate microelectronics course at MIT involving over 100 students. Since then, several undergraduate and graduate courses, both at MIT and other institutions, have made use of WebLab 6.0 for lab assignments. Additionally, the WebLab 6.0 source has been released as an exemplar as it is the first online laboratory implemented using the iLab Shared Architecture [3]. WebLab 6.0 can be accessed at http://openilabs.mit.edu.

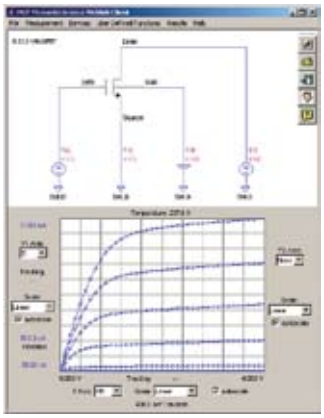

Figure 1: The Microelectronics WebLab 6.0 Client Interface.

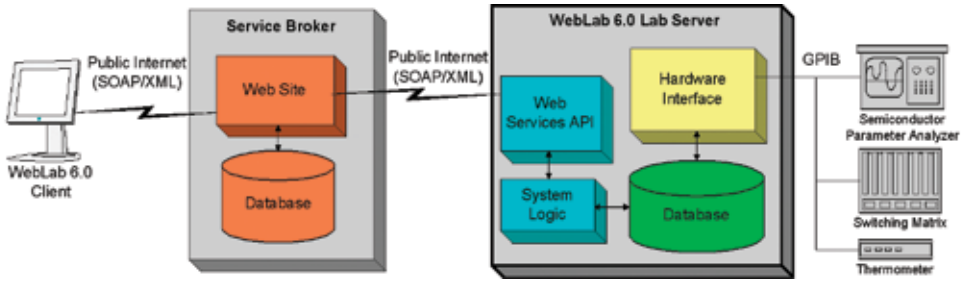

Figure 2: Schematic diagram of the Microelectronics WebLab 6.0 as implemented using the iLab Shared Architecture. The Service Broker performs generic lab functionality.

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Realizing the Potential of Online Laboratories in Developing Countries

J.A. del Alamo
Sponsorship: Carnegie Corporation of New York

We are about to launch an educational outreach program to realize the potential of online laboratories (iLabs) in Sub-Sahara Africa. iLabs constitute a new educational resource that allows students to carry out real experiments through the Internet. iLabs offer the potential of enriching science and engineering education around the world by bringing educationally meaningful laboratory experiences to students wherever an Internet connection is available. This "universality" of iLabs is seriously challenged in locations where access to the global Internet is limited by narrow bandwidths and high connection costs, or where students have restricted access to computers. Such conditions are pervasive in the developing world and are particularly dire in sub-Sahara Africa.

Through our new program, we will create an educational partnership among Makerere University (Kampala, Uganda), University of Dar Es Salaam (Dar es Salaam, Tanzania), Obafemi Awolowo University (Ile-Ife, Nigeria), and MIT to identify a scalable model to exploit the potential of iLabs in Sub-Sahara Africa. Our program will contain three main components: *teaching*, *lab dissemination*, and *student/staff exchanges*. Our *teaching* module aims to insert and utilize MIT's existing iLabs in the curriculum of partner institutions through the direct collaboration of the educators involved. We will share educational content, adapt manuals and tutorial materials, and develop new content and materials in a collaborative manner. Through our *lab dissemination* module, MIT will assist the partner institutions in the development of new iLabs in Africa that are uniquely designed to address local curricular needs and constraints. These iLabs will be constructed using MIT's iLab Shared Architecture (Figure 1) and will be shared among all partners. The *student/staff exchange* component will bring African graduate students and staff to MIT to be part of the group designing and implementing iLab technology and new educational content. It will also send MIT undergraduate students to the three partner universities in Africa to strengthen iLab-related efforts.

For more information, go to:
http://web.mit.edu/newsoffice/2005/africa.html

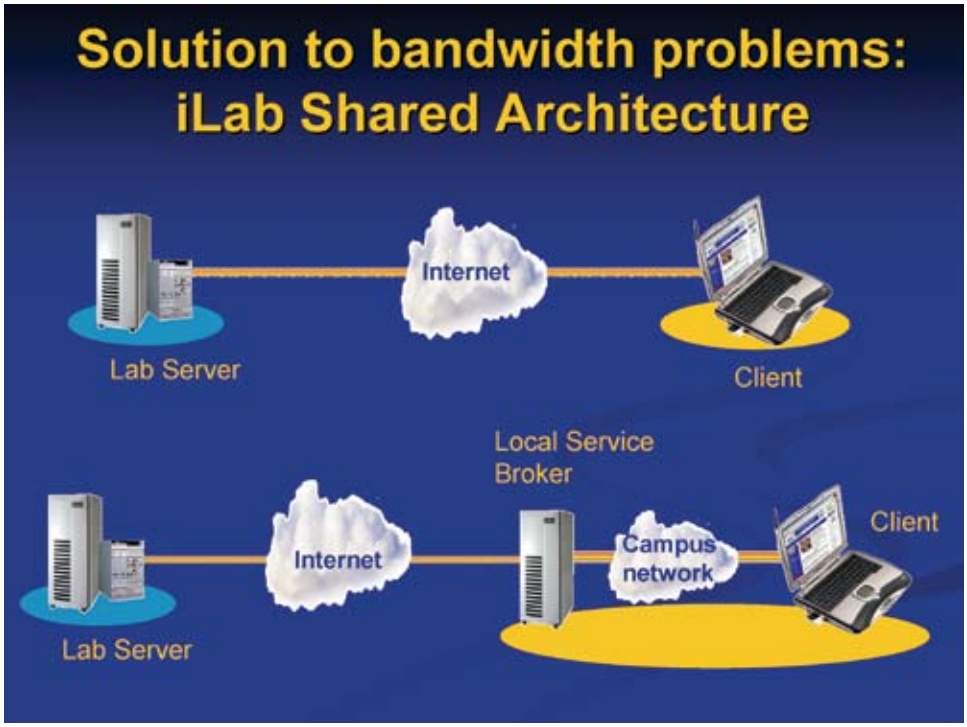


Figure 1: The MIT iLab Shared Architecture for implementing online laboratories helps alleviate the dearth of bandwidth in developing countries by placing a Service Broker in the intranet of the client campus.

A Microfluidics Teaching Laboratory

A.J. Aranyosi, A. Siddiqui, N.I Reyes-Gonzalez, E.J Lim, S. Desai, D.M. Freeman
Sponsorship: VaNTH-ERC, MIT SoE

Microfluidics holds promise for revolutionizing the design of systems for chemical and biological analysis. To introduce students to this important topic, we have developed a teaching laboratory that provides hands-on experience with microfluidic devices. Chambers are built, using soft lithography techniques, and mounted on glass to allow microscopic observation. Figure 1 illustrates a laminar flow chamber in which two fluids mix by diffusion. Students characterize the diffusion constant of a dye by measuring both spatial gradients in brightness across the channel at several locations and the velocity of the fluid along the channel. Measurements were made using custom software (Figure 2) that enabled both qualitative and quantitative analysis of microscope images.

The laboratory has been used successfully in two MIT courses. In 6.021J (Quantitative Physiology: Cells and Tissues), student teams propose and carry out a project to investigate a particular aspect of diffusion, such as determining if the diffusion constant varies with dye concentration. They present their results as a technical paper, which is critiqued by staff, writing experts, and fellow students. This process gives them an introduction to microfluidics, experience with technical writing, a better understanding of the course material, and a keen sense of the challenge of making experimental measurements. In 6.152J (Micro/Nano Processing Technology), students design and fabricate their own laminar flow chambers. They use the laboratory system to characterize these chambers by determining the diffusion constant of a dye. These measurements provide valuable feedback to help students improve their design process. In addition to these courses, the laboratory is scheduled for use in several other courses at MIT and Yale University. By adopting the laboratory, these courses are helping to train a new generation of students to have both conceptual knowledge and practical experience with microfluidics systems.

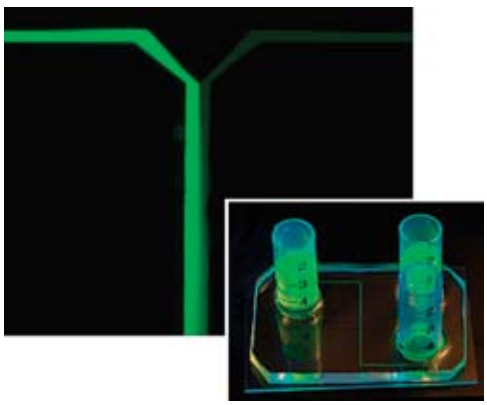


Figure 1: (Lower right) A laminar flow chamber. Fluids flow from the top two reservoirs combine and mix by diffusion as they flow along the center channel. (Upper left) Magnified view showing diffusion where the two fluids meet.

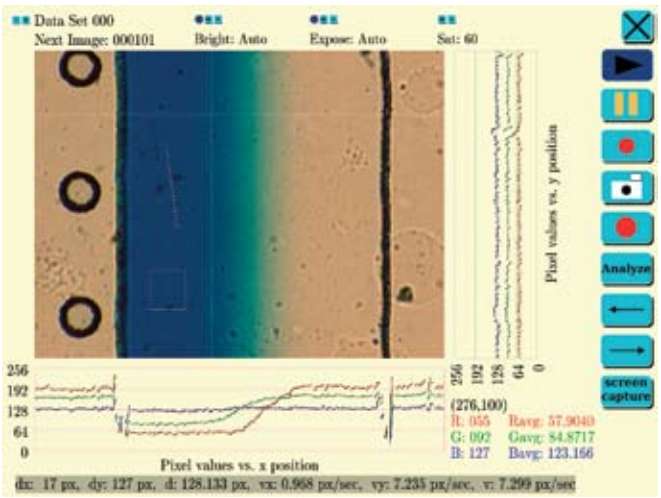


Figure 2: The software interface for the lab. The central image shows the microfluidic channel, with two fluids mixing by diffusion. The plots below and to the right of the image allow quantitative measurements to be made from the images.

Microfabrication Project Laboratory (6.151)

Technical Instructor, L. Wang

This laboratory course is offered in the spring semester for students that have already completed 6.152J. The course is designed to teach experimental microfabrication process design. The students of this subject are given a broad process goal, namely to build a device, and they are challenged to design and develop a process sequence. Typically, the entire class (4-6 students) works on one device, and they partition the integrated process into a set of unit process sequences. Work proceeds first, on the development of the unit processes, and then, on the integrated process. In recent years, the students have succeeded in microfabricating micromachined contactors for integrated circuit testing, flexible electrode arrays for retinal implants, and microcantilevers for AFM applications.

Micro/Nano Processing Technology (3.155J/6.152J)

Technical Instructor, L. Wang

This combination laboratory and lecture course is offered and taught jointly by the Department of Electrical Engineering and Computer Science and the Materials Science and Engineering Department. The course includes weekly lectures on all aspects of micro/nano processing technology with design problems to teach process design. Additionally, the course includes weekly laboratory sessions conducted in the MTL. During these sessions, each student fabricates a wafer of poly-silicon gate MOS devices, silicon nitride nano-mechanical devices, and a plastic microfluidic mixer. All the devices and structures are tested and laboratory reports correlating the test results with theoretical expectations culminates the education experience. The course is offered every semester, and a laboratory-only version of the course is offered 3-4 times/year.

Stacks of silicon wafers wait for the next step in TRL.

MTL RESEARCH CENTERS

MIT Center for Integrated Circuits and Systems (CICS)

Prof. Hae-Seung Lee, Director

The MIT Center for Integrated Circuits and Systems (CICS) is a form of an industrial consortium created to promote new research initiatives in circuits and systems design, as well as to promote tighter technical relation between MIT's research and relevant industry. Seven faculty members, Hae-Seung Lee as Director, Anantha Candrakasan, Joel Dawson, David Perreault, Michael Perrott, Charles G. Sodini, and Vladimir Stojanovic participate in the Center for Integrated Circuits and Systems. We are investigating a wide range of circuits and systems related to wireless and wireline communication, digital systems, microsensor/actuator networks, imaging systems, digital and analog signal processing, power electronics, and many other systems.

We strongly believe in the synergistic relation between the industry and academia, especially in practical research areas of the integrated circuits and systems. We are convinced that the Center for Integrated Circuits and Systems is the conduit for such synergy. The Center currently has twelve member companies. The Center includes all research projects that the three participating faculty members conduct regardless of the sources of funding. There are two different forms of technical interaction between the member companies and the Center. The broad interaction occurs through research reviews held twice a year open to member companies. These are technical reviews where technical representatives from member companies can critique the projects. In each full day review, we present as many projects as possible. The more intimate interaction happens at a more personal level with graduate students who are working on projects of member company's particular interest. The member company may invite them to give presentations at their site.

At biannual research reviews we have received valuable technical feedback as well as suggestions for future research. There has been close interaction between member companies and the Center personnel through company visits, summer employments, and personal interactions. We believe such an interaction has given very positive results for both MIT and member companies. We are hoping to continue to expand the Center in the future.

Intelligent Transportation Research Center (ITRC)

Dr. Ichiro Masaki, Director

Transportation is an important infrastructure for our society. It is time to propose a new transportation scheme for resolving the increasing transportation problems. In responding to social needs, MIT's Microsystems Technology Laboratories established the Intelligent Transportation Research Center (ITRC) in September 1998 as a contact point of industry, government, and academia for ITS research and development.

ITRC focuses on the key Intelligent Transportation Systems (ITS) technologies, including an integrated network of transportation information, automatic crash & incident detection, notification and response, advanced crash avoidance technology, advanced transportation monitoring and management, etc., in order to improve the safety, security, efficiency, mobile access, and environment. There are two emphasis for research conduced in the center:

- The integration of component technology research and system design research.
- The integration of technical possibilities and social needs.

ITRC proposes the incremental conversion and development process from current to near and far future systems and develops enabling key components in collaboration with the government, industries, and other institutions. Other necessary steps are the integration of technical, social, economical, and political aspects. The integration of the Intelligent Transportation Systems in different countries is also essential. The integration of vehicles, roads, and other modes of transportation, such as railways and public buses, are all imperative.

These integrations are fulfilled with the cooperation of researchers in various fields, including the Microsystems Technology Laboratory (MTL), the Research Laboratory of Electronics (RLE), the Artificial Intelligence Laboratory (AI), the Center for Transportation Studies (CTS), the Age Laboratory, the Department of Electrical Engineering and Computer Science, the Department of Civil and Environmental Engineering, the Department of Aeronautics and Astronautics, and the Sloan School of Management. The research center has 8 MIT faculty and several visiting professors and scientists. The director of the center is Dr. Ichiro Masaki.

MEMS@MIT

Prof. Martin A. Schmidt, Director

The MEMS @ MIT Center is a newly formed center intended to serve as a means to unite the wide-ranging campus activities in MEMS with forward-looking industrial organizations. The MEMS research efforts on campus span a wide range of activities with three overarching themes: i) Biological, Chemical and Medical MEMS, ii) Power MEMS, and iii) Enabling Technologies. In addition, we maintain an industrial consortium designed to connect member companies to the MEMS-related activities on campus. Overall, MEMS @ MIT includes approximately two dozen faculty and more than 100 students.

The research program in Biological, Chemical and Medical MEMS includes work on manipulation and processing of biologically-relevant materials of varying size scales from tissue engineering scaffolds and cell manipulation, to devices for separation and sorting of DNA and proteins. Additionally, we are working on various sensing platforms for detection of biomolecules. A wide range of microfluidic devices are explored in this research area. Microchemical systems for synthesis and characterization are an area of substantial research. This includes work in developing the core technology for fabrication and packaging of these reactors. The program in Power MEMS spans a wide range of targeted power outputs. Energy scavenging by vibration harvesting is studied for low power distributed systems. Various approaches to fuel burning power generation are studied from thermophotovoltaics to fuel cells and microturbine engines. Enabling Technologies explored in the Center include work on MEMS processes and process modeling. Materials characterization is a critical area of focus. CAD tools for modeling MEMS devices, as well as novel metrology methods form a core competency of the Center. Micro and nano-mechanical devices such as switches, actuators, and self-assembled devices round out the research portfolio.

MIT Center for Integrated Photonic Systems

Prof. Rajeev J. Ram, Director

The goals of the Center for Integrated Photonic Systems are:

1. To provide leadership and direction for research and development in photonics.

The core activity of CIPS is the development of a long-range vision for research and the development of integrated photonic devices & systems. CIPS will host forums and facilitate working groups with industrial consortium members to identify and discuss technology and roadmapping issues:

- technology directions
- potential disruptive technologies
- technical barriers (gaps)
- actions needed to enable future-generation systems, and
- manufacturing and market issues that drive timing of technology deployment.

As an academic institution we can work openly with a variety of different organizations in developing and gathering input for our models. Whether it is performance data for new devices 'in the lab,' yield data for existing manufacturing processes, planning documents, or first-hand observations of the corporate decision making process, CIPS researchers benefit greatly from the unique relationship between MIT and industry. The level of detail and intellectual rigor of the models being developed here is complemented by the high quality of data available to us. CIPS researchers are developing models of optical and electronic devices, the packages they are wrapped inside, the manufacturing processes that assemble them, the standards that define them, the market that buys them, and the policy processes which influence their deployment.

2. To foster an Institute wide community of researchers in the field of integrated photonics & systems.

The Departments of Electrical Engineering and Computer Science, Materials Science and Engineering, Mechanical Engineering and Economics are consistently ranked as the top graduate programs in the country. Likewise, the Sloan School of Management has consistently ranked first in the nation in the areas of information technology, operations research, and supply chain management. CIPS leverages MIT's strengths, by unifying the photonics researchers in these departments and laboratories to focus on technology developments in photonics.

The combined volume of research funds in the photonics area at MIT exceeds $20 million dollars annually.

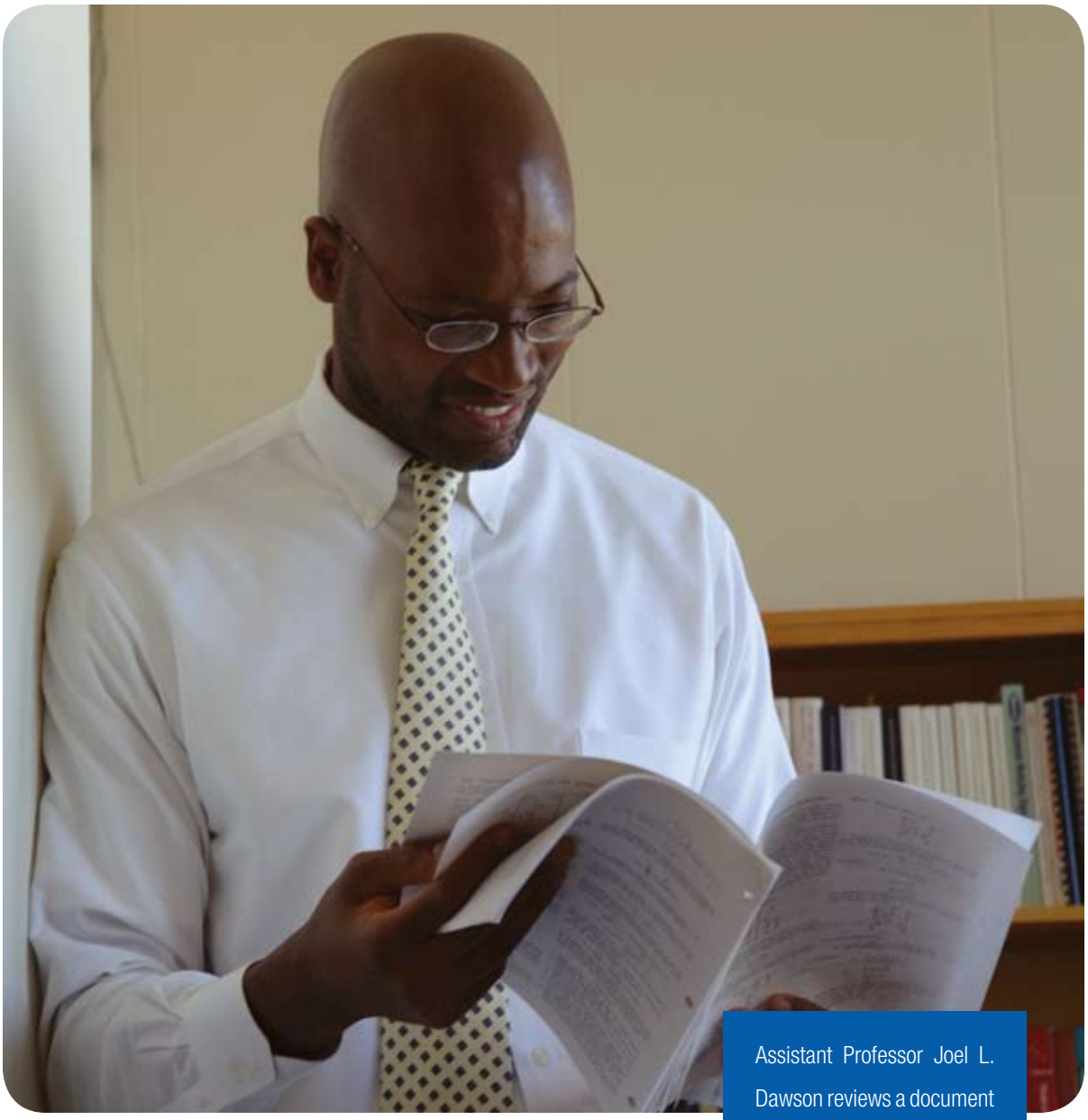
The faculty and staff at MIT in photonics related areas have included Claude Shannon (founder of information theory), Charles Townes (inventor of the laser), Robert Rediker (inventor of the semiconductor lasers), and Hermann Haus (inventor of the single frequency semiconductor laser & ultrafast optical switch). CIPS affiliated faculty and staff continue this tradition of excellence in areas ranging from optical network architectures to novel optical devices to novel photonic materials.

3. To integrate member companies into the MIT photonics community.

CIPS will host annual meetings and seminars in photonics. For CIPS member companies, focused visits to the Institute for individual companies will be organized with faculty and graduate students. In addition, CIPS will hold forums geared towards the creation of campus-industry teams to pursue large-scale research programs. CIPS will host poster sessions at the annual meeting so as to introduce graduate students and their research to industry.

CIPS publications will include a resume book of recent graduate students in the area of photonics. Graduates of the Massachusetts Institute of Technology have founded 4,000 firms which, in 1994 alone, employed at least 1.1 million people and generated $232 billion of world sales. Photonics related companies founded by alumni include Sycamore Networks, Analog Devices, Texas Instruments, Hewlett-Packard, and 3Com as well as recent start-up such as OmniGuide.

Member companies have the opportunity to guide the research of CIPS faculty and students through the Working Groups (WGs) and individual graduate student awards.



Assistant Professor Joel L. Dawson reviews a document in his office.

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PUBLICATIONS

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PUBLICATIONS

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PUBLICATIONS

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Berggren, K.K., "Quantum computing with superconductors," In *Proceedings of the IEEE*, vol. 92, pp. 1630, 2004.

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Tudela, M.A., Lagace, P.A., and Wardle, B.L., "Buckling response of transversely loaded composite shells – part 1: experiments," *AIAA Journal*, vol. 42, no. 7, pp. 1457-1464, July 2004.

Wardle, B.L., Lagace, P.A., and Tudela, M.A., "Buckling response of transversely loaded composite shells – part 2: numerical analysis," *AIAA Journal*, vol. 42, no. 7, pp. 1465-1473, July 2004.

Jacob White
Professor
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COLLABORATORS

L. Daniel, MIT
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GRADUATE STUDENTS

J. Bardhan, Research Assistant, EECS
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T. Klemas, Research Assistant, EECS
S. Kuo, Research Assistant, EECS
J.H. Lee, Research Assistant, EECS
D. Vasilyev, Research Assistant, EECS
A. Vithayathil, Research Assistant, EECS (Graduated)
D. Willis, Research Assistant, Aero-Astro
Z. Zhu, Research Assistant, EECS (Graduated)

SUPPORT STAFF

C. Collins, Administrative Assistant

PUBLICATIONS

Ye, W., Wang, X., Hemmert, W., Freeman, D.M., and White, J., "Air damping in laterally oscillating microresonator: a numerical and experimental study," *IEEE Journal of Microelectromechanical Systems*, vol. 12, no. 5, pp. 557-566, 2003.

Daniel, L., Siong, O.C., Chay, L.S., Lee, K.H., and White, J., "A multiparameter moment matching model reduction approach for generating geometrically parameterized interconnect performance models," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 23, no. 5, pp. 678-693, May 2004.

Marques, N., Kamon, M., Silveira, L.M., and White, J., "Generating compact, guaranteed passive, reduced-order models of 3D RLC interconnects," *IEEE Transactions on Advanced Packaging*, vol. 27, no. 4, pp. 569-580, Nov. 2004.

Li, J., and White, J., "Low-rank solution of lyapunov equations," Selected for Republication in *SIAM Review*, vol. 46, no. 4, p. 693-713, 2004.

Vasilyev, D., Reqienski, M., and White, J., "Perturbation analysis of TBR model reduction in application to trajectory-piecewise linear algorithm for MEMS structures," In *Proc. of Modeling and Simulation of Microsystems*, Mar. 2004.

Willis, D.J., White, J., and Peraire, J., "A pFFT accelerated linear strength BEM potential solver," In *Proc. of Modeling and Simulation of Microsystems*, Mar. 2004.

Coelho, C.P., White, J.K., and Silveira, L.M., "Dealing with stiffness in time-domain stokes flow simulation," In *Proc. of Modeling and Simulation of Microsystems*, Mar. 2004.

Daniel, L., and White, J., "Numerical techniques for extracting geometrically parameterized reduced order interconnect models from full-wave electromagnetic analysis," In *Proceedings of the IEEE AP-S International Symposium and USNC / URSI National Radio Science Meeting*, 2004.

White, J., "CAD challenges in bioMEMS design," In *Proceedings of the Design Automation Conference*, pp. 629-632, 2004.

Zhu, Z., Demir, A. and White, J., "A stochastic integral equation method for modeling the rough surface effect on interconnect capacitance," In Proceedings of the IEEE Conference on Computer-Aided Design, 2004.

Bardhan, J., Altman, M.D., Lippow, S.M., Tidor, B., and White, J.K., "A curved panel integration technique for molecular surfaces," To appear in Proc. of Modeling and Simulation of Microsystems, 2005.

Coelho, C., Desai, S., Freeman, D., and White, J., "A robust approach for estimating diffusion constants from concentration data in microchannel mixers," To appear in Proc. of Modeling and Simulation of Microsystems, 2005.

Lee, J.H., Vasilyev, D., Vithayathil, A., Daniel, L., and White, J., "Accelerated optical topography inspection using parameterized model order reduction," To appear in Proceedings of the IEEE International Microwave Symposium, 2005.

Hu, X., White, J., and Daniel, L., "Analysis of conductor impedance over substrate using novel integration techniques," To appear in Proceedings of the Design Automation Conference, 2005.

Klemas, T., Daniel, L., and White, J., "Segregation by primary phase factors: a full-wave algorithm for model order reduction," To appear in Proceedings of the Design Automation Conference, 2005.

Klemas, T., Daniel, L., and White, J., "A fast full-wave algorithm to generate low order electromagnetic scattering models," To appear in International Symposium on Antennas and Propagation and USNC/URSI National Radio Science Meeting, 2005.

THESES AWARDED

Bachelor of Science (S.B.)

Aponte, J.D. (T. Thorsen), "Characterization of Microfluidic Valves," June 2003.

Barron, K, (G. Chen), "Experimental Studies of the Thermoelectric Properties Of Microstructured and Nanostructured Lead Salts," February, 2005.

Bathurst, S. (N.P. Suh) "Use of Axiomatic Design to Improve the Wear Characteristics of Rotary Shaft Seals," June 2003.

Bishoff, A. N. (G. Chen), "A New Approach to the Electronic Pen Idea," May 2003.

Buckley, P. (M.L. Culpepper),"Wear Characteristics of Hybrid Flexure Joints," June 2003.

Cukalovic, B. (J.A. del Alamo), "WebLabSim Administrative Interface," May 2005.

Funes, F. (G. Barbastathis), "Measurement of a New Electrochemical Capacitor and the Creation of its Dielectric Medium," June 2004.

Gibbons, J.S. (T. Thorsen), "Mobile Power Plants: Waste Body Heat Recovery," June 2004.

Kessenich, G. (M.L. Culpepper), "Factors Affecting the Integral Spring Force in Compliant Robot Joints," June 2003.

Korb, S. (M.L. Culpepper), "Design of a Monolithic, Three-dimensional Compliant Hexapod," June 2004.

Mazzeo, B. (A.I. Akinwande), "Models for Energy States in Thin Film Transistors," May 2005.

Odhner, L.U. (N.P. Suh) "Functional Thinking in Cost Estimation Through the Tools and Concepts of Axiomatic Design," June 2004.

Peliks, B. (N.P. Suh) "Axiomatic Redesign: Using Axiomatic Design to Improve Vehicle Performance of the Steering and Suspension System," June 2003.

Samouhos, S.V. (T. Thorsen), "Mobile Power Plants: Waste Body Heat Recovery," June 2004.

Shih, T. (G. Barbastathis), "Three Dimensional Imaging of Translucent Objects Using Volume Holographic Techniques," June 2004.

Slowe, T. (M.L. Culpepper), "Development of Equipment for Manufacturing Formed and Folded Compliant Mechanisms," June 2004.

Swanson, S. (M.L. Culpepper), "Development of an Assessment Protocol for Engineering Education," June 2003.

Tsikata, S. (T. Thorsen), "Microfluidic Optical Devices," June 2004.

Master of Engineering (M. Eng.)

Akilian, M.K. (M.L. Schattenburg), "Thin Optic Surface Analysis for High Resolution X-ray Telescopes," , September 2004.

Anderson, G. (M.L. Culpepper), "A Six Degree-of-Freedom Flexural Positioning Stage," February 2003.

Carl, P. (M.L. Culpepper), "Design of Accurate and Repeatable Micro-fixtures and Manipulators for Micro-optical Systems", June 2004 (joint with Technischen Universitaet Muenchen).

Chang, C.-H. (M.L. Schattenburg), "Fabrication of Extremely Smooth Blazed Gratings," June 2004.

Chen, S.C. (M.L. Culpepper), "Design of Integral Alignment in Silicon Optical Bench," September, 2003.

Das, R. (M.A. Baldo) "Photovoltaic Devices Using Photosynthetic Protein Complexes," February 2004.

Edalat, F. (C.G. Sodini), "Effect of Power Amplifier Nonlinearity on System Performance Metric, Bit-Error-Rate (BER)," September 2003.

Gadish, N. (J. Voldman), "A Microfabricated Dielectrophoretic Micro-organism Concentrator," August 2005.

Gerhardt, A. (M.A. Schmidt), "Arrayed Microfluidic Actuation for Active Sorting of Fluid Bed Particulates," December 2003.

Hanlon, C. (C. Boppe, Z.S. Spakovszky), "Engine Design Implications for a Blended Wing Body Aircraft with Boundary Layer Ingestion," January 2003.

Ho, J. (V. Bulovic), "Improving the External Extraction Efficiency of Organic Light Emitting Devices," February 2004.

Hou, S.M.C. (J.H. Lang), "A Piezo-Tunable Gigahertz Cavity Microelectromechanical Resonator", May 2004.

Crain, E.A. (M.H. Perrott), "Fast Offset Compensation for a 10 Gbps Limit Amplifier," May 2004.

Jurga, Stanley M. (G. Barbastathis), "Nanostructured Origami," May 2003.

Kumar, R. (M.A. Baldo) "Solid-State Integration of Photosynthetic Protein-Molecular Complexes," May 2003.

Kohen, S.M. (Q. Hu), "Electromagnetic Modeling of Terahertz Quantum Cascade Laser Waveguides and Resonators," May 2004.

Landsiedel, N. (M.L. Culpepper), "Design of a Formed / Folded Compliant Layered Mechanism," February 2005.

Lorilla, L. (C.G. Sodini), "Filtering Techniques for Mitigating Microwave Oven Interference on 802.11b Wireless Local Area Networks," May 2003.

M. Eng. continued

Mehta, A. (M.A. Schmidt, K.F. Jensen), "A Microfabricated Solid Oxide Fuel Cell," June 2004.

Muller, R. (J. Voldman), "A Microfabricated Dielectrophoretic Micro-organism Concentrator," May 2004.

Pakalapati, L.V.V. (M.J. Cima), "Controlled Release Microchip," June 2003.

Powell, M. (C.G. Sodini), "Integrated Feedback Circuit for Organic LED Display Drivers," March 2004.

Pei, C-W. (C.G. Sodini), "Macromodeling and Demonstration of the LT6600 Amplifier and Lowpass Filter," February 2004.

Peters, J. (L. Daniel), "Design of High Quality Factor Spiral Inductors in RF MCM-D", September 2004.

Rodriguez, S. (L.A. Kolodziejski), "Towards Photonic Integrated Circuits: Design and Fabrication of Passive InP Waveguide Bends," June 2004.

Signoff, D. (C.G. Sodini), "A High Bandwidth, Low Distortion, Fully Differential Amplifier," June 2005.

Szczesny, S. (M.L. Culpepper), "Design of Compliant Mechanisms for Attenuation Vibrations in Rotational Systems," February 2005.

Solis, A. (J.A. del Alamo), "MIT Device Simulation WebLab: An Online Simulator for Microelectronic Devices," September 2004.

Tang, B. (D.S. Boning), "Characterization and Modeling of Polysilicon MEMS Chemical-Mechanical Polishing," May 2004.

Varadarajan, K. (M.L. Culpepper), "Design of Ultra-Precision Fixtures for Nanomanufacturing," February 2005.

Walker J.Z. (A. I.. Akinwande, A. Chandrakhasan), "A Low Power Display Driver with Simultaneous Image Transformation," February 2005.

Wang, A.I., (A.I. Akinwande), "Threshold Voltage in Pentacene Field Effect Transistors with Parylene Dielectric," May 2004.

Werkmeister, J. (A. Slocum), "Development of Silicon Insert Molded Plastic (SIMP)," June 2005.

Yu, J. (V. Bulovic), "A Smart Active Matrix Pixelated OLED Display," January 2004.

Master of Science (S.M.)

Abu-Ibrahim, F. (A. Slocum), "Low-cost Precision Waterjet," June 2004.

Arango, A. (V. Bulovic), "Quantum Dot Heterojunction Photodetector," February 2005.

Au, H. (C. Livermore), "Solder Self-Assembly for MEMS Fabrication," September 2004.

Castiella, J.C. (Z.S. Spakovszky),"A Novel Design Methodology for Enhanced Compressor Performance Based on a Dynamic Stability Metric," January 2005.

Chan, E.P. (E.L. Thomas), "Layered-Silicate Triblock Copolymer Nanocomposites," June 2003.

Chen, K.N. (R. Reif), "Material Analysis and Characterization of Copper Wafer Bonding in 3-D Technology," February 2003.

Chen, L.Y. (A. I. Akinwande), "Focused Field Emission Devices," June 2003.

Cheung, K. (M.A. Schmidt), "Die Level Glass Frit Vacuum Packaging for a Micro-Fule Processor System," May 2005.

Cline, J. (A.P. Chandrakasan), "Characterization of Schottky Barrier Carbon Nanotube Transistors and their Applications to Digital Circuit Design," May 2004.

Cord, B.M. (T.P. Orlando), "Rapid Fabrication of Deep-Submicron Josephson Junctions," May 2004.

Cybulski, J.S. (G.Chen), "Fabrication, Modeling, and Electrical Characterization of Self-Assembling Microscale Rollup Structures," June 2004.

Diez, S. (A.H. Epstein, Z.S. Spakovszky), "Preliminary Performance Characteristics of a Microfabricated Turbopump," September 2003.

Dorca-Luque, J. (Z.S. Spakovszky), "Application of an Energy-Like Stability Metric for Axial Compressor Design," August 2003.

Drake, T (J.L. Hoyt), "Fabrication of Ultra-thin Strained Silicon on Insulator," June 2003.

Drego, N.A. (D.S. Boning, M.H. Perrott), "A Low-Skew, Low-Jitter Receiver Circuit for On-Chip Clock Distribution," June 2003.

El Aguizy, T. (S.G. Kim), "Nanopelleting of Carbon nanotubes," May 2004.

Hennessy, J. (D.A. Antoniadis), "Germanium on Insulator Fabrication Technology," June 2004.

Ho Duc, H.L. (M.J. Cima), "Packaging for a Drug Delivery Microelectromechanical System," February 2005.

Kang, S.H. (V. Bulovic), "Evaporative Printing of Organic Materials and Metals and Development of Organic Memories," September 2004.

S.M. continued

Kangude, Y, (L.A. Kolodziejski), "Red Emitting Photonic Devices Using InGaP/InGaAlP Material System," June 2005.

Kern, A. (A.P. Chandrakasan), "PLL-Based Active Optical Clock Distribution," September 2004.

Kuo, S. (M.H. Perrott), "Linearization of a Pulse Width Modulated Power Amplifier," June 2004.

Lee, H. (M.J. Cima), "Experimental Study of the Atomization Process for Viscous Liquids by Meniscus Perturbation and Micro Air Jet," June 2004.

Lee, H. (G. Chen) "Thermoelectric Properties of Si-Ge Nanocomposites," January 2005.

Lei, Y.S.V. (C.G.Fonstad, Jr.), "Post-Assembly Process Development for Monolithic OptoPill Integration on Silicon CMOS," May 2004.

LeCoguic, A. (J. Han), "Gate Potential Control of Nanofluidic Devices," May 2004.

Levy-Tzedek, S. (S.R. Manalis), "Biological detection by means of mass reduction in a suspended microchannel resonator," May 2004.

Limketkai, B.N. (M.A. Baldo) "The Density of States at a Rough Metal-Organic Interface," September 2003.

Liang, J. (C.G. Sodini), "On-Chip Cross-Talk Analysis for Multiple RF Front Ends of a Wireless Gigabit LAN System," September 2004.

Mandal, S. (R. Sarpeshkar), "RF Power Extraction Circuits," May 2004.

Manneville, A. (Z.S. Spakovszky), "Propulsion System Concepts for Silent Aircraft," May 2004.

Mao, P. (J. Han), "Fabrication and Characterization of Nanofluidic Channels for Studying Molecular Dynamics in Confined Environments," January 2005.

Mattson, E. (L.A. Kolodziejski), "Design and Fabrication of an Electrically-Activated Photonic Crystal Nanocavity Laser," June 2005.

Nayfeh, O. (D.A. Antoniadis), "On the relationship between electron mobility and velocity in sub-50 nm MOSFETs via calibrated Monte-Carlo simulation," June 2004.

Ogunnika, O.T. (M.H. Perrott), "A Simple Transformer-Based Resonator Architecture for Low Phase Noise LC Oscillators," October 2003.

Pilczer, D. (Z.S. Spakovszky), "Noise Reduction Assessments and Preliminary Design Implications for a Functionally-Silent Aircraft," May 2003.

Perrot, V. (Z.S. Spakovszky), "A Design Optimization Framework for Enhanced Compressor Stability Using Dynamic System Modeling," August 2003.

Powell, J. (A.P. Chandrakasan), "Antenna Design for Ultra Wideband Radio," May 2004.

Schmidt, A.J. (G. Chen), "Photothermal Lithography," June 2004.

Shah, A. (G. Chen), "Modeling and Fabrication of High Power Density Micro Thermophotovoltaic Devices," December 2003.

Shur, M. (C.F. Dewey, Jr.) "Microfabrication Methods for the Study of Chemotaxis," June 2004.

Shusteff, M. (S.R. Manalis), "A microfabricated hollow cantilever for sub-nanoliter thermal measurements," September 2003.

Taff, B.M. (J. Voldman), "Design and Fabrication of an Addressable MEMS-Based Dielectrophoretic Microparticle Array," June 2004.

Teo, M.S. (C.G. Fonstad, Jr.), "Development of Pic-and-Place techniques for Monolithic OptoPill Integration," January 2005.

Thompson, K. (A. Slocum), "MEMS Fluid Coupling," June 2004.

Tiefenbruck, L. (V. Bulovic), "Visible Spectrometer Utilizing Organic Thin Film Absorption," May 2004.

Tischler, J. (V. Bulovic), "Electrically Pumped Exciton-Polariton Emission in a J-Aggregate OLED at Room Temperature," August 2003.

Vachhani, N.A. (E.L. Thomas), "Using Narrowband Pulse-shaping to Characterize Polymer Structure and Dynamics: Deathstar Ghz Spectroscopy," February 2005.

Wang, Y.C. (J. Han), "On-chip Multi-dimensional Biomolecule Separation Using Multi-layer Microfabricated Valves," January 2004.

Wentzloff, D.D. (J.H. Lang, T.A. Keim), "Experimental Characterization of an Integrated Starter/Generator," August 2002.

Wong, M. (J.A. del Alamo), "The Effect of Varying Gate-Drain Distance on the RF Power Performance of Pseudomorphic High Electron Mobility Transistors," August 2005.

Wu, T.M. (R. Reif), "Carbon Nanotube Applications for CMOS Back-End Processing," February 2005.

Doctor of Philosophy (Ph.D.)

Acosta-Serafini, P. (C.G. Sodini), "A Programmable Wide-Dynamic Range CMOS Image Sensor," February 2004.

Arana, L. (K.F. Jensen, M.A. Schmidt), "High-Temperature Microfluidic Systems for Thermally-Efficient Fuel Processing," May 2003.

Assefa, S. (L.A. Kolodziejski), "The Development of Novel Passive and Active Photonic-Crystal Devices," June 2004.

Awtar, S. (A. Slocum), "Synthesis and Analysis of Parallel Kinematic XY Flexure Mechanisms," January 2004.

Braff, R. (M.A. Schmidt, M. Gray), "Controllable Vapor Microbubbles for Use in Bioparticle Actuation," April 2003.

Brienlinger, K. (A. Slocum), "Three Dimensional Routed Manifolds with Externally Inserted Cables," June 2003.

Chen, A. (H.S. Lee, A.I. Akinwande) "CMOS-Compatible Compact Display," June 2005.

Chen, C.G. (M.L. Schattenburg), "Beam Alignment and Image Metrology for Scanning Beam Interference Lithography – Fabricating Gratings with Nanometer Phase Accuracy," April 2003.

Chen, K.N. (R. Reif), "Copper Wafer Bonding in Three-Dimensional Integration," February 2005.

Choy, H.K.H. (C.G. Fonstad, Jr.), "Quantum Wells on Indium Gallium Arsenide Compositionally Graded Buffers Realized by Molecular Beam Epitaxy," Janruary 2005.

Cooper, E.B. (S.R. Manalis), "Silicon Field-effect Sensors for Biomolecular Assays," September 2003.

Crankshaw, D.S. (T.P. Orlando), "Measurement and On-chip Control of a Niobium Persistant Current Qubit," June 2003.

Das, S. (A.P. Chandrakasan, R. Reif), "Design Automation and Analysis of Three-Dimensional Integrated Circuits," June 2004.

De Mas Valls, N. (K.F. Jensen, M.A. Schmidt), "Scalable Multiphase Microchemical Systems for Direct Fluorination," January 2004.

Hong, C.Y. (A.I. Akinwande), "Integrated MOSFET/Field Emitter Array Devices," June 2003.

Kim, G.S. (K.F. Jensen), "Multiscale Modeling of Thin Film Deposition Processes," September 2002.

Klemas, T. (J. White), "Full-wave Algorithms for Model Order Reduction and Electromagnetic Analysis of Impedance and Scattering," May 2005.

Konistis, K. (Q. Hu), "A Heterojunction Bipolar Transistor with Stepwise Alloy-Graded Base: Analysis, Design, Fabrication, and Characterization," August 2004.

Konkola, P.T. (M.L. Schattenburg), "Design and Analysis of a Scanning Beam Interference Lithography System for Patterning Gratings with Nanometer-Level Distortion," ME, April 2003.

Koser, H. (J.H. Lang), "Development of Magnetic Induction Machines for Micro Turbo Machinery," June 2002.

Kymissis, I. (A.I. Akinwande), "Organic Field Emission Devices," June 2003.

Lee, J. (K.F. Jensen), "Semiconductor Nanocrystal Composite Materials and Devices," June 2002.

Lee, T. (N.P. Suh) "Complexity Theory in Axiomatic Design," June 2003.

Li, J. (J.H. Lang, A.H. Slocum), "Electrostatic Zipping Actuators and Their Application to MEMS," February 2004.

Liu, W. (G. Chen), "In-Plane Thermoelectric Properties of Si/Ge Superlattices," July 2004.

Love, N. (I. Masaki), "Recognition of 3D Compressed Images and its traffic monitoring applications," June 2004.

Lu, H. (K.F. Jensen, M.A. Schmidt), "Microfluidic Biomechanical and Electrical Devices for Rapid Analysis of Cells and Organelles", May 2003.

Maldovan, M. (E.L. Thomas), "Exploring for New Photonic Band Gap Structures," January 2004.

Mascaro, D. (V. Bulovic, T. Swager), "Formation of In-Plane Crystals of Molecular Organic Semiconductors," June 2004.

Melvin, J. (N.P. Suh) "Axiomatic System Design : Chemical Mechanical Polishing Machine Case Study," June 2003.

Meninger, S.E. (M.H. Perrott), "Low Phase Noise, High Bandwidth Frequency Synthesizer Techniques," June 2005.

Min, Rex (A.P. Chandrakasan), "Energy and Quality Scalable Wireless Communication," June 2003.

Mur Miranda, J.O. (J.H. Lang), "Electrostatic Vibration-to-Electric Energy Conversion", February 2004.

Nakada, D.Y. (T.P. Orlando), "Fabrication and Measurement of a Niobium Persistant Current Qubit," June 2004.

Nemirovskaya. M.A. (K.F. Jensen), "Multiscale Modeling Strategies for Chemical Vapor Deposition," September 2002.

Nielson, G.N. (G. Barbastathis), "Micro-opto-mechanical Switching and Tuning for Integrated Optical Systems," July 2004.

Qiu, J. (J.H.Lang, A. Slocum), "An Electrothermally-Actuated Bistable MEMS Relay for Power Applications", June 2003.

Rewienski, M. (J. White), "A Trajectory Piecewise-Linear Approach to Model Order Reduction of Nonlinear Dynamical Systems," June 2003.

Ph.D. continued

Savran, C. (S.R. Manalis), “A Micromechanical Biosensors with Inherently Differential Readout,” February 2004.

Shi, Y. (S.G. Kim), “A Self-Cleaning Lateral Contact RF MEMS Switch,” August 2004.

Sihler, J. (A. Slocum), “A Low Leakage 3-Way Silicon Microvalve,” January 2004.

Sinha, A. (G. Barbastathis), “Imaging Using Volume Holograms,” February 2004.

Song, D. (G. Chen) “Phonon Heat Conduction in Nano and Micro-Porous Thin Films,” June 2003.

Sparks, A. (S.R. Manalis), “Scanning Probe Microscopy with inherent Disturbance Suppression,” February 2004.

Steym. J.L. (J.H. Lang), “A Microfabricated ElectroQuasiStatic Induction Turbine-Generator,” June 2005.

Tandon, S. (L. A. Kolodziejski), “Engineering Light Using Large Area Photonic Crystal Devices,” June 2005.

Tsau, C. (M.A. Schmidt, S.M. Spearing) “Characterization of Wafer-Level, Gold-Gold Thermocompression Bonding,” August 2003.

Urbas, A. (E.L. Thomas), “Block Copolymer Photonic Crystals,” June 2003.

Velasquez, L.F. (A.I. Akinwande, M. Martinez-Sanchez), “Micro-Fabricated Ion Engines,” June 2004.

Wang, Alice (A.P. Chandrakasan), “An Ultra-Low Voltage FFT Processor Using Energy- Aware Techniques,” December 2003.

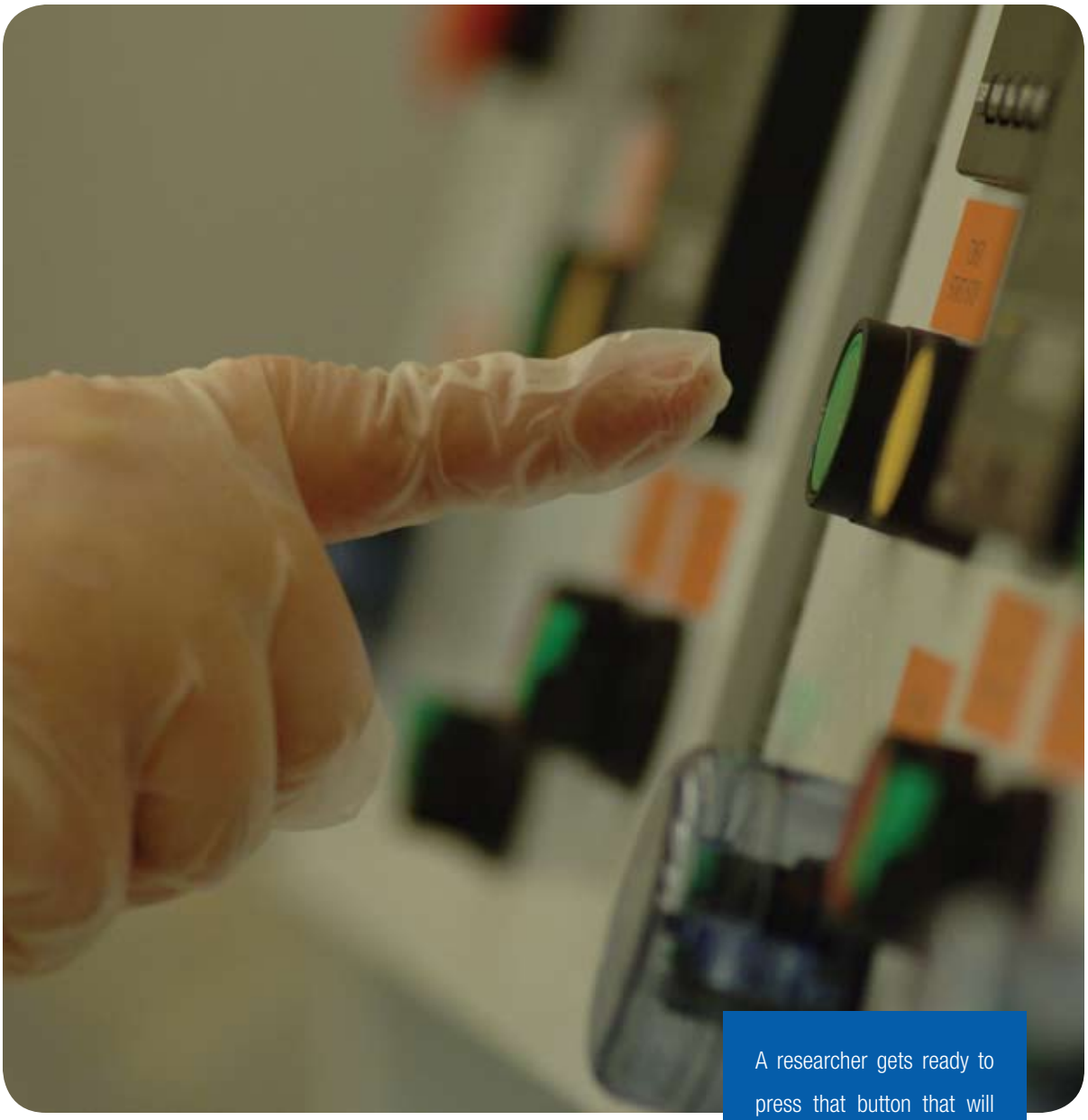
Wang, Andrew Yu, (C.G. Sodini), “Base Station Design for a Wireless Microsensor System,” June 2005.

White, J. (A. Slocum), “The Nanogate: Nanoscale Flow Control,” June 2003.

Yang, B. (G. Chen), “Thermal and Thermoelectric Transport in Superlattices and Quantum Wells,” June 2003.

Zanzotto, A. (K.F. Jensen), “Integrated Microbioreactors for Rapid Screening and Analysis of Bioprocesses,” February 2005.

Zhu, Z. (J. White), ``Efficient Integral Equation Based Algorithms for Parasitic Extraction of Interconnects with Smooth or Rough Surface,” September 2004.



A researcher gets ready to press that button that will begin a new process in ICL.

FACILITIES

FACILITIES

Process research and device fabrication at MTL are primarily conducted in three laboratories; the Integrated Circuits Laboratory (ICL), the Technology Research Laboratory (TRL) and the Exploratory Materials Laboratory (EML). The ICL is designed, equipped and staffed to serve as a highly advanced silicon integrated circuit, device, structures, and process research facility. The laboratory houses a complete six-inch silicon IC fabrication line. Cassette-to-cassette transfer techniques are employed extensively, and VLSI discipline is maintained throughout the facility.

The TRL supports the development of novel process technologies and provides facilities for the fabrication of novel micro and nanostructures

The EML is a highly flexible microfabrication resource with all the basic fabrication capabilities and few limitations, beyond those called for by safety protocols, on substrate and source materials

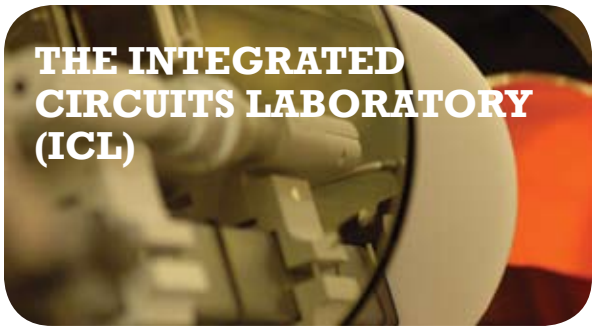
The TRL and ICL are complementary laboratories. Since the ICL is designed to permit fabrication of complex integrated circuits and devices, by necessity it must be operated under the strict discipline that is required for state-of-the-art silicon device and circuit research. The TRL is designed to make up for any loss of flexibility that this discipline imposes. Similarly, fabrication of devices in the ICL can readily take advantage of new technologies that have been developed in the TRL. Examples of such technologies include deep reactive ion etching and wafer bonding. The Class 100 clean room environment and clean room procedures employed in the TRL assure that wafers can move between the ICL and TRL without compromising either the wafers or the facilities.

EML provides an additional degree of flexibility for samples that do not require strict cleanliness or contamination control. Samples that have been in EML cannot be transferred into ICL or TRL.

In addition to these MTL facilities, the Research Laboratory of Electronics (RLE) maintains a shared Scanning Electron Beam Facility (SEBL) with access to direct-write e-beam capabilities

MTL has continued to serve the microfabrication needs of the MIT community, working on projects from an ever-larger variety of academic departments (e.g., Biology, Chemical Engineering, Mechanical Engineering, Physics). Recently, the Scanning Electron Beam Facility (SEBL) was qualified to be compatible with TRL processes, adding nanometer-size capability to our lithography tool set. The Process Technology Committee reviews all new processes in ICL/TRL to ensure the integrity of all processes.

A detailed list of equipment and use protocols for MTL can be found on the MTL web site (http://mtlweb.mit.edu).



THE INTEGRATED CIRCUITS LABORATORY (ICL)

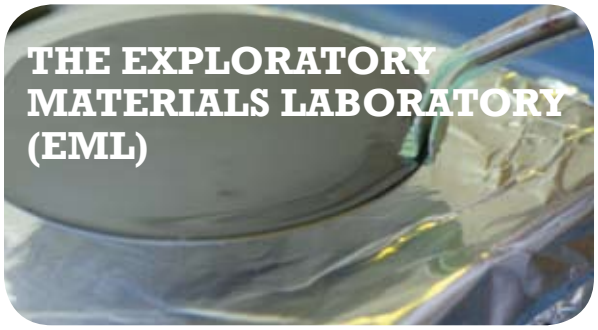
7,910 sq-ft integrated circuit fabrication facility comprised of:

- 2,800 sq.-ft Class 10 clean space
- 4,000 sq.-ft support space
- 460 sq.-ft characterization space

THE TECHNOLOGY RESEARCH LABORATORY (TRL)

3,600 sq-ft of laboratory space comprised of:

- 2,200 sq.-ft class 100 clean space
- 1,400 sq.-ft support space



THE EXPLORATORY MATERIALS LABORATORY (EML)

This is a flexible thin film deposition lab, with photolithography, etching and metrology capabilities.

- 2,100 sq.-ft class 10,000 clean space

PERSONNEL AND COMMITTEES

Director's Office

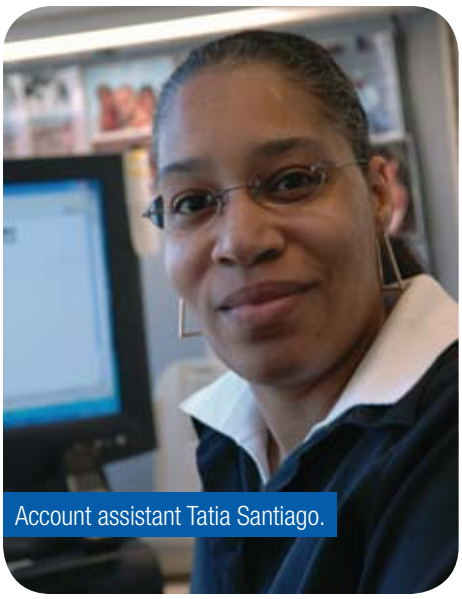
M. Schmidt, Director
A. Chandrakasan, Faculty Associate Director
J. del Alamo, Faculty Associate Director
J. Hoyt, Faculty Associate Director
S. Crooks, Associate Director
V. Diadiuk, Associate Director

MTL Faculty Policy Board

D. Antoniadis, Professor, EECS
D. Boning, Assoc Dept. Head, EECS and Professor, EECS
A. Chandrakasan, Professor, EECS
J. del Alamo, Professor, EECS
J. Hoyt, Associate Professor, EECS
M.A. Schmidt, MTL Director and Professor, EECS (Chair)
C.G. Sodini, Professor, EECS
S. Crooks, Associate Director (ex-officio)
V. Diadiuk, Associate Director (ex-officio)

Administrative Services

S. Crooks, Associate Director and Administrative Officer
D. Hodges-Pabon, Personnel Officer
A. Adams-Heath, Fiscal Officer
M. Karapetian, Media Specialist
T. Santiago, Account Assistant (Billing)
D. Moore, Accounts Payable



Account assistant Tatia Santiago.

Fabrication Services

V. Diadiuk, Associate Director and Principal Research Engineer
P. Varley, Clerical Assistant

Fabrication
D. Adams, Research Specialist, Techn. Supervisor
D. Terry, Project Technician
T. Turner, Technician A
M. Klotz, Technician C

Diffusion and Device Characterization
B. Alamariu, Research Engineer

Vacuum Etching
R. Bicchieri, Research Specialist
D. Jameson, Research Specialist
E. Lim, Research Specialist

Vacuum Deposition
P. Zamora, Research Specialist

EML Processes
K. Broderick, Research Associate

Facilities
P. McGrath, Research Specialist

Equipment Maintenance
B. McKenna, Research Specialist

CORAL and Web Applications
I. Lin, Research Specialist

Photolithography
P. Tierney, Research Specialist

Project Processing
S. Poesse, Research Specialist

Computational Services

J. del Alamo, Professor and Associate Director
T. Lohman, Research Specialist, System/CIM Manager
M. Hobbs, Research Specialist, System Manager
W. Maloney, Research Specialist, System Manager

CAD Services

A. Chandrakasan, Professor and Associate Director
M. McIlrath, Research Specialist, System/CAD Manager

Process Technology Committee (PTC)

A. Akinwande, Associate Professor, EECS
V. Diadiuk, MTL Associate Director, Operations (Chair)
J. Lang, Professor, EECS
C. Livermore, Assistant Professor, MechE
J. Hoyt, Associate Professor, EECS
D. Isaacson, MSE
A. Khakifirooz, EECS
O. Nielson, ChemE
N. Waldron, EECS

PTC meeting in progress, from left to right: Ali Khakifrooz, David Isaacson, Niamh Waldron, Jifeng Liu, Judy Hoyt, Vicky Diadiuk.

VLSI MEMO SERIES

MTL maintains a comprehensive pre-publication Memo Series covering the activities of MTL and related microsystems research at MIT. A chronological list of memos issued from 2003-present appears below Copies of MTL Memos are available online exclusively to members of the Microsystems Industrial Group (MIG) at MTL. MIG members are invited to sign up for an account that will grant them access to these materials in a password-protected directory.

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05-1147	Copper Wafer Bonding in Three-Dimensional Integration	K.N. Chen
05-1148	A CMOS-Compatible Compact Display	A.R. Chen
05-1149	Low-Power Digital Processor for Wireless Sensor Networks	D.F. Finchelstein
05-1150	Development of Silicon Insert Molded Plastic (SIMP)	J.B. Werkmeister
05-1151	Switchable Stiffness Scanning Microscope Probe	C.T. Mueller-Falcke
05-1152	Hybrid Organic/Quantum Dot Thin Film Structures and Devices	S. Coe-Sullivan
05-1153	Low Phase Noise, High Bandwidth Frequency Synthesis Techniques	S.E. Meninger
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05-1156	Design for Manufacturability with Regular Fabrics in Digital Integrated Circuits	M. Gazor
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VLSI SEMINAR SERIES

MTL hosts a series of talks each semester known as the MTL VLSI Seminar Series. Speakers for the Series are selected on the basis of their knowledge and competence in the areas of microelectronics research, manufacturing, or policy. The MTL VLSI Seminar Series is held on the MIT Campus on Tuesdays at 4:00 pm, and is open to the public. A listing of recent seminars is also provided at http://mtlweb.mit.edu. Streaming videos of the VLSI Seminar Series are available online exclusively to individuals whose companies are members of the Microsystems Industrial Group (MIG) at MTL. For information regarding the MTL VLSI Seminar Series, send e-mail to debb@mtl.mit.edu.

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Yannis Tsividis, Department of Electrical Engineering, Columbia University
Continuous-Time Digital Filters and Other Mixed-Domain Processors

March 1, 2005
Bill Krenik, Texas Instruments
Wireless Handset Electronics -- Evolution to 3G and Beyond

March 8, 2005
Timothy Brunner, IBM
Lithography Technology for 45nm CMOS

March 15, 2005
Barbara Chappell, Intel Corporation
CMOS Digital Circuit Design Challenges in the Nanotechnology Era

April 5, 2005
Dr. Rama Divakaruni, IBM
Stressed Si for improved Microprocessor performance

April 12, 2005
Ahmed Busnaina, Northeastern University
Electronics Nanomanufacturing through Directed Assembly of Nanoelements

April 26, 2005
Sven Moller, Hewlett Packard
Nanotechnology Enabling Bio-Sensing Applications: Applications and Challenges

May 3, 2005
Michael G. Kane, Sarnoff Corporation
A High Performance Semiconductor Technology for Large-Area Flexible Substrates

FALL 2004

September 14, 2004
Dr. Simon M . Sze, National Nano Device Laboratories
Evolution of Nonvolatile Semiconductor Memory - from Invention to Nanocrystal Memory

September 28, 2004
Dr. Farrokh Ayazi, Georgia Tech
Bulk-Mode Micro and Nano Mechanical Resonators in RF and Biology

October 5, 2004
Dr. Norman Rohrer, IBM
PowerPC 970 and 970FX in 130nm and 90nm Technologies

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Progress towards development of all-printed RFID tags and sensors: Materials, Devices, and Circuit Implications

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Michael Perott, Massachusetts Institute of Technology
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David Schut, Hewlett Packard
Hewlett-Packard: MEMs and Memory Technology Development - the Story of Atomic Resolution Storage

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CMOS Devise Scaling Strategy

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Chris Menkus, National Semiconductor Corp.
High Speed Self-Calibrating Folding ADC

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Gerry Talbot, AMD
Chip to Chip Serial I/O Interconnects, Today and the Future

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Embedded DSP for Wireless Systems

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Paul E. Baude, 3M company
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Phil Kuekes, HP
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Joerg Appenzeller, IBM
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Thomas Chen & Tim Denison, Analog Devices, Inc.
The Next Generation MEMS Design and Process Combining SOI and CMOS (SOIMEMS)

November 4, 2003
V. Srinivasa Somayazulu, Intel
Design Challenges for High Data Rate UWB Wireless Networks

November 18, 2003
Mark Rodder, TI
Metal Gate CMOS Issues and Challenges

ABBREVIATIONS

Massachusetts Institute of Technology

ACC	Advanced Concepts Committee (MIT LL)
CAES	Center for Advanced Engineering Study
ChE	Department of Chemical Engineering
ChemE	Department of Chemical Engineering
CICS	Center for Integrated Circuits and Systems
CIPS	Center for Integrated Photonic Systems
CMI	Cambridge-MIT Institute
CMSE	Center for Materials Science and Engineering
CSR	Center for Space Research
DMA	Dupont-MIT Alliance
EECS	Department of Electrical Engineering and Computer Science
HST	Health Sciences and Technology, Harvard-MIT
ICL	Integrated Circuits Laboratory
ISN	Institute for Soldier Nanotechnologies
ITRC	MIT/MTL Intelligent Transportation Research Center
LEES	Laboratory for Electromagnetic and Electronic Systems
LFM	Leaders for Manufacturing
MIG	Microsystems Industrial Group
MIT	Massachusetts Institute of Technology
MPC	Materials Processing Center
MSE	Department of Materials Science and Engineering
MTL	Microsystems Technology Laboratories
NSL	NanoStructures Laboratory
RLE	Research Laboratory of Electronics
SMA	Singapore – MIT Alliance
SML	Space Microstructures Laboratory
SOE	School of Engineering
TRL	Technology Research Laboratory
UROP	Undergraduate Research Opportunities Program

Private

AMD	Advanced Micro Devices
CSDL	Charles Stark Draper Laboratory
HP	Hewlett-Packard
IBM	International Business Machines Corporation
KIMM	Korea Institute of Machinery and Materials
MARCO	Microelectronics Advanced Research Corporation
C2S2	Center for Circuits and Systems Solutions
GSRC	Gigascale Systems Research Center
IFC	Interconnect Focus Center
MSD	Center for Materials, Structures and Devices
MGH	Massachusetts General Hospital
NTT	Nippon Telephone and Telegraph
SIA	Semiconductor Industry Association
SRC	Semiconductor Research Corporation
TI	Texas Instruments

Government

AFOSR	U.S. Air Force Office of Scientific Research
ARDA	Advanced Research and Development Activity
ARO	U.S. Army Research Office
AXAF	Advanced X-ray Astrophysics Facility - (NASA)
CSE	Consortium on Superconducting Electronic
DARPA	Defense Advanced Research Projects Agency
DOD	Department of Defense
DOE	Department of Energy
DURINT	Defense University Initiative on Nanotechnology
JPL	Jet Propulsion Laboratories
JSEP	Joint Services Electronics Program
LANL	Los Alamos National Laboratory
MDA	Missile Defense Agency
MRSEC	Materials Research Science and Engineering Center
MURI	Multi University Research Initiative
NASA	National Aeronautics and Space Administration
NCI	National Cancer Institute
NCIPT	National Center for Integrated Photonics Technology
NDSEG	National Defense Science and Engineering Graduate
NHLBI	National Heart, Lung, and Blood Institute
NIH	National Institutes of Health
NIST	National Institute of Standards and Technology
NOAA	National Atmospheric and Oceanographic Administration
NREL	National Renewable Energy Laboratory
NRL	Naval Research Laboratory
NSA	National Security Administration
NSF	National Science Foundation
ONR	Office of Naval Research

Other

CFI	CAD Framework Initiative
CIM	Computer Integrated Manufacturing
IEEE	Institute of Electrical and Electronics Engineers
IEDM	International Electronic Devices Meeting
HARC	Houston Advanced Research Center
MCNC	Microelectronics Center of North Carolina
MRS	Materials Research Society
NATO	North Atlantic Treaty Organization
NTCIP	National Transportation Communications for intelligent Transportation
STW	Dutch Technology Foundation
UCLA	University of California at Los Angeles
ULSI	Ultra Large Scale Integration
VLSI	Very Large Scale Integration

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