Opposite page:

A schematic of the MIT 3D photonic crystal.

Courtesy of M. Qi, J.Joannopoulos and H. I. Smith

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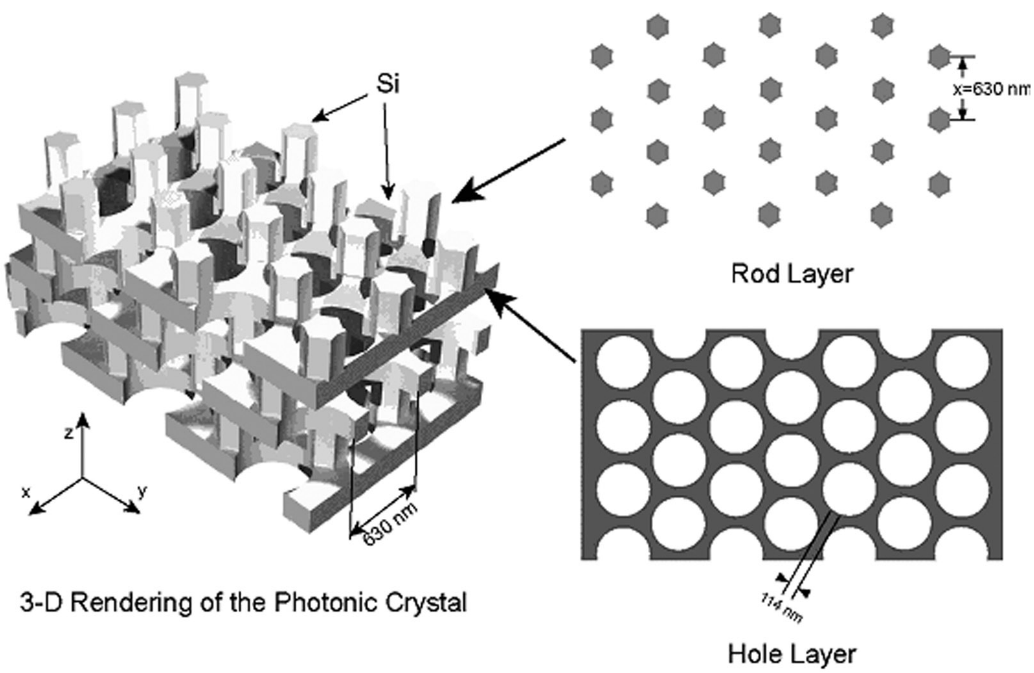
Optoelectronics



Optoelectronics

- *Fabrication of H-tree Waveguide Structures for Optical Clock Signal Distribution*
- *Erbium-Doped Waveguide Amplifiers*
- *Silicon Photonic Band Gap, Microcavity and Waveguide Structures*
- *Silicon Waveguide Structures*
- *Planarization of Processed Si IC Wafers for Planar Optical Waveguide Formation*
- *Waveguide Materials for Microphotonics*
- *Strain-tunable Photonic Band Gap Microcavity Waveguides at 1.55 μm*
- *Enhanced Extraction from a Light-Emitting Diode Modified by a Photonic Crystal and Lasing Action*
- *Fabrication of 3-D Photonic Bandgap Structures*
- *Guiding Light Through Sharp Bends Using Two Dimensional Photonic Crystals*
- *GaAs Superprism Using Two-Dimensional Photonic Crystals for Enhanced Beam Steering*
- *Application of RM^3 Integration to Optical Clock Distribution on Si-CMOS*
- *Aligned Pillar Bonding Technology for RM^3 Integration*
- *Optimization of Cells for Microscale Themophotovoltaic Energy Conversion*
- *Recess Mounting with Monolithic Metallization (RM^3) Polylithic Integration Technology*
- *Magnetically-Assisted Statistical Assembly*
- *Large Scale Oxidation of AlAs Layers for Broadband Saturable Bragg Reflectors*
- *Variable Amplitude Optical Fourier Filtering Using Controlled Thickness Metal Structures*
- *Towards Optical Logic*
- *Design and Variation Analysis of an On-Chip Optical Clock Receiver Circuit*
- *Optical Nano-Electromechanics*
- *Optoelectronic Integrated Circuits for Diffuse Optical Tomography*
- *Investigation of Dark Line Defects in Semiconductor Laser Diodes*
- *Compact Optoelectronic Neural Co-processor Project*
- *Terahertz Quantum Cascade Lasers*
- *Development of Bipolar Cascade Lasers*
- *Design and Fabrication of a Superprism Using Two Dimensional Photonic Crystals*
- *Coupling into Photonic Crystal Waveguides*
- *Development of Birefringence-Free Ridge Waveguides for Waveguide Isolators*

Fabrication of H-tree Waveguide Structures for Optical Clock Signal Distribution

Personnel

D. Ahn, J. Michel, K.Wada, and L. C. Kimerling

Sponsorship

MARCO/DARPA Focused Research Center on Interconnect

Electrical interconnects are the current platform for clock signal distribution across a chip, which governs the internal operations of a microprocessor in a synchronous chip design. However, the continuous enhancement of electrical clocking speed is expected to face severe limitations in the near future. Electrical clocking will have difficulties arising from jitter and skew of the signal and increased power consumption, as the clocking frequency is increased.

A solution to overcome this barrier is optical clock signal distribution. Using photons instead of electrons can help reduce skew and jitter of clocking and therefore enables the increase of the clock signal frequency well above 10 GHz, while keeping the power consumption and heat generation low. We fabricated waveguides for H-tree structures that split and distribute the source optical signal across the chip, while keeping the waveguide interconnect length identical.

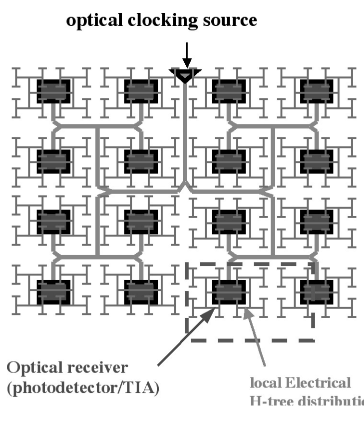


Fig. 1: Schematic of optical clocking and H-tree waveguide structure

We used SiO_xN_y and SiO_2 as waveguide core and cladding material, respectively. SiO_xN_y has the benefit of good compatibility with Si CMOS processing and gives the flexibility to adjust the refractive index within the range of 1.45-2.0 by changing the composition ratio of nitrogen and oxygen. Using 850nm wavelength and designing waveguide dimensions such that it retains only one single optical mode, we fabricated 1x4, 1x16, and 1x 64 fan-out H-tree structures. They have bending radii of 800μm, 250μm, and 120μm, respectively. All waveguides successfully distributed optical signals to each leaf node passing through all splitting and bending stages. Optical loss in the waveguide was measured to be about 2dB/cm.

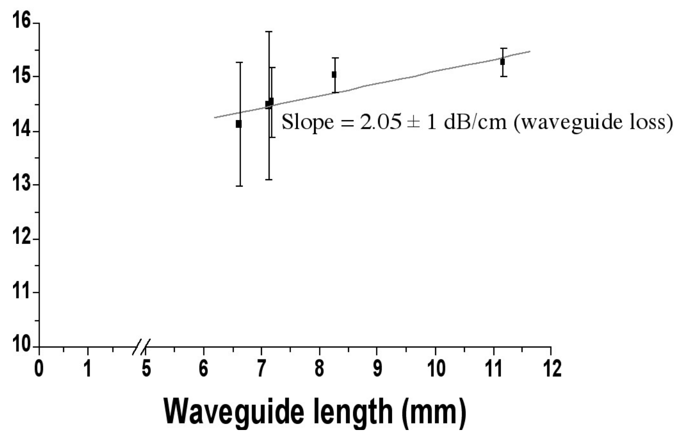


Fig. 2: Waveguide loss for 1.5µm 1.5µm PECVD-deposited SiON waveguide (Δn=0.05, unannealed)

One of the key requirements is equal power distribution at the 3 dB splitters. Conventional Y-splitters can exhibit high losses at the split fork due to limitations in lithography. These splitters are therefore susceptible to unequal splitting of the optical energy. By developing a new splitter design, we significantly reduced splitter loss and achieved more even splitting of optical energy.

Erbium-Doped Waveguide Amplifiers

Personnel

S. Saini, X. Duan, and J. Michel (L. C. Kimerling)

Sponsorship

CMSE and NSF

Erbium ion-based optical amplification has been a technological enabler in the establishment of long distance telecommunication at λ=1.55 μm wavelength light. The current evolution of telecommunication systems is to higher information capacity (by means of wavelength-division multiplexing) and to lower cost planar waveguide components (creating a new economy-of-scale technology). To meet both these demands, our research is focused on meeting two key amplification goals, using the broadband Er atom in glass hosts: (i) to take advantage of index scaling effects to reduce the required optical pump power for gain amplification, and (ii) to dope the highest possible concentration of optically active Er within a waveguide amplifier. These two goals are synthesized into a critical performance figure of merit, called the device gain efficiency.

Figure 3 is a theoretically computed plot summarizing our studies of goal (i): the effect of waveguide core-cladding index difference Δn on amplifier gain. Traditional Er-doped fiber amplifiers operate at index differences of Δn=0.05; design of a waveguide amplifier with Δn=1.0 results in an 80× increase of device gain efficiency. This means 80× less pump power shall be required for the Δn=1.0 waveguide amplifier, to achieve the same gain per unit length, as the fiber amplifier.

This stunning performance scaling advantage occurs because for different Δn waveguides, core dimensions just below single mode cut-off result in 64% of the λ=1.55 μm light being confined to the Er-doped core. From a confinement perspective, the two waveguides are morphologically equivalent for both pump and signal wavelengths. But for the higher Δn single mode cut-off waveguide, this confinement of the waveguiding modal fraction is within a smaller core cross-section. As a result, the optical flux rate (photons/cm^2) increases, and Er atoms within the core are pumped at a higher excitation rate.

Figure 4 is an experimentally acquired plot summarizing our studies of goal (ii): the exploration of new Er-based materials systems that yield ultra-high concentrations of optically active Er atoms. To evaluate the ultimate high-concentration candidate, we performed PhotoLuminescence (PL) studies on erbium oxide Er_2O_3, a ceramic-class material with ~10^{22} Er/cm^3 density. Studies from room temperature down to 4.2 K were done in order to isolate the effect of phonon-assisted non-radiative de-excitation. A factor of 60× drop in PL peak was observed from 4.2 K up to room temperature. In addition, the spectra shape was observed to profoundly change between 4.2 K and 20 K, indicating the presence of competing light-emitting Er optical centers, whose emission is intimately related to non-radiative processes. Comparison of integrated 4.2 K PL and room temperature absorption intensities of this sample, versus a standard Er-doped SiO_2 glass sample, allowed us to conclude that the 4.2 K main PL peak is associated with a minority volume phase, making up ~3% of the ceramic. Correlation with X-ray diffraction and Transmission Electron Microscopy has helped identify this minority phase to be a metastable FCC phase. If this phase can be made into the majority phase, gain coefficients 10× better than the best current fiber amplifier may be realized, for nearly the same device gain efficiency. Studies are underway to increase volumetric yield of this FCC phase.

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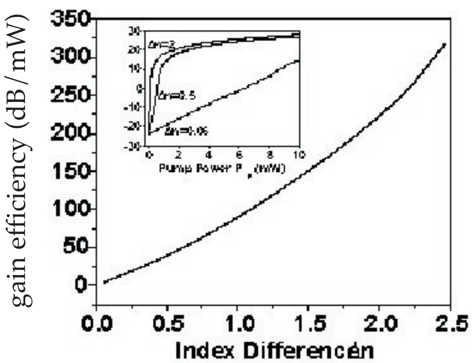

Fig. 3: Device gain efficiency versus index difference Δn *for a 1 m long waveguide amplifier with* 10^{20} *Er/cm*^{3} *optically active. Inset: plot of device gain* γ_d *vs. optical pump power* P_p *shows an increasing slope with higher* Δn*. The slope of this plot gives the device gain efficiency.*

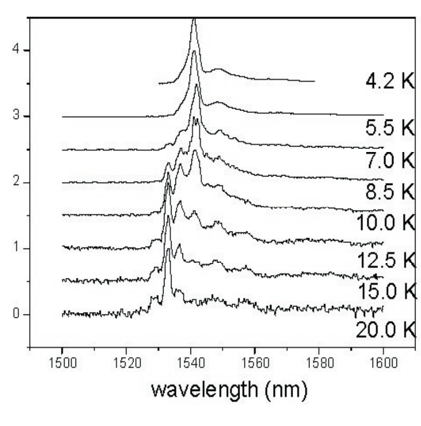

Fig. 4: Low temperature photoluminescence study of Er_2O_3*. Observations indicate the presence of three optical light-emitting centers, correlated by X-ray diffraction with the formation of three crystal phases.*

Silicon Photonic Band Gap, Microcavity and Waveguide Structures

Personnel

Y. Yi, S. Saini, M. Lipson, X. Duan, and K. Wada
(L. C. Kimerling)

Sponsorship

NSF and MRSEC

Tunable photonic crystals are key devices for microphotonics, especially for future WDM applications. Since the first introduction of Photonic Band Gap structures (PBG), also known as photonic crystals, new concepts and designs are being proposed, which could be building blocks for next generation photonic integrated circuits. When defects are formed within PBG materials, localized state can be introduced where light is strongly confined around the defect. The confinement of light to small volumes on the order of a wavelength will lead to large reduction of photonic circuit size and numerous useful devices, especially for Si microphotonics. Realization of the tunability of the photonic crystal, which makes it an active component, will play a key role for switching, modulation and wavelength conversion. This project is in collaboration with Profs. Joannopoulos, Ippen, Haus, Kolodziejski, and Smith.

Here, we demonstrate a tunable one-dimensional photonic crystal with a large air defect in silicon based PBG materials. Multiple localized resonance modes are observed within the photonic band gap at 1.402 µm, 1.582 µm, 1.792µm and 2.072µm. The observed photonic band gap is from 1.19µm to 2.18µm, which has 1000nm bandwidth. The Free Spectral Range (FSR) is larger than 100nm. Employing an electrostatic force, low voltage tuning of the localized modes are achieved simultaneously around the two telecom wavelengths of 1.3 µm and 1.55 µm. At 10V, an almost 60 nm mode shift is achieved. This is the lowest as we know so far.

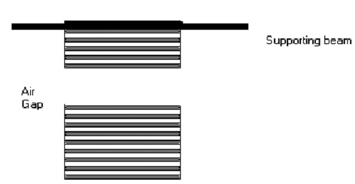

Fig. 5: The illustration of the one-dimensional photonic crystal with a large air defect.

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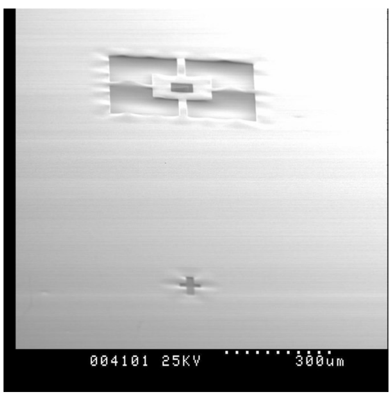

Fig. 6. SEM picture of the one-dimensional photonic crystal with a large air defect.

While fabrication of 3D photonic crystals by CMOS compatible process as is still challenging, the 1D omnidirectional PBG is easily incorporated into a CMOS process, while retaining important features of 3D PBG structures. Tunability can also be realized. Here we utilize the Micro-Electro-Mechanical-System (MEMS) method to realize low voltage tuning of the 1D PBG structure with large air defects. The top Si/SiO_2 mirror a membrane suspended by supporting beams over an airgap (cavity) and bottom mirror (see Figure 6). Applying a voltage between the membrane and substrate can tune the cavity thickness, i.e, can shift the multiple resonance modes within the PBG. Here, we emphasize that the low voltage can be used to tune a large wavelength. We concentrate on the windows from 1.2 μm to 1.7 μm. We plot the wavelength shift vs. voltage square in Figures 7 and 8 around 1.402 μm and 1.582 μm which are close to the two telecom wavelengths of 1.3 and 1.55 μm. The near-perfect linear relationship between the wavelength shift and voltage square confirms the electro-static tuning of the localized modes. We notice that, at 1.582 μm resonance, an almost 60 nm shift is realized with up to 10 volts. This is the lowest shift we have observed. Switching and modulation mechanism can be realized with such a shift.

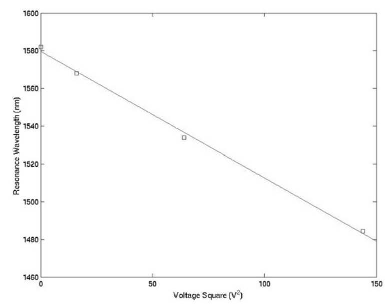

Fig. 7 The resonance wavelength shift with voltage square at 1.582μm.

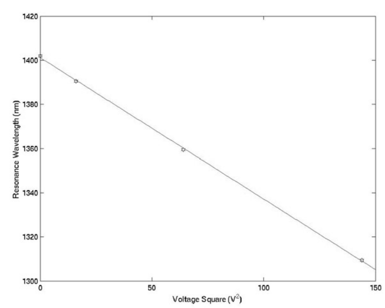

Fig. 8: The resonance wavelength shift with voltage square at 1.402μm.

Figures 7 and 8 indicate the possibility of continuous tuning from 1.3 to 1.5 μm by applying higher voltages, using flexible beams or a larger defect cavity. This is because the discrepancy between two tunable wavelength bands is only 60 nm. Figure 9 shows the first continuous tuning using a single defect in a microcavity in terms of electrostatic force. The voltage swing is up to 20 V, which covers a 1000 nm tuning range. This is the first demonstration of such wide range tuneability by a single filter.

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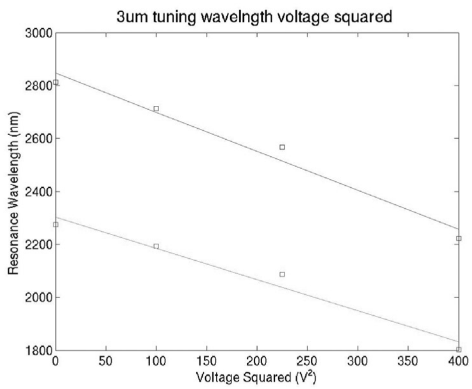

Fig. 9: First demonstration of an optical filter with a continuous tuning wavelength range of 2 μm.

This presented one-dimensional PBG filter with large air defect will be of importance in various applications other than data and telecom, such as solid state sensors of chemical substances.

Silicon Waveguide Structures

Personnel

D. Sparacin and K. Wada (L. C. Kimerling)

Sponsorship

NSF and MRSEC

The Si-SiO_2 materials system is an ideal platform for microphotonics because of the large index contrast between core and cladding, and the semiconductor characteristics of Si allowing carrier injection for ultra fast index change. Despite these attractive properties, the Si-SiO_2 system has a tradeoff associated with device processing: surface roughness. Waveguide surface roughness causes light scattering, resulting in transmission loss. This phenomenon scales with Δn^{2-3} and is crippling for high Δn photonic systems. Thus, surface roughness is a barrier for realizing silicon photonic devices.

Silicon On Insulator (SOI) wafers, with a 0.2 μm top Si layer and 1 μm SiO_2 layer, were patterned with a G-line (x=436nm) 10X stepper. RIE with SF_6 was used to etch the silicon waveguides, defined by photoresist, above the SiO_2. All samples were taken from the same wafer to ensure uniformity in the experiment. Dry oxidation of waveguide samples was performed for 30, 60, and 120 minutes at 1050ºC. Buffered Oxide Etch (BOE) was used to remove the oxide for roughness measurement.

A Digital Instruments NanoscopeIIIa Atomic Force Microscope (AFM) was used to measure the roughness of the waveguides. Measurement scans (3 X 3 μm^2) were performed parallel to the direction of the waveguides using the tapping mode. This was necessary for distinguishing between waveguide roughness and errors between adjacent scans. The problem seems to be provoked when measuring on a surface with a large slope, such as the sidewall of a waveguide. Another point to note is that unlike planar surfaces, which are scanned with the end of the AFM tip, the side of the tip is used when measuring sidewalls, diminishing the feature size resolution that can be obtained. The lessened resolution results in a smoothing of the surface in terms of amplitude height. Thus the values obtained in our measurements are understated. Roughness measurements were averaged over the entire waveguide

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sidewall area. Care was taken to measure all samples with the same tip orientation. TSUPREME4, a simulation program for CMOS design, was used to model the oxidation smoothing of the waveguides. In our simulation, an SOI substrate was created with a chosen surface roughness containing one frequency and amplitude. Trapezoidal cut outs in the silicon surface were used to simulate the roughness. This approximation only affects the short-term oxidation behavior, since the high surface energy corners of the trapezoids are oxidized fastest, leaving an ideal sinusoidal profile after only a few minutes of oxidation. The simulated roughness underwent dry oxidation at 1050ºC and roughness amplitude was recorded as a function of time.

Surface roughness, when created by dry etching processes, exhibits a distribution of spatial periods. In our study, roughness profiles obtained from AFM were processed using the Digital Instruments Nanoscope Software. The reduction of surface roughness is clear, when viewing the AFM images as oxidation time, increases. As seen in Figure 10, the as-fabricated waveguide surface contains mostly short period roughness, but as oxidation time is increased, the surface roughness period increases. This is expected since short period roughness is associated with a higher surface energy than long period roughness. Therefore, as oxidation time increases, the shorter period roughness is diminished more rapidly than the longer period roughness.

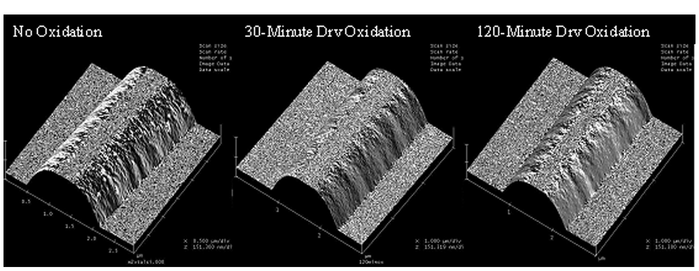

Fig. 10.: AFM images of silicon waveguides, the left image is as-fabricated whereas the center and right waveguides have undergone 30 and 120 minutes of dry oxidation and subsequent oxide etch respectively.

A quantitative measurement of this roughness is contained in Figure 11. There are three things to note about this plot. First, the roughness amplitude increases with period. The origin of this roughness distribution is thought to be associated with the grain size of the photoresist film under our baking conditions. Second, the shorter period roughness diminishes faster, relative to its respective initial amplitude, than the long period roughness. This is expected given our surface energy arguments stated earlier. Third, there appears to be "saturation" in the roughness profile. This is evident when comparing the 60-minute and 120-minute curves. Roughness saturation indicates that there is a practical limit in reducing propagation loss in Si waveguides. A waveguide designed for 1550 nm light is particularly sensitive to roughness periods around 125 nm ($\lambda/4n_{eff}$). TSUPREME4 simulations indicate that saturation should not occur, and roughness amplitude should continuously decrease to a perfectly smooth surface. While TSUPREME4 treats materials as a continuum of matter and neglects discrete atoms, this explanation does not contribute to why saturation occurs.

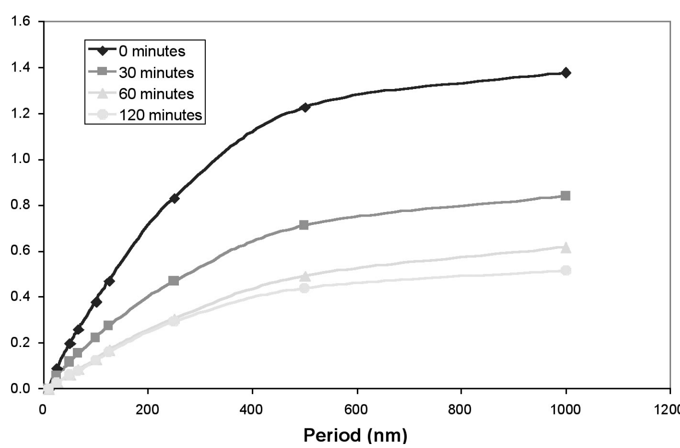

Fig. 11: Plot of waveguide roughness amplitude versus roughness period for different oxidation times.

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One explanation for the discrepancy between the observation and simulation is the error in comparing a surface roughness with a single amplitude and period to a distribution of amplitudes and periods. When a single roughness amplitude and frequency is simulated, the roughness period does not change. To see if this is always the case, a roughness with two sets of roughness was simulated. The shorter period of the bimodal roughness was given a smaller amplitude, to imitate the experimentally found roughness distribution. When the bimodal roughness distribution was simulated, the longer period roughness dominated and the shorter period roughness was absorbed as it was oxidized. The overall result, as seen in Figure 12, is a roughness with a smaller amplitude but longer period. This is an important kinetic phenomenon to note, for it lengthens the oxidation time needed to minimize the amplitude of a specific spatial period, such as the highly attenuating quarter wavelength period. This behavior can be likened to Oswald Ripening in grain growth, in which larger grains grow at the expense of smaller grains, but with respect to spatial period rather than grain size.

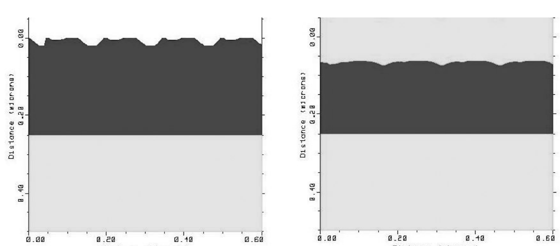

Fig. 12: Simulation images of a surface roughness profile, with a bimodal roughness distribution, before and after oxidation.

The bimodal simulation suggests that the roughness distribution in Figure 11 should shift to the right as oxidation time increases. This qualitatively explains the saturation, but cannot explain the presence of roughness near the origin after long oxidation times. A possible explanation for this is the nucleation of roughness by oxidation. The phenomenon of roughening by oxidizing {111} silicon has been observed by other studies. Likewise, the waveguide sidewalls in this study are very close to the {111}. Thus we suggest that oxidation of the {111} silicon waveguide sidewalls creates short period roughness that is absorbed by larger period roughness. This in turn feeds into the roughness distribution, eventually creating a "steady state" roughness distribution. In essence, there is a competition between roughness minimization and creation by oxidation of silicon waveguides. This "steady state" roughness distribution leads one to wonder whether there is a limit on propagation loss reduction of Si waveguides by oxidation. Further studies into oxidation smoothing kinetics are needed to better understand this.

In this study, we examined the oxidation kinetics of silicon waveguide roughness minimization. As anticipated we found that small period roughness is reduced faster than long period roughness. Unexpectedly, we also observed saturation in oxidation smoothing, which is problematic because it increases the needed oxidation time for minimizing roughness and prevents the possibility of atomically smooth silicon waveguides. We suggest that oxidation smoothing saturation is due to a competition between long period absorption of short period roughness and the nucleation of short period roughness by oxidation of the {111} silicon waveguide sidewall surface.

Planarization of Processed Si IC Wafers for Planar Optical Waveguide Formation

Personnel

E. Barkley (C. G. Fonstad, Jr.)

Sponsorship

Singapore-MIT Alliance

The integration of mixed materials and the corresponding material technologies has implied benefits for various applications from MEMs and sensors to optical communications and smart RF systems. Low temperature wafer bonding is an attractive technique that can be used to achieve the wafer-scale integration of various materials. The reduced temperatures allow for integration (bonding) with fully processed wafers, meaning that the well established separate base processes need not be altered. Our low temperature wafer bonding process starts with the deposition of several microns of PECVD oxide layer on both wafers. This layer is CMP'd (Chemical-Mechanically Polished), removing much of the deposited oxide layer and significantly increasing the planarity of the surface. This cycle is repeated until the required level of planarity is achieved. The wafers are then cleaned with the dual purpose of removing particles and achieveing surface activation to ensure a strong initial room termperature bond. The wafers are bonded at room temperature and are then annealed at higher temperatures to harden the bond. The upper temperature limit is set by the difference in thermal expansion coefficients for the two materials. In the case of wafer bonding in which one of the wafers is an SOI wafer, the SOI sustrate may be selsctively removed resulting in an increase in the annealing upper temperature limit for the thinned bonded wafer pair.

In past research we discovered that it was difficult to repeatedly achieve strong wafer bonds. We now attribute this uncertainty to the past inability to quantitatively measure and detect particles present on the wafer surface that were not removed by the cleaning step. Through a collaboration with Lincoln Labs, we have been studying and quantifying the effects of particle counts and surface microroughness on low temperature wafer bonding unsing 6" test wafers. We have been using a Tencor SurfScan particle counter to determine particle counts for our wafers at each step in the process (post-dep, post-CMP, post-clean). Although more testing is still required, we have found that particle counts can be significantly reduced by water-polishing the wafers post-CMP. The water polish step is basically just the CMP step repeated with DI water used in place of the CMP slurry. However, we have found that the water polishing step even when combined with a standard piranha clean is not sufficient to achieve repeatable strong bonds. We are currently seeking additional cleaning steps such as megasonic cleaning which has been shown to be successful by the 3D integration group at Lincoln Labs.

We have recently begun a study of the integration of waveguides on processed Si wafers, a topic we are well positioned to address because of our expertise in planarizing processed wafers for bonding. Our objective is to be able to add upper layer dielectric optical waveguide interconnect layers to a processed silicon wafer to complement the already existing metallic electrical interconnect layers formed in standard back-end processing. There is an extensive literature dealing with dielectric waveguides on silicon wafers, and significant attention has been paid to improving the waveguide deposition and definition processes in an attempt to minimize losses while achieving proper core and cladding dimensions and refractive index difference. However, almost all of this work has been done on silicon wafers without underlying devices and circuitry, and thus it does not address the issue of fabricating guides in a realistic environment. In particular, it does not deal with the issue of potential losses caused by the non-planarity of the wafer surface introduced by the metal layers in the back-end. The surface upon which the waveguide core is deposited must be flat enough to keep surface-normal scattering at some acceptable level. We are planning on studying how CMP be used to planarize the wafer surface prior to core deposition in an attempt to minimize scattering losses. This work will build directly on our work planarizing processed wafers for bonding.

Waveguide Materials for Microphotonics

Personnel

S. Akiyama, J. Sandland, M. Stolfi, V. Nguyen, A. Eshed, M. Navi Marenzi, X. Duan, K. Wada, and J. Michel (L. C. Kimerling)

Sponsorship

MARCO/DARPA Focused Research Center on Interconnect, Pirelli Labs, Draper Labs, and CMSE

Silicon Oxynitride Film for Optoelectronic Applications

The Silicon Oxynitride (SiON) materials system provides a very flexible system for producing waveguides.

Silicon oxynitride films can be produced with refractive indices ranging from that of silicon dioxide (1.46) to that of silicon nitride (2.0). This wide index range allows a great deal of flexibility in index contrast while remaining in the silicon oxynitride materials system.

However, current deposition methods, such as PECVD, have significant limitations. Hydrogen incorporation during processing causes substantial absorption in the 1550 nm wavelength window. Additionally, high post-annealing stresses often lead to film cracking and delamination. These film quality issues limit the useable range of silicon oxynitride indices.

This study focuses on the materials properties of low-hydrogen, moderate stress silicon oxynitride films created by reactive rf magnetron sputtering. SiON films are sputtered from a silicon nitride target in an oxygen ambient to produce films with indices ranging from 1.55 to 1.89. The refractive index tunes linearly with gas flow rate, making the refractive index easy to tune. Wavelength dispersive spectroscopy shows these films have a good match with an SiO_2/Si_3N_4 alloy (Figure 13). SIMS (Figure 14) shows the good depth uniformity of the films, and TEM (Figure 14) demonstrates that the films are homogeneous. Preliminary waveguide measurements of sputtered n=2.29 silicon nitride on silica show losses of less than 10dB/cm.

Air Trench Waveguides

Silica Optical Bench (SiOB) technology is mature and widely used in integrated WDM applications, such as Arrayed Waveguide Gratings (AWGs). The low-index-

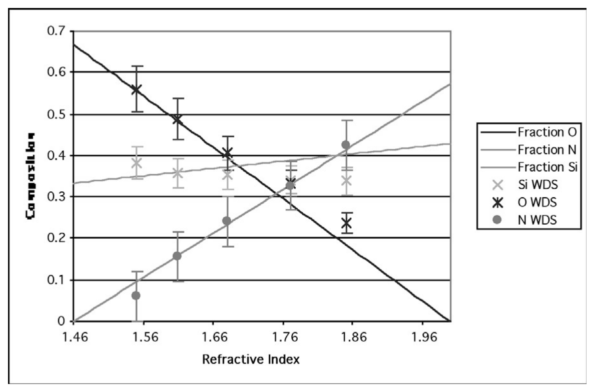

Fig. 13: Data points show atomic fraction as determined by WDS. Solid lines are predictions based on a silica/silicon nitride alloy.

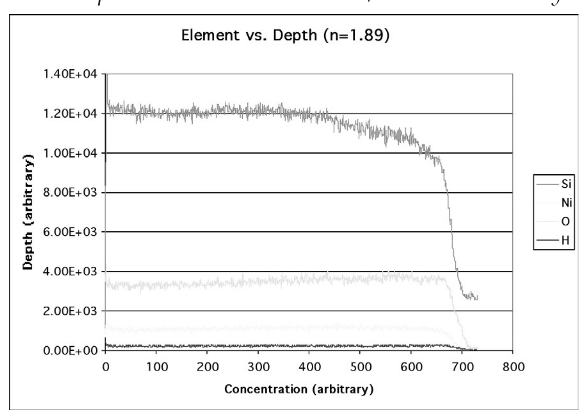

Fig. 14: SIMS profile of silicon, oxygen and nitrogen through the depth of a n=1.89 silicon oxynitride film.

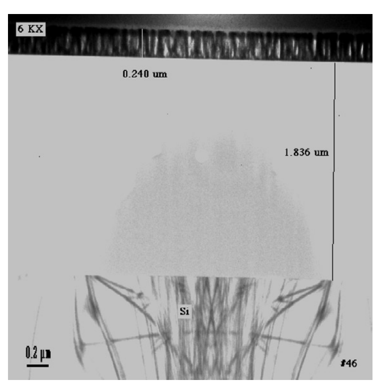

Fig. 15: TEM micrograph of n=1.89 silicon oxynitride film.

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contrast waveguides permit low insertion loss at fiber coupling and low propagation loss. However, a major drawback is the large bending radius to keep radiation losses within acceptable range, limiting the density of integration. We proposed a simple, CMOS compatible technology that allows sharp bends in silica, therefore increasing the density of integration by orders of magnitude (Figure16). Air trench waveguides realize compact bending radii by introducing air or low index materials at the bends and hence locally increasing the index contrast. This air trench waveguide realizes high optical integration on chip using a low index contrast materials system. Therefore, this waveguide has excellent characteristics for future microphotonics applications such as low transmission loss, low bending loss, low coupling loss between fiber and waveguide in addition to small, compact bends. Simulations were done using the Finite Difference Time Domain (FDTD) method, primarily in two dimensions. These simulations show that a waveguide bend, designed to have a throughput efficiency of 98%, can be reduced in size by a factor of 10-100 with the use of air trenches. The bending radius decreases 30-500 times. For the fabrication, we employed Silicon Oxynitride (SiON) for the core and SiO_2 for the cladding. The fundamental processes such as the optimization of SiON deposition and successive defect removal annealing process, film stress management, and a precise deep oxide etch process were established.

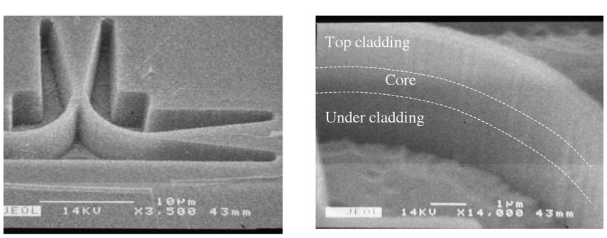

Fig.16: SEM images of an air trench T-splitter (x3,500) and an air trench waveguide(x14,000)

Strain-tunable Photonic Band Gap Microcavity Waveguides at 1.55 μm

Personnel

C. W. Wong, M. Qi, P. Rakich, S. G. Johnson, and Y.-B. Jeon (G. Barbastathis, S.-G. Kim, H. Smith)

Sponsorship

MIT Microphotonics Center

Concept and Key Idea

Photonic-bandgap microcavities in optical waveguides have demonstrated cavity resonances at wavelengths near 1.55 μm band, quality factors on the order of 300, and modal volume at 0.055 μm^3 in high-index contrast Si/SiO_2 waveguides and GaAs air-bridge waveguides. Applications include zero-threshold microlasers, filters and signal routers. For tunability in Si microphotonic platforms, thermal actuation is often utilized. Compared to thermo-optics, the novel strain-tuning via thin-film piezoelectric micro-actuators provides a significantly faster response, lower power consumption and better localization of tunability. This level of integration would permit dynamic reconfiguration of the cavity resonance and band-edges, fine-tuning for fabrication mismatches, and active compensation of device arrays to external disturbances. We have designed and fabricated the first tunable photonic-bandgap microcavities in optical waveguides, with the strain modulation via thin-film piezoelectric actuators on deformable membranes. Cavity resonance tunability, with sub-nanometer lattice control, is designed through perturbation on FDTD computations. Device fabrication integrates X-ray nanolithography, piezoelectric micro-actuators and bulk micromachining.

Device Design

The conceptual design is illustrated in Figure 17. The Si microcavity waveguide is located on a deformable double-anchored SiO_2/Si membrane. The thin-film piezoelectric actuators provide sufficient driving force, under 5V actuation, for the sub-nanometer strain control of the geometric lattice in the microcavity. Comparative designs of the double-anchored membrane have been demonstrated for analog tunable diffractive gratings. Experimental effects of static strain on coupled vertical microcavity resonators and theoretical designs for shear-modulated 2D photonic crystals on bulk piezoelectric substrates have also been reported.

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continued

We employ first-order perturbation theory to obtain a semi-analytical result for the strain-induced shift in the cavity resonance; such methods ease the study of small modulations such as the 0.3% strain considered here. First, a closed-form solution for the hole boundary displacements is derived following classical mechanics. The material boundary displacements are then numerically meshed and employed in a perturbation-theory formulation, which involves surface integrals of the unperturbed fields (obtained by FDTD simulation) over the perturbed material boundaries. The result predicts a 0.8% shift in resonant wavelength (12.7 nm in the C-band) for a 0.3% mechanical strain from a 3D computation. This is illustrated in Figure 18a. While a 2D computation suggests similar final results in the resonant shift, the 3D computation highlights differences from the individual contributions – hole ellipticity, defect cavity length, and hole diameters – in the strain perturbation. Other effects such as photoelasticity and waveguide out-of-plane bending were found to be secondary.

Fabrication and Results

For resonance wavelength at 1.55 μm, the minimum feature size, located between the waveguide edges and the hole edges, is 130 nm. X-ray lithography is employed with a Cu_L source at 1.3 nm to transfer the pattern from the mask to a PMMA resist. The mask is a thin SiN_x membrane with 200 nm Au patterned with e-beam lithography. The resist image is then transferred to 50 nm of Cr, via lift-off, and etched into a 212 nm single-crystal Si layer to form our waveguide. The microfabricated piezoelectric film has an excellent dielectric constant of 1200 and a d_{31} coefficient of ~ -100 pC/N. A fiber lens assembly is used to couple a 1.430 μm to 1.610 μm tunable laser diode source, with TE polarization and lock-in amplification, into the prepared input/output waveguide facets. For a static microcavity waveguide, resonance is detected at 1555.4 nm with a Q of 159, as shown in Figure 18b. Experimental measurements of the tunable cavity resonance, band-edges and other cavity responses are currently underway.

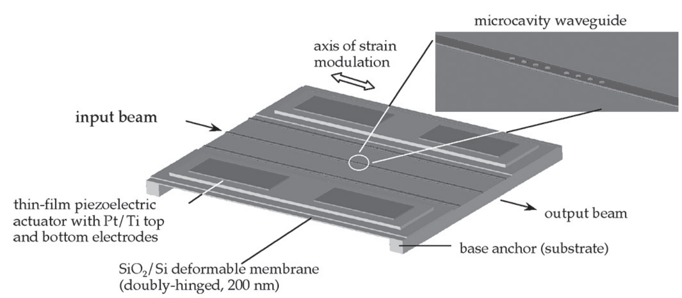
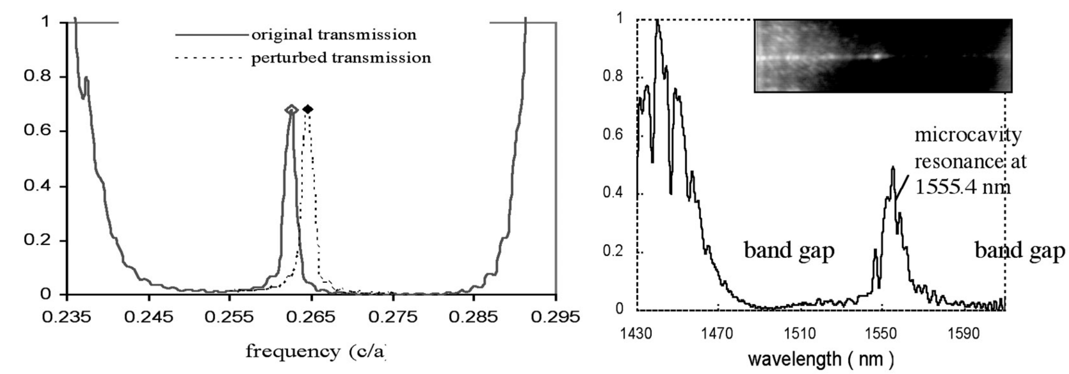


Fig. 17: Device schematic of the tunable photonic-bandgap micro cavity waveguide , with strain modulation via thin-film piezoelectric actuators on the deformable membrane.



(a) (b)

Fig. 18: (a) Computed transmission shift through perturbation theory in the photonic band gap; (b) Measured static microcavity resonance with Q of 159. Inset; top view of microcavity waveguide in transmission.

Enhanced Extraction from a Light-Emitting Diode Modified by a Photonic Crystal and Lasing Action

Personnel

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(E. P. Ippen, J. D. Joannopoulos, L. A. Kolodziejski, and H. I. Smith)

Sponsorship

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Semiconductor LEDs have the potential to be low-cost and long-lifetime solid-state lighting sources for applications as varied as room lighting and flat-panel displays. LEDs are also used in short-range telecommunication systems and may be desirable for optical interconnects in computers. Unfortunately, most of the light emitted from a semiconductor LED is lost due to total internal reflection resulting in low extraction efficiency.

In this work, the effect of a Two-Dimensional (2D) Photonic Crystal (PC) on the emission properties of a Quantum Well (QW) inside an LED is examined. Enhanced extraction of light into the vertical direction is obtained and attributed to the presence of leaky resonant states created by the coherent scattering from the periodicity of the PC. Scattering along the high-symmetry directions also provides sufficient distributed feedback for lasing to occur. The 2D PC is fabricated in the top cladding layer of an asymmetric active region that emits at $\lambda = 980$ nm with a full-width at half-maximum of approximately 60 nm at room temperature. The PhotoLuminescence (PL) emission at 935 nm, normal to the surface, is enhanced by a factor of 100, and the spectrally integrated PL is enhanced by a factor of 8, both when compared to a reference structure without a PC. When optically pumped above threshold, lasing occurs at a wavelength of 1005 nm. This work provides a basis for the design of high efficiency LEDs and lasers based on 2D PCs.

The 2D PC is a 30 x 30 μm triangular lattice of holes etched within the upper InGaP cladding layer of a 50 μm mesa, as illustrated in Figure 19. To minimize carrier recombination at the etched surfaces, the holes do not penetrate the InGaAs QW; however, the hole depth is sufficient to cause enhanced extraction of light and laser feedback. The device structure is grown using gas-source molecular beam epitaxy. The separation layer is initially grown as $Al_{.98}Ga_{.02}As$ and the DBR consists of AlAs and GaAs layers. A SiO_2 layer is deposited on the grown structure using plasma enhanced chemical vapor deposition. The holes are defined in PMMA by direct-write electron-beam

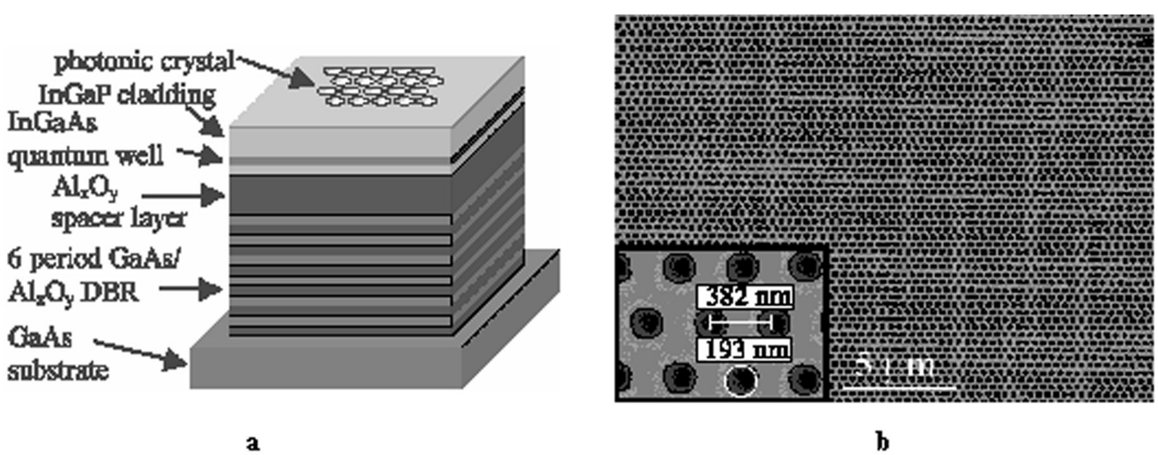


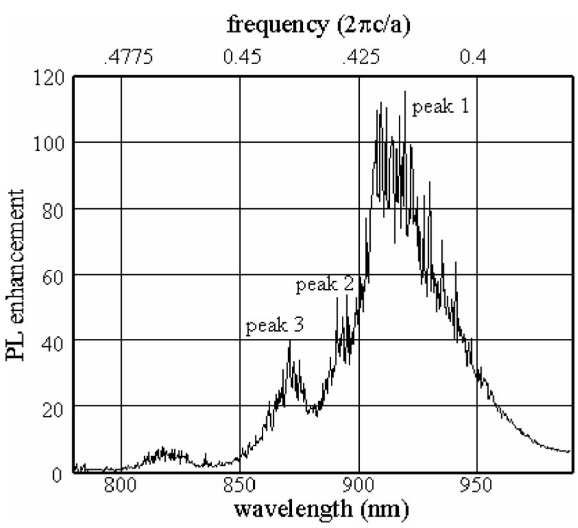
Fig. 19: a) The 2D PC structure. b) Scanning electron micrographs of PC structure.

continued

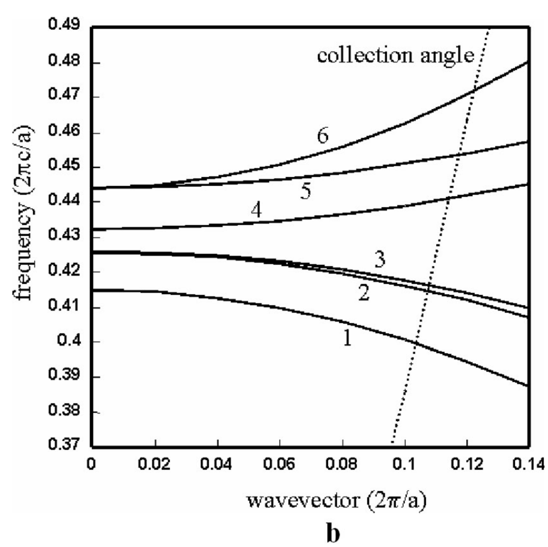
lithography. The electron beam writes a square pattern in the PMMA to represent each hole. The beam size, however, is larger than the step size for translating the electron beam. This leads to the desired circular pattern following development.

The PMMA is used as a mask in transferring the hexagonal pattern to the SiO_2 layer using RIE. This is accomplished by RIE with a CHF_3 plasma using 15 second steps in between 1 minute cool-down steps. The purpose of the cool-down step is to prevent flowing of the PMMA mask. The SiO_2 mask is subsequently used in the RIE of the holes into the upper InGaP cladding layer using RIE with a $CH_4/H_2/O_2$ plasma in a 20:20: 2.5 gas flow ratio. The mesas are next defined using photolithography followed by RIE with the $CH_4/H_2/O_2$ plasma to penetrate the active region. RIE with a BCl_3 plasma is used to expose the mesa sidewalls. The final step in the device fabrication is the wet thermal oxidation of the $Al_{.98}Ga_{.02}As$ separation layer and the AlAs DBR layers. Figure 19b shows scanning electron micrographs of a PC structure with lattice constant, a, of 382 nm, hole diameter of 193 nm, hole depth of 101 nm, and an active region thickness of 198 nm. This structure is characterized and the results are reported below.

The photoluminescence is observed using a cw Ti: Al_2O_3 laser with an emission wavelength of 785 nm. Figure 20(a) shows a spectrum of the enhancement of PL from the PC region normalized to the same structure but without a PC. Figure 20(b) is a calculation of the photonic band structure near the G point in the first Brillouin zone. The bands represent leaky resonant states that provide a pathway for the enhancement of light extraction. On the long wavelength end of the spectrum, the range covered by the first three bands closely matches the large observed peak centered near 935 nm. The width of the peak is determined by the



a



b

Fig. 20: a) PL enhancement spectrum from PC structure. b) Calculated hotonic band structure near G point.

continued

Q of the leaky resonance and by the collection angle (dotted line). Band 4 and bands 5 and 6 closely match the peaks near 890 nm and 860 nm respectively. The dip between peaks 2 and 3 corresponds well with the gap in available states between bands 3 and 4.

Lasing occurs at a wavelength of 1005 nm as the pump power is increased (Figure 21(a)). The lasing peak occurs from distributed feedback and corresponds well with the bending of bands at the M point (Figure 21(b)).

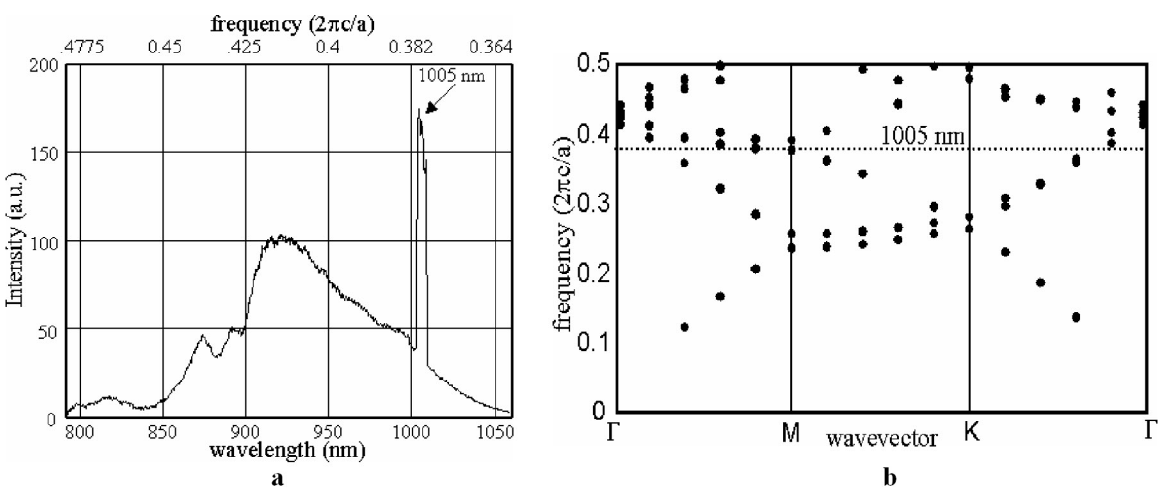


Fig. 21: a) Lasing spectrum. b) Calculated band structure showing band folding near M point.

Fabrication of 3-D Photonic Bandgap Structures

Personnel

M. Qi, J. Joannopoulos and H. I. Smith

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Three-Dimensional (3D) Photonic BandGap (PBG) Structures offer opportunities for miniaturizing a variety of conventional optical devices. The structure under investigation consists of a stack of alternating "hole" layers and "rod" layers, which themselves are 2D PBG structures (Figure 22). Consequently, result most results in 2D structures can be ported to the 3D design with minimal modification. Compared to other 3D structures in the literature, this design has the unique advantage that each layer is highly symmetric so that optical devices, such as cavities and waveguides can be realized by modifying only one layer. From the fabrication point of view, the rod layer is a byproduct of etching holes into the previous hole layer, which effectively cut the fabrication steps by one half.

The structure has been fabricated in a layer-by-layer approach using e-beam lithography and spin-on-dielectrics planarization. E-beam lithography has the advantages that it allows design flexibility, controlled introduction of defects and robust overlay alignment. Figure 23 shows the SEM micrographs of the final structure. Seven functional layers can be seen clearly.

With the success of the pilot process, two efforts are ongoing simultaneously. One is to fine-tune the structure and process, and the other is to demonstrate the capability of large area, low-cost fabrication of 3D PBG structures. The structure shown in Figure 22 is suboptimal because the effective radius of the rod layer is dependent on the hole size. The bandgap can increase from 21% (measured as a percentage of the midgap frequency) to 27.3% if the shape and size of the rods can be varied (in this case reduced) independently from those of the holes. However this will require that the rod layer being fabricated in a separate step. A balance can be found by changing the shapes of the holes as shown in Figure 24(a). In this way the rod

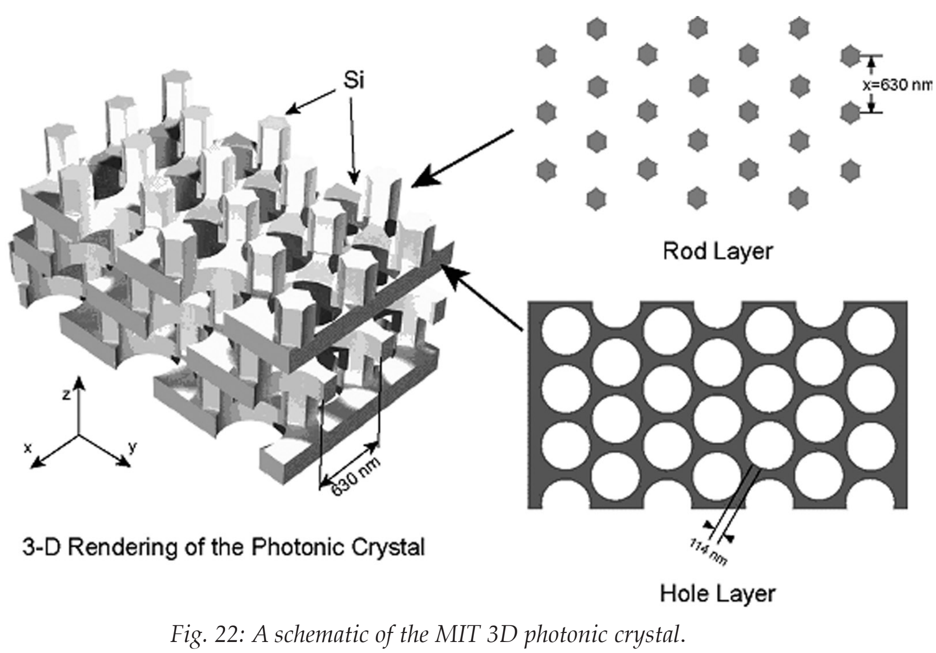

Fig. 22: A schematic of the MIT 3D photonic crystal.

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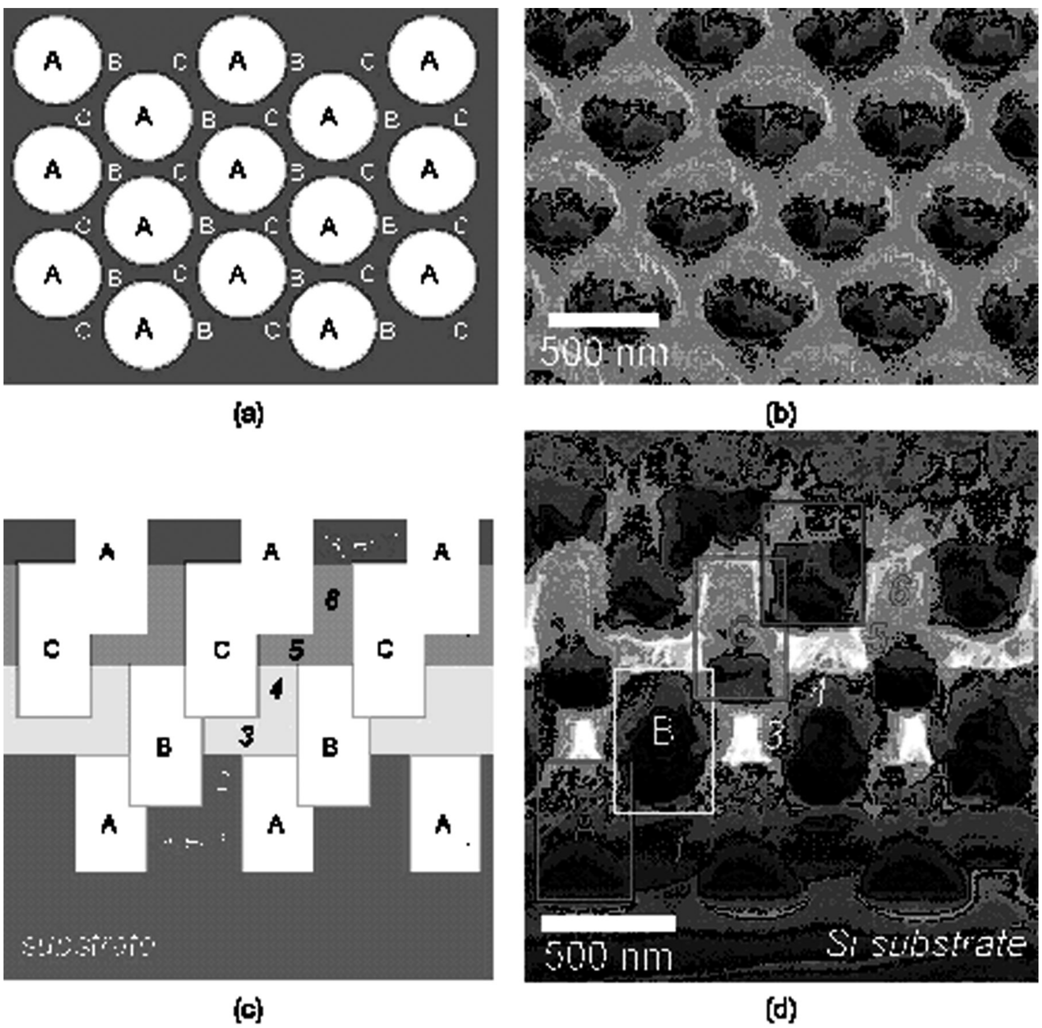

Fig. 23: (a) Schematic of the 3D photonic crystal viewed from the top, showing the hexagonal array of holes. The points marked "B" and "C" designate the centers of holes in layers beneath, as depicted in cross section in (c). (b) Scanning-electron micrograph of the seventh layer of the photonic crystal. The sixth layer can be seen through the holes. (c) Cross-sectional schematic of the photonic crystal. Different colors correspond to different process cycles. (d) A cross-sectional view of the 3D photonic crystal cleaved with a diesaw. The functional layers are marked by numbers, while the etched holes are outlined with rectangles.

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size will be reduced due to the extra semicircular holes at the six corners of the main holes. Meanwhile the change of the effective hole size is minimal because the holes are much larger than the rods. Simulation shows that a complete bandgap of 25% can be achieved, which is a 19% increase over the original 21% gap. The fabrication of such a structure will be no different than the pilot process since the e-beam lithography can pattern virtually any shapes. A larger bandgap is highly desirable because it displays the biggest optical effects, allows the widest bandwidth for optical devices, and most importantly, is robust in the presence of fabrication imperfections.

In order to realize real-world applications of 3D PBG structures, large area and spatial coherence are required. Interference lithography can easily pattern a hexagonal lattice of holes (or rods) by a double exposure with the second exposure rotated 60 degrees from the first. However, the holes obtained are elliptical. Such elliptical shape breaks the hexagonal symmetry of the lattice, and simulation shows that the bandgap will be reduced by a factor of two. Last year we proposed a set of new techniques which overcame such difficulty via a combination of interference lithography and tilted X-ray lithography. The method is ideally suited to low-cost, large-area 3D fabrication of periodic structures. This year we set up the equipment and demonstrated the synthesis of a hexagonal array of circular holes (Figure 25). The staging that we build for exposure is shown in Figure 26.

By combining this tilting technique and an overlay alignment technique, such as Interferometric Broad-Band Imaging (IBBI), it should be possible to fabricate large area 3D photonic crystal.

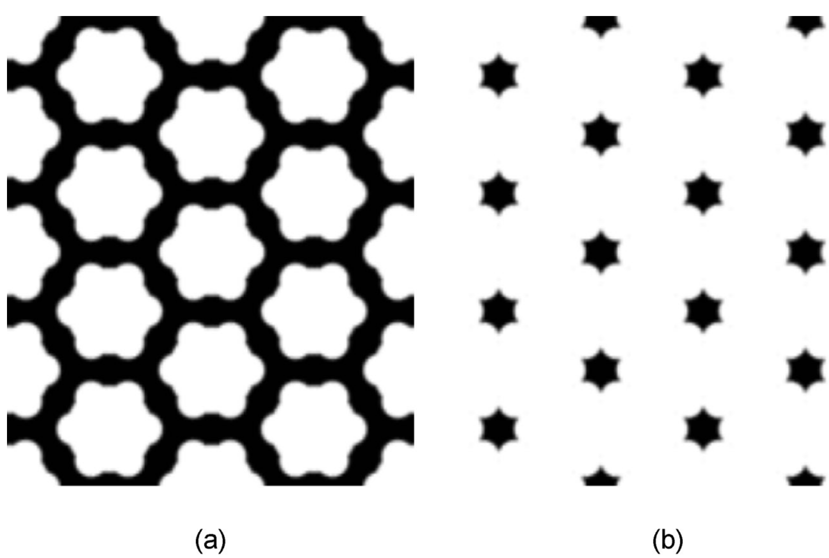

Fig. 24: Schematics of the improved 3D PBG design. (a) The "hole" layer. (b) The "rod" layer.

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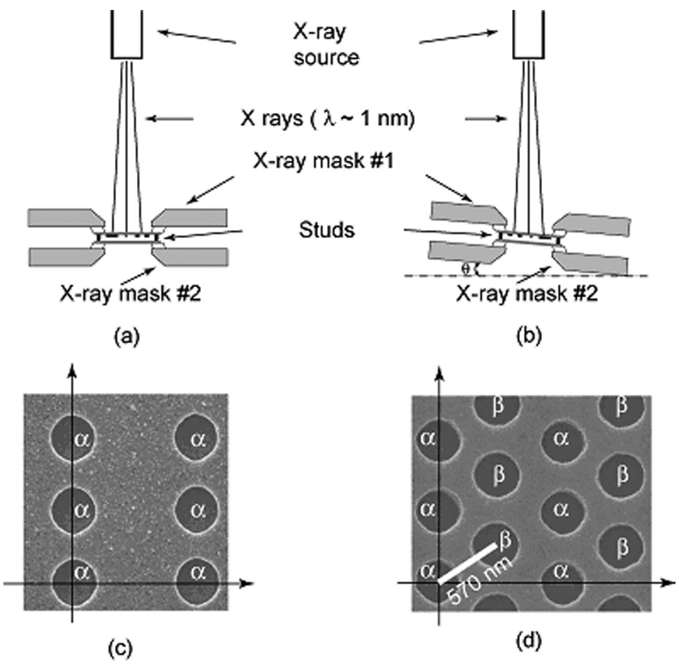

Fig. 25: Synthesizing a hexagonal lattice of circular holes with tilted X-ray exposure. (a) Schematic of proximity X-ray exposure. (b) After the first exposure, a second one is carried out with the mask-substrate assembly tilted with an angle q=G/V, where G is the gap between the mask and substrate and V is the image shift vector, in this case it is set to 570nm. (c) Pattern on X-ray mask #1. (d) Pattern on the substrate after the double exposure (in this case the substrate is a wafer).

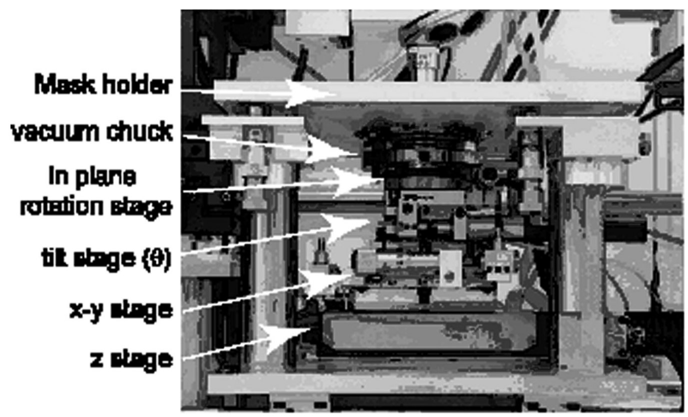

Fig. 26: Photograph of the stage for tilted X-ray exposure. The X-ray source, which is not shown, is above the mask holder.

Guiding Light Through Sharp Bends Using Two Dimensional Photonic Crystals

Personnel

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Large-scale photonic integrated circuits require guiding light around sharp bends with a radius of curvature on the order of a wavelength. In conventional index-guided waveguides, light is confined as a result of total internal reflection at the interface between the high refractive index waveguiding layer and its low index surroundings. However, bends in index-guided waveguides are susceptible to large optical losses as the radius of curvature decreases. Photonic Crystals (PCs), which consist of a periodic arrangement of high- and low-dielectric constant material, have been proposed as a potential solution in order to guide light around corners, including 90° bends, with near perfect transmission.

One such Two-Dimensional (2D) photonic crystal consists of an array of cylindrical rods of high dielectric material above a low dielectric material. Introducing a line defect, such as a row of smaller diameter cylinders into the 2D photonic crystal, results in a linear waveguide. The 2D periodic arrangement of dielectric rods, surrounding the line defect, contains a Photonic Band Gap (PBG), i.e. a range of frequencies in which light can not propagate. Thus, an optical signal with a frequency inside the PBG has its energy confined within the line defect and is evanescent within the photonic crystal. The diameter of the cylinders in the line defect remains large enough to provide index guiding in the third dimension (normal to the plane of periodicity). The localization of a mode inside the line defect can be utilized to guide light around sharp corners, including a 90° bend, with low optical loss.

Nevertheless, the practical use of photonic crystal waveguides is limited due to the poor coupling efficiency between the photonic crystal waveguide, and the conventional index-guided waveguide. Coupling poses a challenge because the photonic crystal waveguide exhibits a significantly different mode profile and propagation mechanism as compared to traditional waveguides that use index confinement. In the conventional waveguide, the field has only forward propagating components, while the field in the photonic crystal waveguide has both forward and backward propagating components due to scattering. Furthermore, guiding in the conventional waveguide is in the high index core that is surrounded by a low index material; in the photonic crystal waveguide, guiding is in a low effective index core that is surrounded by two photonic crystal mirrors.

Three different designs for coupling into the defect photonic crystal waveguide are being investigated. In the first design, the waveguide abruptly terminates prior to the photonic crystal region. This design suffers from Fabry-Perot reflection at the edges of the photonic crystal region, which makes the transmission of the waveguide dependent on the photonic crystal waveguide length. In the second design, the input and output ends of the index waveguides are tapered, which reduces the reflections. In the third design, the input waveguide is adiabatically converted into a strongly coupled cavity waveguide. This adiabatically transforms the forward propagating component of the field into both forward and backward propagating components before reaching the photonic crystal. Also, the photonic crystal cladding is introduced slowly from the edge, thereby, adiabatically transforming the mode from high-index guiding to gap guiding. 2D simulations show that this third coupling scheme results in almost 100% transmission through the photonic crystal waveguide.

The cylindrical rods of the photonic crystal consist of a high-index, 830nm thick epitaxial GaAs layer sandwiched between a 100nm thick SiO_2 cap layer and a 600nm thick low-index Al_xO_y layer. An additional 900nm thick Al_xO_y layer is below the cylindrical rods isolating the GaAs guiding layer from the GaAs substrate. The structures are fabricated using gas source

continued

molecular beam epitaxy, hard etch mask deposition, direct-write electron beam lithography, Ni lift-off, reactive ion etching, and AlAs oxidation. Figure 27 shows Scanning Electron Microscope (SEM) images of the three designs at various stages of fabrication. Figure 28 shows a side view of the bulk photonic crystal.

Currently, the photonic crystal devices are being tested. The band gap is being mapped first by varying the number of columns in a bulk photonic crystal. Also, the three coupling mechanisms are being compared by measuring the transmission through the photonic crystal waveguide.

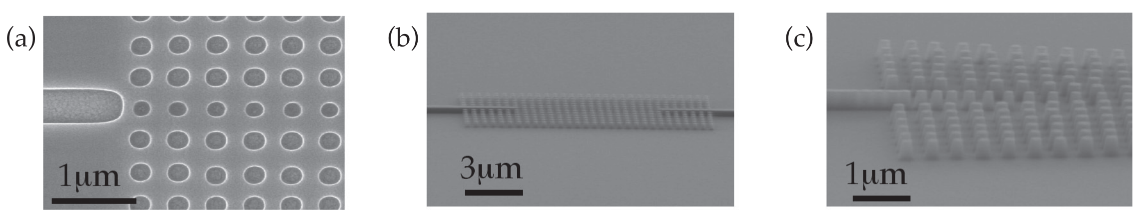

Fig. 27: Top view SEM image of (a) the first coupling design after electron-beam lithography, (b) the second coupling design after a hard mask etch, and (c) the third coupling design after a hard mask etch.

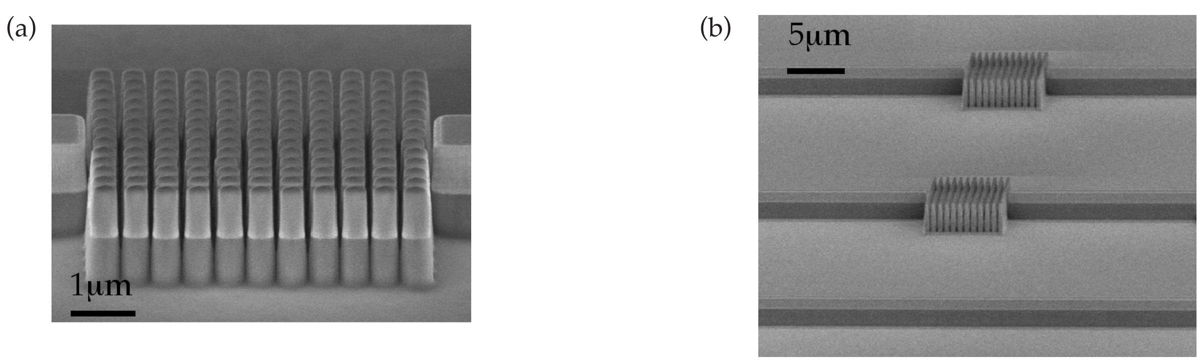

Fig. 28: (a) Side view SEM image of a bulk photonic crystal. The period is 500nm and the diameter of the pillars is 300nm. The input and output waveguides are 1.5μm wide. (b) Photonic crystal devices on a single chip. The design contains a straight waveguide for normalization purposes.

GaAs Superprism Using Two-Dimensional Photonic Crystals for Enhanced Beam Steering

Personnel

S. Tandon, C. Luo, M. Soljacic, M. E. Walsh, and G. S. Petrich
(H. I. Smith and L. A. Kolodziejski in collaboration with J. D. Joannopoulos)

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A superprism is an optical device similar to a conventional prism only with two enhanced properties: (1) super-dispersion; and (2) ultra-refraction. Just as a conventional prism separates light into multiple wavelengths, a superprism separates these wavelengths over wider angles--termed "super-dispersion." A superprism can also be used to magnify the angle of propagation of a single wavelength of light to steer the beam over a wide range of angles--termed "ultra-refraction." Photonic crystals form the essence of the superprism effect. Being able to realize these superprism effects would be very useful for a number of applications ranging from enhanced devices for Wavelength-Division-Multiplexed (WDM) systems to a new class of ultra-refractive optical elements for beam manipulation.

The device consists of a two-dimensional photonic crystal with a square lattice of cylindrical air holes in a high index material such as silicon or gallium arsenide. The device is hexagonal-shaped with the Photonic Crystal (PC) occupying a square region in the center. The initial design has focused on realizing ultra-refraction such that an input angular sweep of approximately +/- 2 degrees is amplified to about +/- 30 degrees at the output for a wavelength of 3.2 μm. A thick low index layer is used to minimize radiation loss into the high index substrate.

The feature sizes of the photonic crystal can be scaled depending on the wavelength of operation. The desired wavelengths of 3.1μm and 1.55μm imply lattice constants of 750nm and 372nm, and hole radii of 300nm and 150nm, respectively. The total thickness of the device (excluding the substrate) is about 3.5 microns (460nm GaAs, 3μm Al_xO_y) while the top surface will have an area of about 2 x 2cm.

The hexagonal device shape is patterned using photolithography; while the photonic crystal holes are patterned using interference lithography. Figure 29(a) shows a digital photograph of the patterned hard mask layers on a silicon substrate. Two hard mask layers have been used: 50nm chromium on top of 250nm HSQ (spin-on oxide). The chromium layer is patterned with the superprism hexagonal shape, while the open square area is patterned with the ~780nm period photonic crystal in HSQ. The diffraction pattern from the PC can be seen as the streak across the square area. Figure 29(b) shows a microscope image (100x magnification) of the corner region of the photonic crystal area. The unit cell of the PC is rotated 45 +/- 1 degrees with respect to the square region. The alignment accuracy between the photonic crystal orientation and the square region is critical for superprism performance.

Future work includes calibrating the photonic crystal hole size during the interference lithography exposure, determining a more robust hard mask layer other than chromium due to post-wet etch residue, and reactive ion etching of the silicon substrate material via reactive ion etching.

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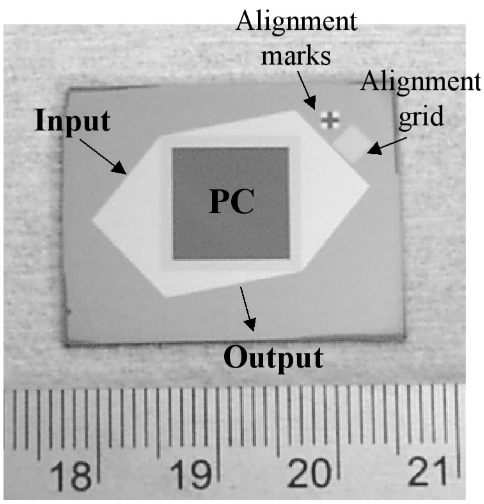
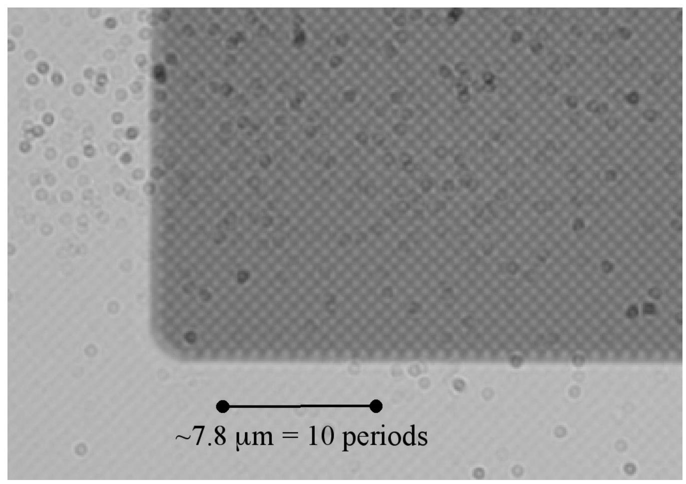


(a)



(b)

Fig. 29: (a) Digital photograph showing a top view of the superprism hard mask layers on a silicon substrate.
(b) Microscope image of the corner area of photonic crystal region.
Please note that the microscope lens has dust particles that can not be removed.

Application of RM^3 Integration to Optical Clock Distribution on Si-CMOS

Personnel

E. Atmaca and W. Giziewicz (C. G. Fonstad, Jr. in collaboration with D. Boning, MIT, and Y. S. Fatt, Nanyang Technological University, Singapore)

Sponsorship

MARCO Focused Research Center on Interconnect (MARCO/DARPA) and National Science and Engineering Research Council of Canada Postgraduate Scholarship

One of the most significant factors limiting future microprocessor performance and consumers of microprocessor power is the clock distribution network. As clock rates continue to rise, the design of the clock distribution network will assume an increased importance. From the power point of view, the H-tree or other networks that distribute the global clock to functional subunits are continually growing and must be charged and discharged during each cycle. From the performance point of view, as die sizes and clock rates increase, clock skew becomes very significant.

Optical clock distribution could address most of these problems. Depending on the scheme in use, deterministic skew may be significantly reduced. A global optical clock would also decrease power consumption as large metal lines (designed for high current-carrying capacity) would no longer require charging at each clock cycle. Optical distribution would also avoid a good deal of random skew for the same reason. Random skew in this design would be contributed by process variations affecting the performance of the optical receivers of the global clock. Circuit techniques to perform compensation of this sort of variation are being investigated and developed by Prof. Boning and his group at MIT. In a collaborative effort to study optical clock distribution, we are using our RM^3 (recess mounting with monolithic metallization) technology to integrate high performance III-V photodetectors on CMOS integrated circuit chips designed by Prof. Boning's group.

In this work, InP-InGaAs PiN diodes are to be integrated with Si-CMOS electronics to provide efficient, high speed photodetectors to receive the optical clock signals. As shown in Figure 30, diode heterostructures (grown by MBE in Prof. Yoon Soon Fatt's laboratory at Nanyang Technological University in Singapore) are being bonded to 0.18um Si-CMOS test chips designed by Prof. Boning and his students, and fabricated by a foundry, in this case, Taiwan Semiconductor Manufacturing Company. Following bonding, the diode heterostructures will be processed in place on the chip with the deposition of ohmic contacts, a mesa etch to control dark current, passivation dielectric material, and a metal line to join the diode ohmic contacts with Metal-7 V_{dd} lines.

We have, recently, also entered discussions with Profs. David Miller and Mark Horowitz of Stanford University regarding the use of our recess mounting technology to realize their direct input (no amplifier) optical clock distribution proposals to overcome process-related skew and to significantly reduce latency. A key requirement of their approach is that the capacitance seen at the output node of the photodiode, which in their approach is loaded by the junction capacitance of two photodiodes, the input to an inverter stage, and any associated parasitic capacitances, must be 10 fF, or less. We have proposed a RM^3-integrated device design that, in theory, achieves this level of performance, something that is not possible using other technologies they have considered. We expect to begin an effort to demonstrate this experimentally in the coming year.

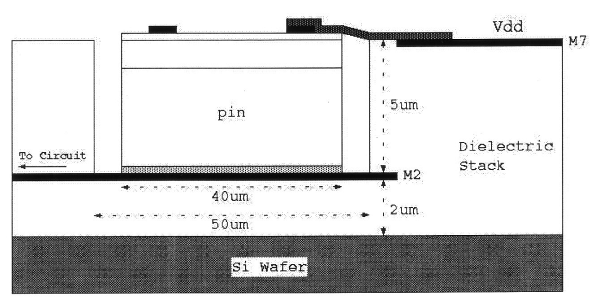


Fig. 30: Cross-sectional drawing illustrating a InP-InGaAs PiN photodiode ABP integrated on a CMOS integrated circuit chip for use in optical clock distribution studies.

Aligned Pillar Bonding Technology for RM^3 Integration

Personnel

E. Atmaca and W. Giziewicz (C. G. Fonstad, Jr.)

Sponsorship

NSF and MARCO Focused Research Center on Interconnect (MARCO/DARPA)

A new heterogeneous integration technique is under development which uses aligned, selective-area bonding to integrate III-V heterostructure devices, such as laser diodes and p-i-n detectors, with commercially-processed Electronic Integrated Circuits to create OptoelEctronic Integrated Circuits (OEICs) with VLSI levels of density and complexity. This technique has been named Aligned Pillar Bonding (APB); it is illustrated in Figure 31. The APB technique is similar in function to the Epitaxy-on- Electronics (EoE) technique in which III-V device heterostructures are first grown epitaxially in dielectric growth windows exposing the substrate surface in selected areas on fully-processed GaAs integrated circuit wafers. The APB process used bonding rather than direct selective area epitaxy to add heteostructures to processed IC wafers. It is compatible with any VLSI process on wafers that match the thermal expansion coefficient of the heterostructure wafer, meaning that GaAs-based heterostructures can be APB-integrated on both GaAs IC wafers and on silicon-on-sapphire IC wafers.

In the APB technique, the heterostructure for an optoelectronic device, such as a laser diode, is first grown under optimal conditions on the optimal substrate. The heterostructure is then patterned into pillars, which are in turn bonded into dielectric windows on a suitably prepared integrated circuit wafer (i.e., into the same windows that would be used for epitaxy in the Epitaxy-on-Electronics process). Doing this requires something more complex than encountered in previous III-V bonding experiments, namely alignment. The wafer on which the device heterostructure is grown and the pillars are formed, called the “source” wafer, must be aligned with the dielectric windows on the integrated circuit wafer onto which the devices are to be bonded. This wafer is called the “target wafer.

We have developed techniques using equipment developed originally for MEMS processing for achieving this alignment, and several years ago, demonstrated the successful aligned fusion of III-V pillars in dielectric windows on a GaAs IC chip. We, then, also demonstrated the subsequent removal of the substrate of the source

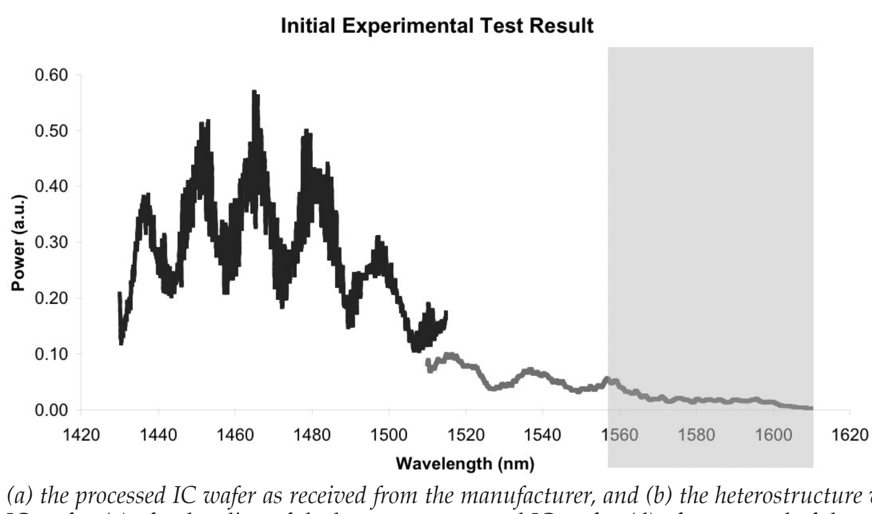


Fig. 31: The APB process: (a) the processed IC wafer as received from the manufacturer, and (b) the heterostructure wafer with pillars etched to match the windows on the IC wafer; (c) after bonding of the heterostructure and IC wafer; (d) after removal of the substrate of the device wafer leaving heterostructures bonded in the windows; and (e) after completing device processing and integration.

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wafer to complete the transfer of the pillars to the target wafer. That initial work involved direct semiconductor-to-semiconductor bonding and required substantial pressure to achieve contact and bonding. Subsequent work has investigated layered Au/Sn alloy-to-Au/Sn alloy, palladium-to-GaAs, and layered tin and palladium-to-GaAs bonding. Non-aligned bonding has been demonstrated using all three systems, and work on aligned bonding is continuing, with out current emphasis being on the first system. A major difficulty we have experienced recently, however, is accessing suitable aligned bonding equipment. Equipment in the MIT Microsystems Technology Lab does not currently have fixtures for work with partial wafers, an economic necessity when dealing with processed circuits. We have been using a bonder at Northeastern University with limited success.

Optimization of Cells for Microscale Themophotovoltaic Energy Conversion

Personnel

M. Masaki (C. G. Fonstad, Jr in collaboration with R. DiMatteo of C.S. Draper Laboratory, Inc., and P. Haglestein)

Sponsorship

C. S. Draper Laboratory, Inc.

In 2000, we succeeded in our effort to provide the first experimental demonstration that a significant increase in the rate of ThermoPhotoVoltaic (TPV) energy conversion (5 to 10 times) is obtained by positioning the active diode surface in extreme close proximity to the radiator (on the order of a tenth of the wavelength of the radiation, or less). The demonstration of this proximity effect, which we have earlier shown theoretically is due to enhanced evanescent coupling of radiation for the radiator to the cells, is the first step in the creation of a new class of Microscale ThermoPhotoVoltaic (MTPV) devices which promise to make the extraction of electrical energy from a wide variety of heat sources practical and to provide a new class of compact, portable sources of electricity. Moreover, MTPVs will be able to utilize thermal energy, now discarded as waste heat, and will enable increases in the overall efficiency of many complex systems.

The initial demonstration devices were InAs cells grown and fabricated at MIT. InAs cells are ideally suited for the applications ultimately envisioned for MTPV, but are less readily available than wide bandgap InGaAs diodes; so the Draper experimental work has continued using InGaAs cells obtained through their government sponsors. They have, recently, also begun procurement of cells with all of the contacts made to the epitaxial side of the wafer and designed to be “illuminated” through the substrate. Recalling that the proximity effect is due to enhanced evanescent coupling of light between the high refractive index radiator into the high refractive index cell, one realizes that the active junction need not be in close proximity to the source of radiation, making this substrate illumination geometry very attractive; because it places the temperature sensitive junction much further away for the high temperature source and significantly reduces the thermal management problem.

At MIT, we have concentrated on modeling and understanding how best to optimize the basic TPV device

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structure. An important aspect of our modeling effort has been directed at understanding the impact of the proximity effect on overall system efficiency. To the first order, one would expect that while the output level of a cell increases due to the proximity effect, the cell efficiency remains the same. Closer consideration, however, reveals that while the efficiency of the cell in converting absorbed photons to junction current will not increase, the overall power conversion efficiency will increase because of the concentrator effect. That is to say, because the diode characteristic is exponential, and the output power depends on the maximum of the product of the cell current and cell voltage, the power conversion efficiency of a TPV cell increases as one drives it harder, i.e., with more intense illumination and therefore, larger short circuit current. The parameter that matters in this situation is the ratio of the short circuit photocurrent to the reverse saturation current of the diode. The larger this ratio, the better, particularly when the ratio is relatively low. That is to say, if the ratio is already very high, as it is in the case of a silicon solar cell illuminated by sun light, for example, then increasing it by a factor of 10 improves the power conversion efficiency only a few percent, and it must increase by several orders of magnitude to have an appreciable effect. When this ratio is low (10^1 to 10^4, for example), however, as it is in the present case because we have narrow bandgap diodes (i.e. large saturation current) and weak illumination (i.e. small photocurrent), then increasing the ratio by even a factor of 10 can have a meaningful effect and can increase the efficiency 15 to 20%. Thus, the proximity effect has a dual impact on TPV cells. It significantly increases their rate of thermal-to-electrical energy conversion, and it increases the efficiency of this conversion.

In the past year, we have also participated in extensive discussions looking at other proximity effects that can be exploited to further increase the efficiency of the thermal-to-electrical energy conversion process.

Recess Mounting with Monolithic Metallization (RM^3) Polylithic Integration Technology

Personnel

E. Atmaca, E. Barkley, W. Giziewicz, J. Perkins, and J. Rumpler (C. G. Fonstad, Jr.)

Sponsorship

NSF , MARCO Focused Research Center on Interconnect (MARCO/DARPA) , SRC, and Singapore-MIT Alliance

Heterostructure devices, such as laser diodes and high electron mobility transistors, play an increasingly important role in our lives, and are key, enabling components of such common items as compact disk players, cellular telephones, fiber communication links, and direct broadcast television receivers. Their impact would be even greater, however, if a technology existed which could integrate heterostructure devices with silicon VLSI circuitry, using the same monolithic wafer-scale batch processing techniques that are largely responsible for the continuing Moore's Law growth of integrated circuit performance and functionality. Addressing this bottleneck, our research group in the MIT Microsystems Technology Laboratory and Center for Materials Science and Engineering has made significant advances in integrating complex compound semiconductor heterostructure devices with commercial VLSI (Very Large-Scale Integration) electronic circuits.

We refer to the general integration methodology we are pursuing as Recess Mounting with Monolithic Metallization, or RM^3 (i.e., "RM-cubed") integration, for short. This is a name introduced last year to more clearly indicate the common unifying themes of the several integration techniques we are studying: the mounting of the devices, or device material, to be integrated in shallow recesses formed in the surface of processed integrated circuit wafers, followed by continued monolithic processing to complete the devices, processing their electrical interconnection with the pre-existing circuitry using monolithic metallization.

Our Epitaxy-on-Electronics (EoE) and Aligned Pillar Bonding (APB) processes have been developed to integrate state-of-the-art heterostructure devices on commercially-processed GaAs and Silicon-on-Sapphire VLSI-level integrated circuits. Recently, we have initiated two new collaborative research programs in which we are integrating optoelectronic devices on custom designed silicon CMOS ICs for three quite different

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applications: optical clock distribution on CMOS chips, diffuse optical tomography subsurface imaging in living tissues, and free-space parallel optical signal processing. We have also continued our efforts to improve our techniques for heterogeneous integration, and to this end, we are researching a novel technique we call Magnetically-Assisted Statistical Assembly (MASA). In MASA, we form heterostructure nanopills and physically place them directly into the recesses on an IC wafer surface, exploiting statistics and magnetism.

Our successful Silicon-on-Gallium Arsenide (SonG) program has shifted from a program directed solely at providing wafers for optoelectronic integration to one also investigating three-dimensional integration of GaAs- and Si-based electronics. Most recently, we have begun investigating the use of the CMP (chemical-mechanical polish) techniques we have developed for this work to fabricate planar dielectric optical waveguides on the surface of processed Si wafers, in effect, adding additional optical "metal" layers to the normal backend process. These waveguides will be designed to couple directly to RM^3 integrated in-plane laser diodes and photodiodes, providing a total optical interconnect fabric for the electronics and optoelectronics communities.

More extensive descriptions of the individual projects within Professor Fonstad's RM^3 research program can be found in subsequent abstracts in this section.

Magnetically-Assisted Statistical Assembly

Personnel

J. Perkins and J. Rumpler (C. G. Fonstad, Jr.)

Sponsorship

Singapore-MIT Alliance and SRC

We have recently proposed a radically new approach to the heterogeneous integration of compound semiconductor devices, such as laser diodes with silicon integrated circuits, and have begun an experimental program to develop this technique. Our new approach, called Magnetically-Assisted Statistical Assembly (MASA), uses statistical self-assembly to locate compound semiconductor device heterostructures in shallow recesses patterned into the surface of an integrated circuit wafer, and short-range magnetic attractive forces to keep them there. When all of the recesses on the wafer are filled with heterostructures, the wafer is processed further to transform the heterostructures into devices monolithically integrated with the underlying circuitry. The process is summarized in Figure 32.

During statistical assembly, the surface of a wafer prepared with recesses will be flooded with several orders of magnitude more nanopills than are needed to fill its recesses. The large number of pills will mean that there are many pills in the vicinity of each of the recesses, and the highly symmetric nature of the pills and recesses will result in a high probability that a pill in the vicinity of a recess will fall into it. The strong short-range magnetic attractive force, which will come into play when a pill settles into a recess, will keep the pill from being removed from the recess by gravity or by another nanopill or by the fluid used to flood the surface with nanopills. The process can be favorably compared to carrier trapping by deep levels in semiconductors, and the probability that a given recess is filled will be one. Once the nanopills are assembled on the circuit wafer, they will be fixed in position using a polymer, which will also fill in any voids on the surface surrounding the pills and planarize the surface. Processing of the heterostructures to convert them into devices and integrate them with the underlying electronics then proceeds, using standard monolithic photolithographic processes.

With the help of Professor Zahn (MIT), we have analyzed the magnetic retention concept. Analysis of pat-

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terned hard magnetic layers, having both in-plane and out-of-plane magnetization, has been performed. The results suggest that both of these magnetization orientations will exert sufficient attractive force on nanopills coated with a permeable magnetic layer. This attractive force is very short range and for separations less than the nanopill thickness, far exceeds the force of gravity. The preliminary models showed an order of magnitude reduction in force using in-plane magnetic fields. However, the fabrication simplicity of in-plane hard magnetic material makes the reduced attractive force manageable.

Experimental work this past year has resulted in the refinement of the nanopill process and the target substrate process. Specifically, a ferromagnetic nickel layer has been successfully integrated with GaAs optoelectronic diode material. This process involves sputter depositing nickel and using a sputter etching technique to directionally etch the nickel layer. The GaAs/AlGaAs diode material is, then, reactively ion etched, using a BCl_3/Ar etch chemistry. The nanopills are, then, freed from their substrate by a backside substrate etch. The pills themselves are protected in a wax. The surrounding wax is dissolved in TCE. The solution is, then, centrifuged and decanted several times. This procedure produces a concentrated pellet of pills to be assembled. Optoelectronic pill yields were improved dramatically using these refined processing techniques.

The target substrate process involves the patterning of a cobalt hard magnetic film that has been deposited on a silicon substrate. Silicon dioxide is, then, deposited on top of this hard magnetic patterned media. Then 5.5 μm deep, 50 um diameter recesses have been reactively etched in this oxide. The etch stops on the patterned cobalt layer. We have also had collaboration with Dr. Chong Tow Chong of the Data Storage Institute in Singapore. Dr. Chong and his staff have prepared 250 period Co/Pd multi-layer films that have been patterned into a 5 μm period stripe pattern. These magnetic films along with the magnetic films fabricated at MIT have been characterized using a vibrating sample magnetometer.

The assembly technique has also been investigated and is being refined. Currently, a recirculating pump is being used in our system, enabling efficient use of pills. Further study of the assembly still needs to be done beyond these initial runs. Magnetic characterization of the magnetic material within the recesses must also be preformed. We will continue to investigate patterning techniques in order to obtain regular patterned material with 5-micron periods at the bottom of existing 5-micron deep recesses. With the successful development of the assembly process, our program will expand to encompass the use of this technology in a variety of applications.

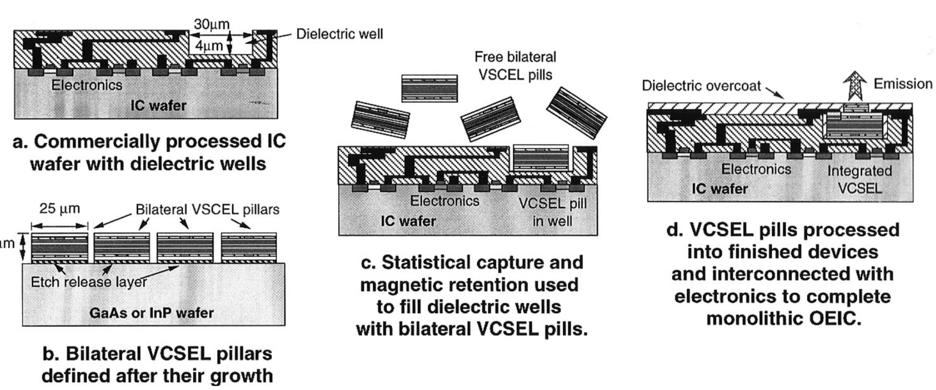

Fig. 32: The MASA process: (a) the processed IC wafer with the recesses prepared, and (b) the p-side down VCSEL wafer with pillars etched in a close-packed array; (c) statistical assembly of the freed nanopills in the recesses on the IC wafer; and (d) after completing device processing and integration.

Large Scale Oxidation of AlAs Layers for Broadband Saturable Bragg Reflectors

Personnel

S. N. Tandon, A. A. Erchack, J. T. Gopinath, T. Schibli, and G. S. Petrich
(L. A. Kolodziejski in collaboration with F. X. Kaertner and E. P. Ippen)

Sponsorship

ONR

Semiconductor saturable Bragg-reflectors (SBRs) are important components for the generation of femtosecond pulses from ultrafast laser systems. In order to create shorter pulses, it is necessary to use mirrors with a wider bandwidth. An alternative to GaAs/AlAs mirrors is to monolithically integrate absorbers onto broadband GaAs/Al_xO_y Bragg-mirrors, created by the steam oxidation of GaAs/AlAs dielectric stacks. The AlAs is converted to Al_xO_y using a wet oxidation system. Figure 33(a) and (b) show top and side views of a 500µm diameter SBR with a GaAs/Al_xO_y mirror stack. The top view shows a fully-oxidized 500μm diameter SBR. However, oxidation at 435°C for 3.5 hours resulted in delamination between the layers as shown in the side view. This delamination is possibly due to a number of factors; one of which is the weak bonding between GaAs and Al_xO_y.

By using low Al content AlGaAs layers instead of GaAs, the bonding between the layers can be strengthened, resulting in a stable mirror stack after oxidation. Figure 34(a) and (b) show top and side views of an SBR design that uses $Al_{0.3}Ga_{0.7}As$/Al_xO_y layers. The top view shows a fully-oxidized 500μm diameter SBR that has not experienced delamination. The cross-section shows the absorber layers consisting of an InGaAs quantum well between two GaAs buffer layers, and a 7 pair mirror stack of Al_xO_y/$Al_{0.3}Ga_{0.7}As$. For oxidation temperatures between 415°C and 435°C, the mirror stack was successfully oxidized without delamination. At higher temperatures, oxidation of the structure was limited by delamination of the absorber layer at the SBR edges, possibly due to interfacial strain. At 420°C, the mirror was completely oxidized in 4 hours without absorber delamination. Using $Al_{0.3}Ga_{0.7}As$ as the mirror's high index layer strengthens bonding between layers upon oxidation, while preventing significant oxidation of this layer.

In conclusion, saturable absorbers can be integrated with broadband Bragg-mirrors using epitaxial growth and the steam oxidation of AlAs layers. By using low Al content AlGaAs layers as the high index material in the dielectric stack, interfacial bonding is strengthened permitting the stable oxidation of large areas.

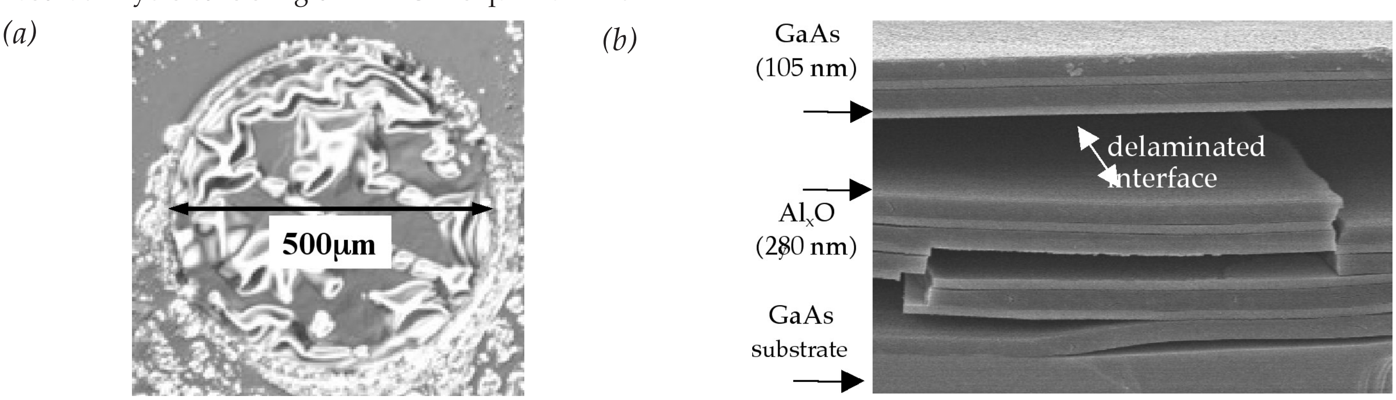

Fig. 33: (a) Top view SEM image of mesa structure oxidized at 435C for 3.5 hours.
(b) Cross-sectional SEM image showing the GaAs/Al_xO_y layers with delaminated interfaces.

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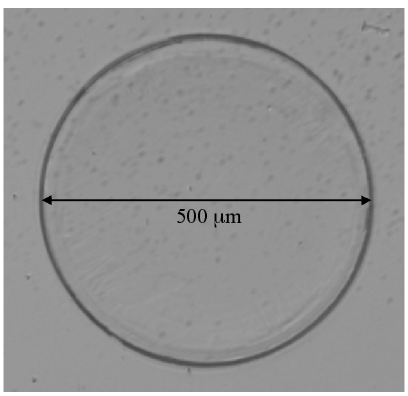
(a)



(b)

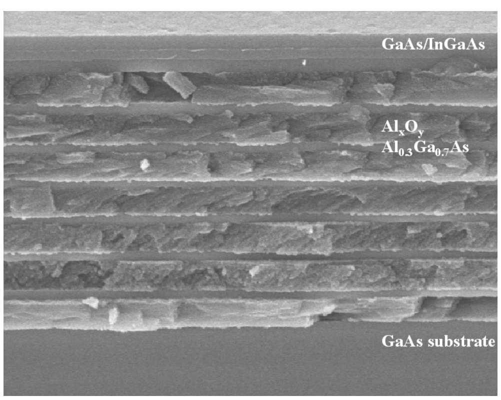


Fig. 34: (a) Nomarski image of fully-oxidized SBR. (b) SEM image of SBR cross-section showing 67 nm GaAs, 40nm InGaAs, 67 nm GaAs absorber with a 7 pair $Al_xO_y/Al_{0.3}Ga_{0.7}As$ mirror stack (~180nm/92nm).

Variable Amplitude Optical Fourier Filtering Using Controlled Thickness Metal Structures

Personnel

H. Iwai, L. DeFlores, G. Popescu, C. M. Fang-Yen, R. R. Dasari, and M. Feld

Sponsorship

NIH and Hamamatsu Co, Japan

Intense research efforts have been devoted at the Spectroscopy Laboratory towards investigating biological systems at the sub-micron level. Optical interference provides access to the phase information, which in turn allows obtaining information on a much smaller scale than the wavelength of light. In addition, using optical fields of $<$1mW power, the phase images are obtained in a completely non-invasive fashion. Thus, the technique we are developing has a great potential for the study of living biological samples, such as cultured cells, in their unperturbed environment. This opens the door for a whole new class of biological applications related to the nanometer dynamics of cells and organelles.

An important obstacle in obtaining high-contrast phase images from a confluent monolayer of living cells in the reflection geometry is represented by the strong specular reflection that takes place at the glass surface on which the cells are growing. This specular signal is characterized by a low-spatial frequency and can be labeled as "dc spatial component". This effect has two implications. First, even with AR coated cell wells, this signal is many times stronger than the light scattered from the cells themselves and tends to fill the well depth of the CCD used for imaging. Second, the specularly reflected field and the field backscattered by the cells are coherent and, thus, interfere, producing a total optical field characterized by a new phase, which can be quite different from the phase associated with the sample. In order to alleviate this difficulty, we used a traditional Fourier filtering arrangement to attenuate the spatial dc component. In the Fourier plane of a convergent lens, the specular reflection is focused onto a spot on axis. Thus, using a strong attenuator that covers this area, the dc component can be drastically limited. The obvious choice for the attenuator material was a thin metal film. Aluminum spots of different sizes and thickness have been deposited using the MTL facilities at MIT. The size of the attenuator dictates the "bandwidth" of the spatial filter, while its thickness determines the absolute attenu-

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ation provided. The initial desired attenuation factor was 100 (2 OD), which corresponds to an aluminum film of 35 nm. Various spot diameters, ranging from 25 microns to 150 microns, have been deposited on glass substrates. For a better flexibility, filters of different thickness have also been deposited. Preliminary results show that the quality of the images can be significantly improved by this filtering procedure, but the improvement varies from sample to sample. Thus, further analysis to find the most suitable metal structure properties is to be performed in the near future.

Towards Optical Logic

Personnel

A. Markina, S. J. Rodriguez, and G. S. Petrich
(L. A. Kolodziejski in collaboration with E. P. Ippen)

Sponsorship

DARPA and Lincoln Laboratory

Currently, network services impose bottlenecks on optical fiber communications. While network management complexity increases with the number of wavelengths that the fibers carry, most signal processing operations, such as switching and routing, are still performed electronically after Opto-Electronic (OE) conversion. An average internet packet transverses 16 nodes, with OE-EO conversions for electronic switching at each node. The development of ultrafast all-optical logic would make it possible to avoid multiple opto-electronic conversions and to distribute low-level network functionality in the optical core. High-level slow electronic processing would, then, be pushed to network edges. Desired functionality of all-optical signal processing includes routing, synchronization, and header processing. Developing a family of optical logic with complete Boolean functionality (an optical equivalent of Transistor-Transistor Logic) will be an important step in this direction.

This project includes the design of epitaxially-grown heterostructures that will form the basis for the optical logic, the optimization of passive components as well as the semiconductor optical amplifiers, a discussion regarding the issue of integrating active and passive components together on a single platform, and the design and analysis of an optical logic "unit cell". The proposed optical logic unit cell is based on an integrated Mach-Zehnder interferometer with a Semiconductor Optical Amplifier (SOA) in each arm. The unit cell will be designed for ultrafast 2x2 crossbar operation with an ideal extinction ratio and will be capable of performing a complete set of Boolean operations (AND, INV and XOR). Although the basic implementation does not address the issues of timing, reflections, and separating multiple co-propagating wavelengths, resolving these issues is crucial in order to ensure cascadability of individual unit logic cells.

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A schematic illustration of cascading three Mach-Zehnder interferometer-based "unit cells" together is presented in Figure 35. However, in order to operate properly, this optical circuit requires a number of additional devices. Time delays are used in order to equalize the optical path lengths in order to control the timing; while filters remove unwanted wavelengths, such as those used for the clock signal or control signals. Additionally, wavelength converters can be employed to resolve ambiguity between the data and the control signals. Absorbers can be inserted to eliminate the back reflections into the logic stages. Multiple wavelength clocks/control signals are required for cascading optical logic elements into larger functional blocks.

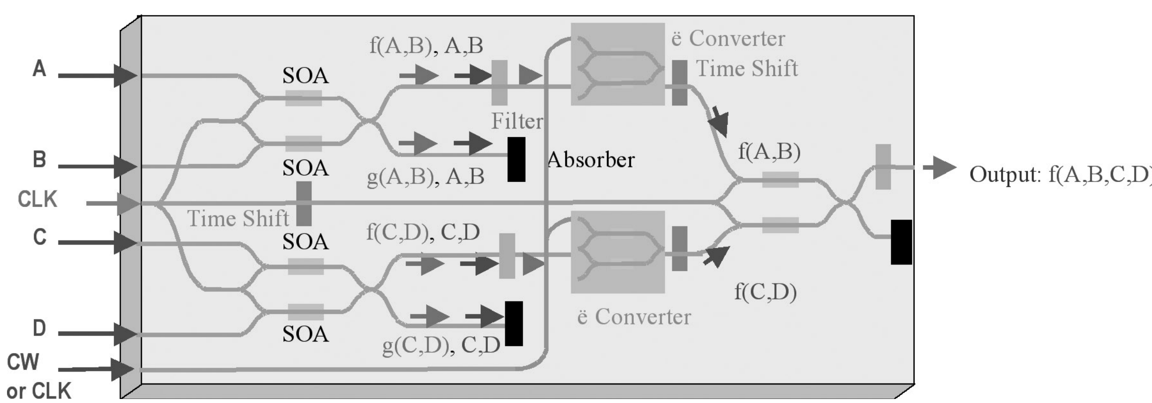

Fig. 35: Three unit cells cascaded on a chip with additional components that enable proper signal processing.

Design and Variation Analysis of an On-Chip Optical Clock Receiver Circuit

Personnel

N. Drego (D. Boning and M. Perrott)

Sponsorship

MARCO Focused Research Center on Interconnect (MARCO/DARPA)

As deep sub-micron CMOS technology continues to scale, decreasing gate lengths and line widths introduce greater variation, propagation delay, crosstalk, and other parasitics into clock distribution networks. Typical H-Tree and other balanced clock distribution schemes are becoming increasingly vulnerable to these effects, particularly to line-width variation and increased propagation delay. Often, buffers are inserted into the network so the total load seen at any segment of the network is decreased. However, buffers cannot compensate for line-width variation and crosstalk. Furthermore, power dissipation in the clock distribution network is becoming a significant fraction of the overall power budget.

An alternative to balanced electrical clock distribution networks is the use of an optical distribution network at the global level (See Figure 36). Light can be distributed to multiple receivers across the chip with low skew. If this light can be efficiently converted to an electrical signal and locally distributed using typical balanced networks, this idea becomes a viable alternative. Variation in the optical network can and will affect the optical signal received at the receiving photodetector. The extent to which this variation will affect the received signal is yet to be fully characterized. Thus, variation-robust optical receiver circuit design and analysis is a critical step toward implementation of on-chip optical clocks.

Two generations of receiver circuits have been designed with the intention of reducing the effects of variation. However, skew remains high (~200ps for a 1GHz clock). A third-generation receiver circuit (See Figure 37) has been designed using a fully-differential architecture. The advantages of differential signaling are primarily common-mode and power-supply rejection, enabling high-bandwidth amplifiers. Mismatch in differential circuits is a large problem in deep submicron processes. As such, offset compensation circuitry is employed to counteract mismatch effects. In addition to replica feedback biasing, a process-compensated current reference developed elsewhere has also been incorporated. Using such techniques, simulated skew due to process variation has been reduced to ~80ps, while clock frequency has been increased to 2GHz. Skew, however, is only one parameter that is characterized in a clock distribution network. Jitter is becoming more significant as clock frequencies scale upward. With circuit techniques such as active deskewing and those mentioned above, jitter is the dominant source of concern in clock distribution today. It is primarily the result of noise, particularly power-supply noise, and is not deterministic. Since noise tends to affect both signals in a differential circuit, it appears as a common-mode variation to differential amplifiers and is rejected. Mismatch can reduce common-mode and power-supply rejection, and thus, noise analysis must be done.

More work remains to be done in studying variation in the optical network as well as determining how further CMOS scaling will affect variation. Furthermore, it remains to be seen whether the optical alternative will prove as advantageous to clock distribution as previously hoped for.

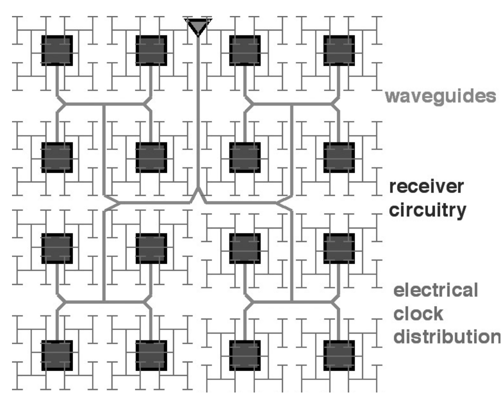

Fig. 36: Global optical clock with local electrical clock distribution.

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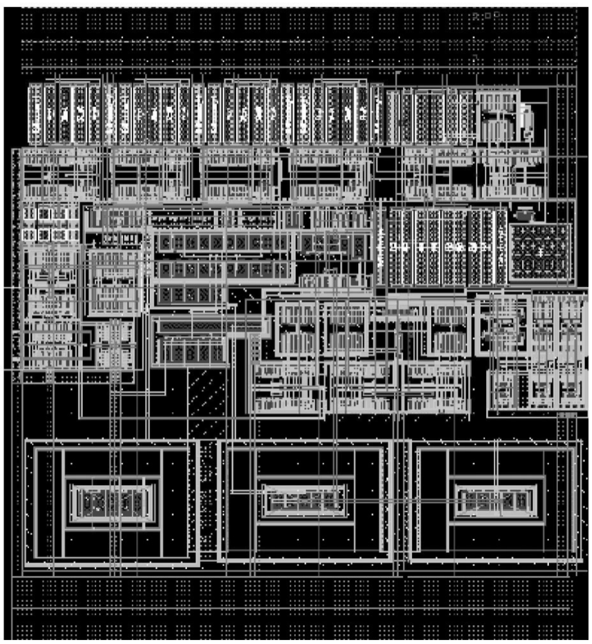

Fig. 37: Third generation clock receiver circuit.

Optical Nano-Electromechanics

Personnel

R.E. Bryant, S. Assefa, P. Rakich, M.L. Povinelli, S. G. Johnson, and G.S. Petrich, (H.I. Smith and L.A. Kolodziejski in collaboration with E.P. Ippen, and J.D. Joannopoulos)

Sponsorship

NSF

A major focus of optical engineering research is to bring optical systems to the large-scale functionality of electrical systems. Striving to reach this objective, a variety of optical devices are currently being developed in an aluminum gallium arsenide III-V material system. The III-V material system is the choice optical bench in which these optical devices are being developed due to advances in material engineering, which allows nanometer precision of high index contrasting layers, ranging from oxidized aluminum arsenide to gallium arsenide. As a result of such precision, a variety of optical manipulations can be carried out with nanometer-sized devices at micron-sized wavelengths. Presently, the focus has been set upon the deployment of nanometer-sized electromechanical-actuated waveguide devices with the prospect of broadening the functionality of integrated optical systems. These devices are termed Optical NanoElectroMechanical devices (ONEM devices).

The ONEM device that is currently being developed, routes optical energy between two adjacent waveguides by lateral coupling after an electrostatic mechanical deflection of the waveguides from an applied voltage. Initially, in a ground state (zero applied voltage), a distance of g_o separates the waveguides. The initial g_o separation is defined using electron beam lithography and is set as to not allow for any lateral coupling between the two adjacent waveguides. A potential difference is then applied to both waveguides, which then reduces the separation of the waveguides.

The initial separation of g_o and the deflected separation of g_{couple} are determined from optical simulations and electromechanical simulations of the two-waveguide system. The separations g_o and g_{couple} are contingent upon the width, thickness, length, and geometry of the two waveguides. Due to the dynamic relation arising from the optics and the electromechanics of the ONEM device, iterations of both types of simulations are being done for a variety of configurations in order to optimize design trade-offs between the optical and electromechanical operations. Figure 38 shows some prototypes of the ONEM device.

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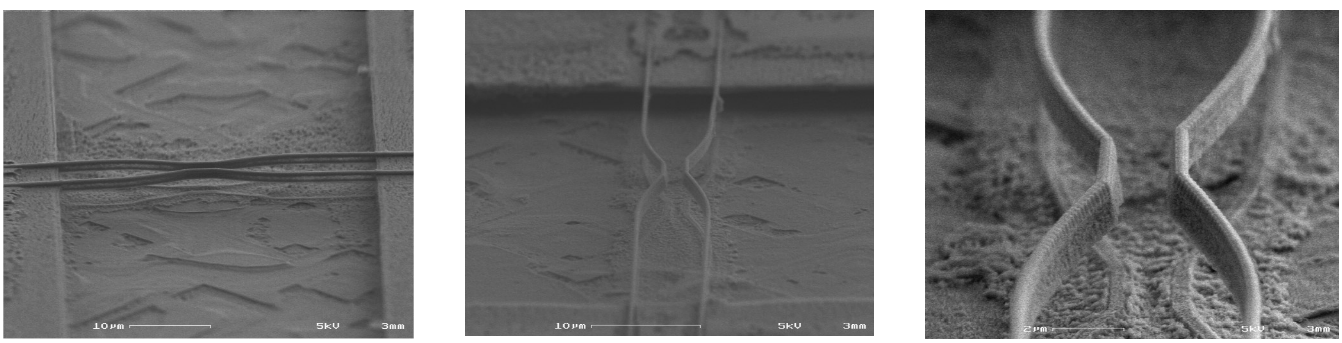

Fig. 38: SEM images of a fabricated ONEMS device in a gallium arsenide-based material system with an exponentially tapered geometry.

Optoelectronic Integrated Circuits for Diffuse Optical Tomography

Personnel
W. Giziewicz (C. G. Fonstad, Jr. in collaboration with S. Prasad and D. Brooks, Northeastern University)

Sponsorship
NSF

Diffuse Optical Tomography (DOT) is an emerging medical imaging technique in which tissue is illuminated by near-infrared light. The multiply-scattered light which emerges is observed with an array of detectors, and then, a model of the propagation physics is used to infer the localized optical properties of the illuminated tissue. The primary absorbers at the wavelengths of interest (approximately from 780 nm to 830 nm), water and both oxygenated and de-oxygenated hemoglobin, all have relatively weak absorption but strong scattering characteristics. The most important current applications of DOT are detection of tumors in breast tissue and imaging of the brain.

The current state of the art in DOT systems involves light sources and detectors coupling to the measured tissue through optical fibers. The resulting systems are quite large and complex. An optoelectronic circuit that would integrate light emission, detection, and signal amplification on-chip would provide a drastic reduction in size, cost, and complexity. It would also open new applications for this technique, potentially including implantable devices. An illustration of how the DOT OptoElectronic Integrated Circuit (OEIC) might be used for subsurface imaging *ex-situ* is presented in Figure 39.

The OEIC will be fabricated in a 1.5 μm low-noise analog process by AMI Semiconductor, through MOSIS. The design of the circuitry is under way, and the layout will be submitted in mid-2003. An important part of the design process was verification of length-scales for the design. On-chip, detector, and emitters will be separated by between one and four optical scattering lengths. Monte Carlo simulations were performed to confirm that a diffuse optical field would be seen at such small separations. The effect of intensity on angle of incidence of the light was also investigated, and it was found that with separations above approximately one scattering length, the diffusely reflected light behaves as desired.

Once returned from fabrication, MBE-grown LEDs will be integrated into the chip using a metal-semiconductor Aligned Pillar Bonding (APB) technique. The devices will be tested with the help of Prof. Brooks at Northeastern University and his collaborators at Massachusetts General Hospital.

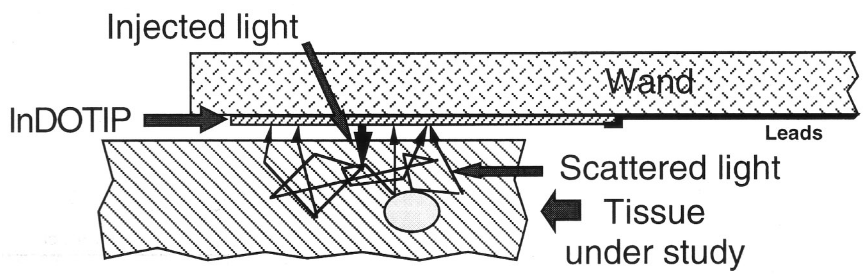

Fig. 39: An illustration of one way the DOT OEIC die might be mounted on the end of a wand and used for DOT subsurface imaging of soft body tissue. In use, each VCSEL is illuminated in turn (the figure shows one turned on) and the pattern of scattered light seen by the detector array is recorded. With this information, an image of the sub-surface structure can be constructed.

Investigation of Dark Line Defects in Semiconductor Laser Diodes

Personnel

K. H. Choy (C. G. Fonstad, Jr.)

Sponsorship

Singapore-MIT Alliance

Heteroepitaxial growth of gallium arsenic (GaAs) and indium phosphide InP-based materials on silicon has been studied for over 20 years. The large differences in lattice constants between silicon and the III-V materials useful for optical devices is the most critical hurdle which has beset the development of this technology. When these materials are epitaxially growth on Si directly, dislocations of great density were found to thread through the films. These dislocations act as sites for nonradiative recombination of electron and holes, lowering the performance of the devices. Furthermore, such electron-hole recombination events drive the expansion of these threading dislocations in the active region of the devices, causing more nonradiative recombination; the devices degrade quickly in the process.

Such degradation also occurs in devices grown on lattice-matched substrates, due to the small but finite number of dislocations inevitably existing there, or induced during the processing of the devices. It has been found that when the GaAs quantum wells in GaAs/AlGaAs lasers are replaced with strained InGaAs ones, this elongation process of the threading dislocations can be significantly retarded, and lifetimes of the devices are enhanced. The origin of this retardation is still in dispute, and it is not clear to what extent this technique can assist the epitaxial growth of III-V materials on silicon, when the density of dislocations is very large.

The core of this thesis will be to carry out a systematic study of this effect; (1) by deliberately generating a known density of dislocations in layers grown on GaAs substrates, (2) by controlling the amount of strain in InGaAs quantum wells through which these dislocations will thread, and (3) by observing their degradation. The structures will be grown in a solid source molecular beam epitaxial system. They will be started with thin layers of mismatched materials that generate approximately known amounts of threading dislocations. Then, InGaAs relaxed graded buffers with different final compositions will be grown. The subsequent parts of the growth, including the claddings of the lasers, will be grown lattice matched to the top of the graded buffer layers. The InGaAs quantum wells, however, will all have identical composition, regardless of the lattice constants of the claddings sandwiching them. By doing so, the quantum wells will be set in different states of strain, depending on the differences between the lattice constants of the quantum wells and those of the final compositions of the graded buffers, which will be different from sample to sample. The goal is to isolate and investigate the factors contributing to the significant suppression of laser degradation, resulting from the use of strained InGaAs quantum wells. Hopefully, it will also add to the understanding of the laser degradation process itself.

Compact Optoelectronic Neural Co-processor Project

Personnel

B. Rudlinger (C. G. Fonstad, Jr. and C. Warde)

Sponsorship

National Science Foundation

We have just initiated a research program to develop algorithms and architectures, and to fabricate and demonstrate a rugged, compact, modular, versatile, Optoelectronic, Integrated-Circuit (OEIC) neural network and fuzzy logic co-processor system that would work in conjunction with the standard PC microprocessor. This OEIC co-processor will perform sophisticated parallel and/or fuzzy processing operations more efficiently than the standard PC microprocessor. The proposed OEIC co-processor will be about the size of a CD-ROM drive, and thus, would fit easily inside the case of a conventional personal computer. Another important goal of the program is that this compact OEIC co-processor be amenable to mass manufacturing.

The key feature (and advantage) of the proposed class of OEIC co-processors is that they combine the parallel processing and longitudinal (inter-plane) free-space communication strengths inherent in optics with the transverse (intra-plane) communication and computation strengths of electronics to realize extremely powerful and versatile machines. This work distinguishes itself from earlier attempts in that: (1) for the first time in history all of the needed components are available with sufficient performance to demonstrate the co-processor, and (2) we have a unique design and packaging technology that takes care of the alignment, compactness, and ruggedness issues.

To demonstrate the feasibility of the co-processor, the proposed hardware development tasks include: (1) design, fabrication, and characterization of novel 2-D arrays of GaAs-SOS (silicon-on sapphire) OEIC cascadable smart pixels with a detector, integrated-circuit logic, and a light source in each pixel (Resonant Cavity Light-Emitting Diodes (RCLEDs) in the first two years of the program, and Vertical-Cavity Surface-Emitting Lasers (VCSELs) replacing the RCLEDs in the third year), (2) design, fabrication, and characterization of novel reconfigurable optical interconnection elements based on arrays of Bragg-holographic phase gratings, (3) alignment (with the help of a mask aligner) and gluing of all the components of the co-processor (OEICs, interconnection elements, and output photodetector array) together into a rugged, compact, modular multi-layer sandwich configuration so as to permanently solve any micro-optics alignment problems, and (4) characterization of the resulting high-speed, multilayer optoelectronic co-processor.

In addition to the above-mentioned fabrication tasks, another early focus of the program will be on neural network configurations. We will carry out the following theoretical, modeling and simulation tasks related to this aspect of the program: (a) develop algorithms, especially those suitable for programmable nearest-neighbor interconnections (e.g. pulse-coupled networks) to solve a large class of multi-dimensional information processing problems, and (b) explore the application of these novel co-processors to three different types of problems: (i) associative-memory-based pattern recognition, (ii) medical image segmentation, and (iii) fusion of a set of low-contrast spectro-polarimetric infrared images into a single high-contrast image.

Terahertz Quantum Cascade Lasers

Personnel

B. Williams, H. Callebaut, S. Kumar, and S. Kohen (Q. Hu in collaboration with Dr. J. Reno at Sandia National Lab)

Sponsorship

National Science Foundation, NASA, and AFOSR

Semiconductor quantum wells are human-made quantum mechanical systems in which the energy levels can be designed and engineered to be of any value. Consequently, unipolar lasers based on intersubband transitions (electrons that make lasing transitions between subband levels within the conduction band) were proposed for long-wavelength sources as early as the 1970s. However, because of the great challenge in epitaxial material growth and the unfavorable fast nonradiative relaxation rate, unipolar intersubband-transition lasers (also called quantum-cascade lasers) at mid-infrared wavelengths were developed only recently at Bell Laboratories. This achievement paved the way for development of coherent laser sources at customized frequencies ranging from THz to near-infrared. However, compared to the infrared QCLs, THz QCLs at much longer wavelengths face unique challenging issues. First, the energy levels corresponding to THz frequencies (1 THz = 4 meV) are quite narrow, thus, it is very challenging to design quantum well structures for selective injection to the upper level and selective depopulate electrons from the lower level. The requirements for fabrication of such quantum-well structures with adequate accuracies are also demanding. Because of the narrow separation between subband levels, heating, and electron-electron scattering will have a much greater effect. Also, the small energy scales of THz photons make the detection and analysis of spontaneous emission (a crucial step toward developing lasers) quite difficult. Second, mode confinement, which is essential for any laser oscillation, is difficult at longer wavelengths. Conventional dielectric-waveguide confinement is not applicable because the evanescent field penetration, which is proportional to the wavelength and is on the order of several tens of microns, is much greater than the active gain medium of several microns. Recently, we have made breakthroughs in developing quantum-cascade lasers at 3.4 THz (corresponding to 87 μm wavelength), and more recently, at an even longer wavelength of 100 μm. In both laser structures, population inversion was achieved with resonant phonon scattering for the depopulation of the lower level. Key results are summarized in the following sections.

THz quantum cascade lasers based on resonant phonon scattering for depopulation

The direct use of LO-phonon scattering for depopulation of the lower state offers several distinctive advantages. First, when a collector state is separated from the lower state by at least the phonon energy $h\omega_{LO}$, depopulation can be extremely fast, and it does not depend much on temperature or the electron distribution. Second, the large energy separation provides intrinsic protection against thermal backfilling of the lower radiative state. Both properties are important in allowing higher temperature operation of lasers at longer wavelengths.

The present design combines advantages of our two previously investigated THz emitters. As shown in Figure 40, the radiative transition between levels 5 and 4 is spatially vertical, yielding a large oscillator strength. The depopulation is highly selective, as only the lower level 4 is at resonance with a level 3 in the adjacent well where fast LO-phonon scattering takes place. The four-well structure inside the dashed box is one module of the structure, and 175 such modules are connected in series to form the quantum cascade laser.

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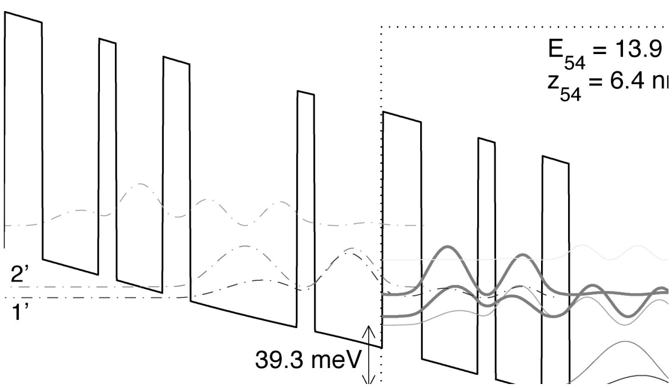
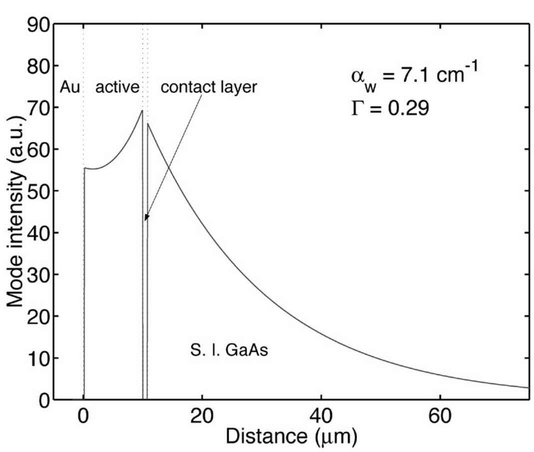


Fig. 40: Conduction band profile calculated using a self-consistent Schrödinger and Poisson solver (80% conduction band offset) biased at 64 mV/module. Beginning with the injector barrier, the layer thickness in Å are 54/78/24/64/38/148/24/94. The 148-Å well is doped with Si at 1.9×10^16/cm^3, yielding a sheet density of 2.8×10^10/cm^2.

Mode confinement in this laser device was achieved using a surface plasmon layer grown under the active region. The schematic of the device structure and the calculated mode profile and waveguide loss are shown in Figure 41. The calculated waveguide loss of 7.1 cm^{-1} and mode confinement factor $\Gamma \approx 29\%$ are quite favorable compared to the calculated gain of our laser device.

Lasing at 3.437 THz ($\lambda = 87.2$ μm) was obtained in this device at a threshold current density of 840 A/cm^2 at 5 K. Typical emission spectra above threshold are shown in Figure 42. The emission frequency corresponds to an energy of 14.2 meV, close to the calculated value of 13.9 meV. For much of the bias range, the emission is dominated by a single mode, although the spectrum shifts toward a higher mode with increasing bias due to the Stark shift.

Measured optical power versus current (*P-I*) curves at low duty cycle are plotted in Figure 43(a). Lasing is observed up to 64 K (72 K in a more recent measurement) with a power level of 25 μW, compared to the 2.5 mW observed at 5 K. Figure 43(b) displays the voltage versus current, as well as several *P-I* curves taken for pulses of increasing width. Even at a high 50% duty cycle, the laser still produces 0.5



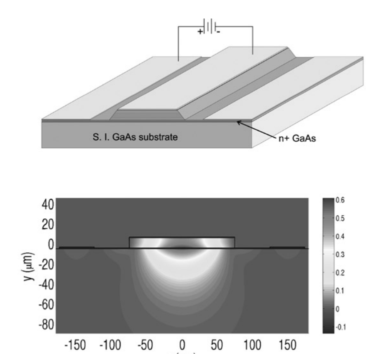


Fig. 41: Schematic of the THz laser ridge structure, calculated two-dimensional mode profile using FEMLAB (on the left), and one-dimensional mode profile, confinement factor, and waveguide loss (on the right).

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mW of peak power, indicating its robustness. The result of this initial success is quite promising. We are confident that improvement in injection efficiency, mode confinement, and fabrication process will readily lead to CW operation of THz quantum cascade lasers at liquid-nitrogen or higher temperatures, and at even longer wavelengths where electronic devices, such as transistors, have been the only functional solid-state devices. Clearly, such a development will have a qualitative impact on science and technology in the THz frequency spectra.

THz quantum cascade lasers using metal waveguides for mode confinement

After our initial success in the development of 3.4-THz quantum cascade laser, one of the improvements was made in the mode confinement. As shown in Figure 41, the mode confinement using surface plasmon layer yields a relatively low mode confinement factor of $\Gamma \approx 0.29$. This mode confinement is sufficient for lasing at 3.4 THz. However, as we are developing even longer wavelength quantum cascade lasers, the mode confinement will become much worse or even unconfined at frequencies lower than 2 THz for the carrier concentration in our laser structures. An alternative method for mode confinement is to use metal waveguides. As shown in Figure 44(a), the mode is now tightly confined between the top and bottom metal contacts, yielding a confinement factor close to 100%. Figure 44(b) shows the process of wafer bonding and selective etching to fabricate such a metal waveguide structure. This process was developed by a former student Bin Xu in 1997.

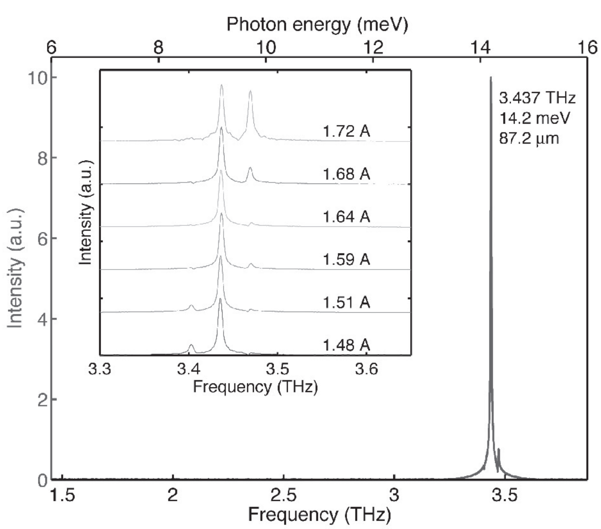

Fig. 42: Emission spectrum above threshold biased at 1.64 A at 5K heat sink temperature. The inset shows an expanded view of spectra at various bias points, offset for clarity.

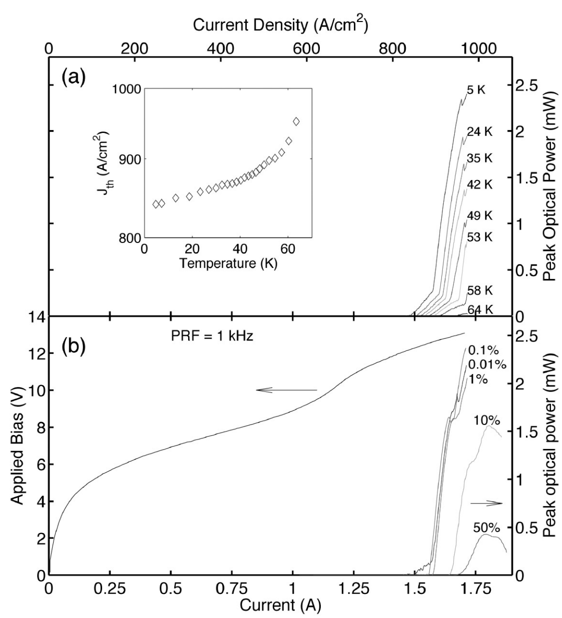

Fig. 43: (a) Emitted light versus current at various temperatures. The inset is a semi-log plot of the threshold current density J_{th} as a function of temperature. (b) Applied bias voltage and peak optical power versus current, collected at various duty cycles.

continued

Using this novel mode confinement structure, we have recently developed a quantum cascade laser at 100-μm wavelength. The power-current relation and emission spectrum of this laser are shown in Figure 45. The laser operates up to 70 K, and the wavelength of 100 μm is among the longest achieved in QCLs. This is the first successful demonstration of using metal waveguides for mode confinement at THz frequencies. In fact, devices fabricated from exactly the same wafer but using the surface plasmon layer for mode confinement did not achieve lasing, which demonstrates a clear advantage of the metal waveguide over that of surface plasmon layer in mode confinement. As we proceed towards even longer wavelengths, to approach the ~300-μm range where electronic devices such as transistors function, this advantage will become more significant and even crucial.

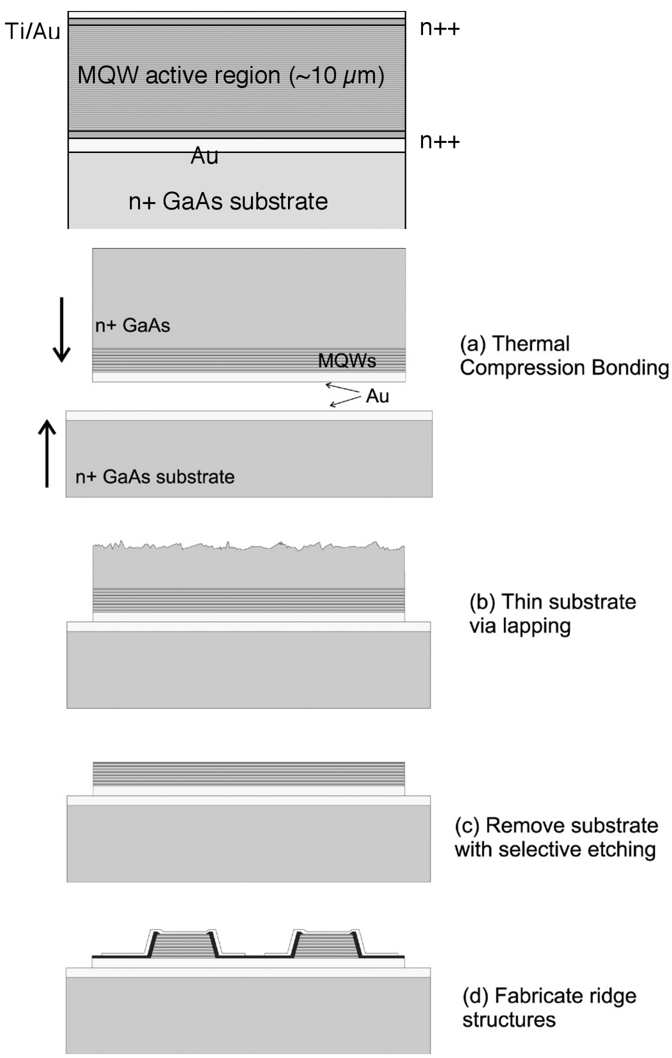

Fig. 44: Top: Side view of a metal waveguide structure for THz mode confinement. Right: Fabrication process of the metal waveguide structures.

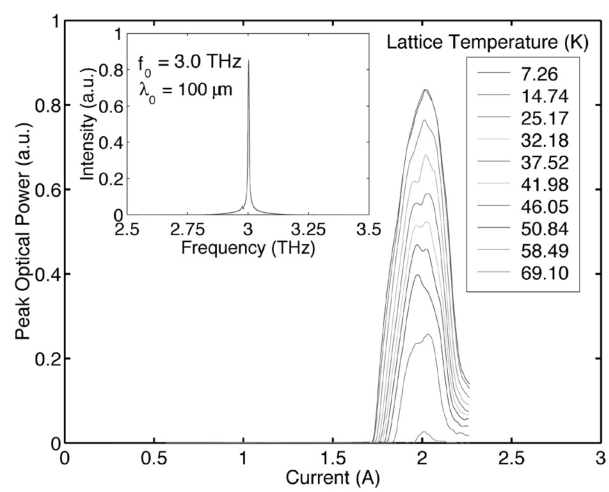

Fig. 45: Power-current relations of a laser device using metal waveguide for mode confinement, measured at heat sink temperatures up to 70 K. Inset: Emission spectrum taken at a bias voltage 11.4 V and current 1.8A. The spectrum is single-mode, and the wavelength is among the longest achieved in QCLs.

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Analysis of transport properties of THz quantum cascade lasers

Even though mid-infrared and THz quantum cascade lasers operate on the same principle, that is, intersubband transition in semiconductor heterostructures, they show a qualitative difference in the dynamics of electron transport. For mid-infrared QCLs, the subband separations exceed the LO-phonon energy $h\omega_{LO}$, and electron transport is dominated by LO-phonon scattering. For THz QCLs, many subband separations are smaller than $h\omega_{LO}$, only the high-energy tail of a hot electron distribution is subject to the LO-phonon scattering, which results in a significantly higher temperature sensitivity for the electron transport and a far greater importance of electron-electron (e-e) scattering. The long delay in the development of THz QCLs is testimony to the difficulty of achieving population inversion involving these complicated transport mechanisms. It is, thus, important to quantitatively model these transport processes to extend the operation of THz QCLs to broader frequency ranges and higher temperatures.

Our transport analysis is based on Monte Carlo (MC) simulations, which have been used to analyze and design mid-infrared and THz QCLs. Compared to conventional rate-equation analysis, the MC method is especially useful for THz QCLs, as it does not rely on a specific model for carrier distributions and can easily handle temperature- and density-dependent scattering times. Figure 46 illustrates the flow chart of our Monte Carlo simulation scheme. It follows a conventional scheme for an ensemble of particles, in our case 10^4 particles, with a focus on e-e and e-phonon interactions involving the electrons in one module of the device under study. An electron that scatters out of a module is reinjected with identical in-plane *k*-vector into a subband equivalent to its destination subband, in accordance with the spatial periodicity of QCLs.

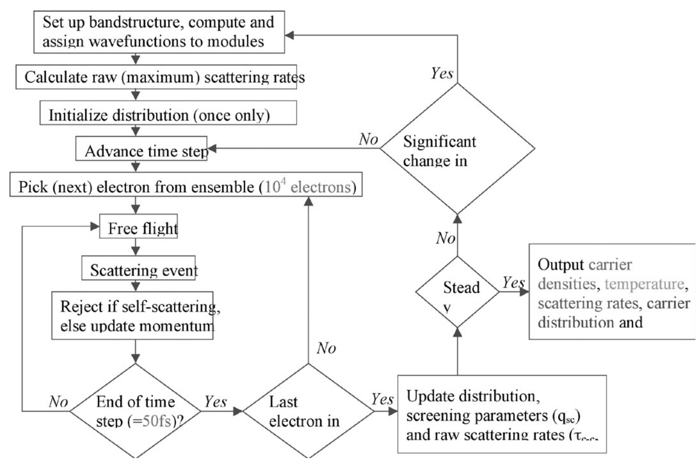

Fig. 46: Flow chart of our ensemble Monte Carlo simulation scheme.

The results of the Monte Carlo simulations, focused on the 3.4-THz laser structure shown in Figure 41, are summarized in Figure 47. All simulations assumed a lattice temperature of 25 K, corresponding to a 10 K heat sink temperature. In Figure 47(a), the calculated I-V relation qualitatively resembles that of measured one, with the calculated peak current density is noticeable lower. This discrepancy suggests the scattering processes in the MC simulations are slower than in actual devices. The slower scattering processes yielded a higher calculated peak gain than inferred from experiments, as shown in Figure 47 (d). The two horizontal lines are calculated total cavity losses with one facet Au coated and without any facet coating. Our device lased only with one facet coating, thus the two lines define the range of material gain in our laser device. The qualitative agreement between the MC and experimental results indicate the usefulness of MC simulation as a design tool. The discrepancy requires further investigation of all important scattering channels.

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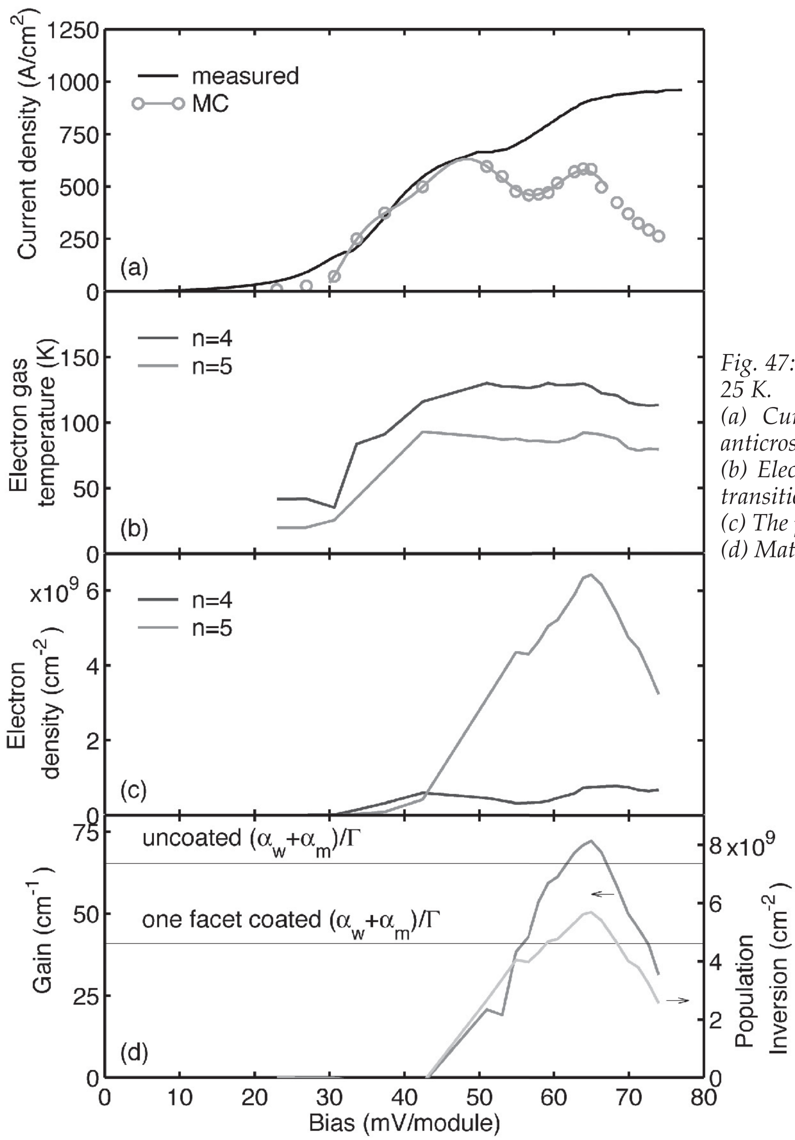


Fig. 47: Key results of the MC simulation for a lattice temperature of 25 K.
(a) Current density for a range of bias voltage. The injection anticrossing occurs at 65 mV/module.
(b) Electron temperature for the subbands involved in the radiative transition, n = 4 and n = 5.
(c) The population density in n = 4 and n = 5.
(d) Material gain and population inversion for different biases.

Development of Bipolar Cascade Lasers

Personnel

R. D. Williams, A. Markina, and G. S. Petrich (R. Ram and L. A. Kolodziejski)

Sponsorship

DARPA-OptoCenter

The bipolar cascade laser design aims to combine two or more lasing active regions in epitaxial series. Previous work realized room temperature, continuous wave, and bipolar cascade lasers at 980 nm. Currently, the work has focused on transitioning the design from using quantum wells that emit at 980 nm to quantum dots that emit at 1300 nm, as well as, improving the characteristics of the reverse-biased tunnel junction which connects the consecutive active regions.

As 1300 nm is an important wavelength in telecommunications, recent work has focused on obtaining InAs quantum dots on GaAs substrates. InAs quantum dots extend the range of achievable emission wavelengths of GaAs-based active devices well into the functional telecommunications regime. Furthermore, quantum dots allow for the realization of ultra-low laser threshold currents, narrow emission spectra, improved gain properties, and increased temperature stability. Photoluminesence studies have shown strong emission between 1250-1300 nm. Careful control of the growth conditions, such as the substrate temperature and deposition rate, has allowed precise control over the emission wavelength and intensity. Atomic force microscopy has been used to confirm the presence of quantum dots and has shown their average diameter to be around 20 nm as shown in Figure 48.

The introduction of indium into the GaAs tunnel junction material is theorized to improve the differential resistance of the junction and thereby, increase the tunneling current, resulting in improved quantum efficiency for the laser. Samples have been grown by gas source molecular beam epitaxy and processed to examine the effects of indium-incorporation and are currently undergoing electrical testing. Bipolar cascade lasers using 980 nm emitting quantum wells have been integrated with indium containing tunnel junctions and are undergoing processing.

The current aim of the project is to produce a bipolar cascade laser on a GaAs substrate containing quantum dot active regions and operating at 1300 nm. Laser structures have been grown and are currently undergoing processing and testing.

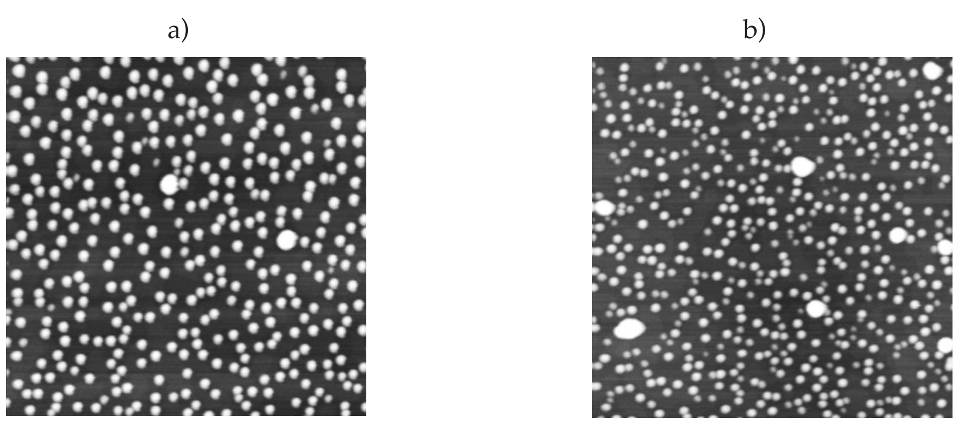


Fig. 48: Atomic force micrographs of 1 µm x 1 µ m square areas. a) With the arsine flow =0.1 sccm, the density of InAs quantum dots is 4 x 10^{10} cm^{-2} and the average diameter is 23 nm. b) With the arsine flow =1.0 sccm, the density of InAs quantum dots is 6 x 10^{10} cm^{-2} and the average diameter is 21 nm.

Design and Fabrication of a Superprism Using Two Dimensional Photonic Crystals

Personnel

S. Tandon, C. Luo, M. E. Walsh, and G. S. Petrich (L. A. Kolodziejski, H. I. Smith, and J. D. Joannopoulos)

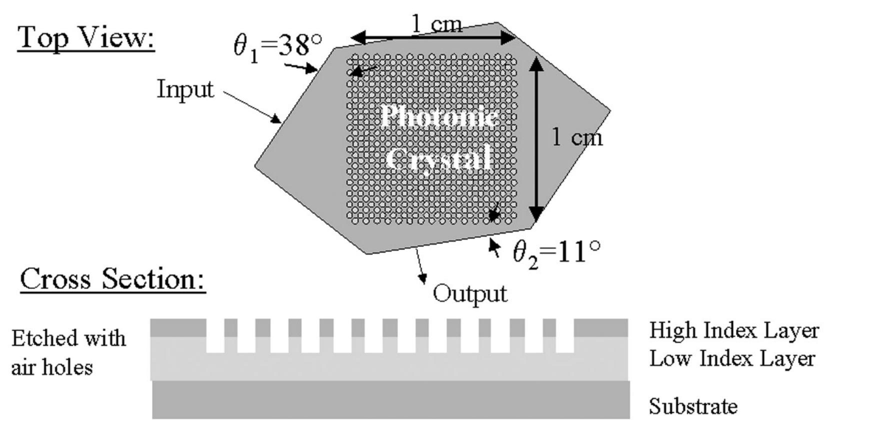
Sponsorship

DARPA/Rockwell Scientific Corp.

A superprism is an optical device similar to a conventional prism but with two enhanced properties: (1) super-dispersion and (2) ultra-refraction. Just as a conventional prism separates light into its component wavelengths, a superprism separates these wavelengths over wider angles--termed “super-dispersion.” A superprism can magnify the angle of propagation of a single wavelength of light to steer the beam over wide angles--termed “ultra-refraction.” Photonic crystals are responsible for the superprism effect. Superprism effects would be useful in a number of applications, ranging from enhanced devices for Wavelength-Division Multiplexing (WDM) to a new class of ultra-refractive optical elements for beam manipulation.

Our superprism consists of a 2D photonic crystal with a square lattice of cylindrical air holes in a high index material such as silicon or gallium arsenide. The top view schematic of the device shape is shown in Figure 49. The device is hexagonal shaped with the Photonic Crystal (PC) occupying a square region in the center. The initial design has focused on realizing ultra-refraction such that an input angular sweep of approximately +/- 2 degrees is amplified to about +/- 30 degrees at the output for a wavelength of 3.2 μm. A thick low-index layer is used to minimize radiation loss into the high index substrate.

The feature sizes of the photonic crystal can be scaled depending on the wavelength of operation as shown in Figure 49. Our desired wavelengths of 3.1μm and 1.55μm imply hole lattice constants of 750nm and 372nm, and hole radii of 300nm and 150nm. The total thickness of the device (excluding substrate) is about 3.5 microns (460nm GaAs, 3μm Al_xO_y), while the top surface will have an area somewhat larger than 2x2cm.



	GaAs Substrate		Si Substrate	
	λ=~3.1 μm	λ=~1.55 μm	λ=~3.1 μm	λ=~1.55 μm
PBG Lattice Constant	750 nm	372 nm	750 nm	372 nm
PBG Hole Radius	300 nm	150 nm	300 nm	150 nm
High Index Thickness	450 nm	223 nm	700 nm	205 nm
Low Index Thickness	3000 nm	1500 nm	3000 nm	3000 nm

Fig. 49: Superprism device design showing top and side views of the device.

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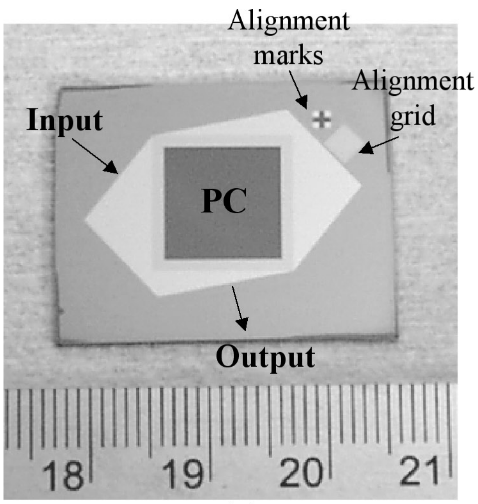
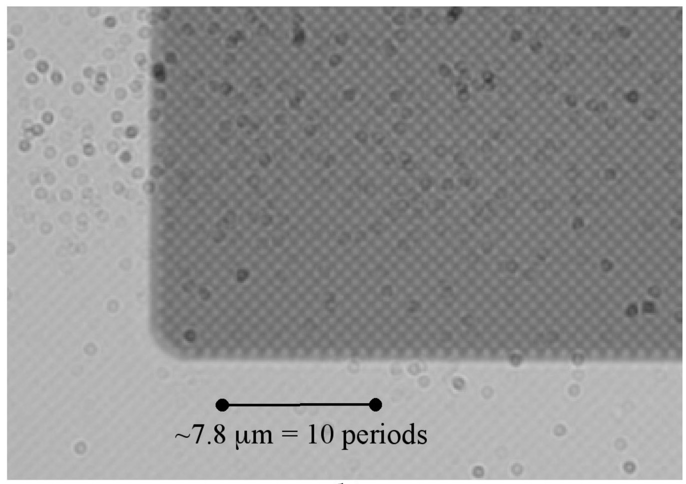


(a)



(b)

Fig. 50: (a) Photograph showing a top view of the superprism hard mask layers on a silicon substrate. (b) Microscope image of the corner area of the photonic crystal region shown in Fig 48(a). The defects in the photograph are due to dust particles in the microscope optics that could not be readily removed.

The hexagonal device shape is patterned using photolithography, while the photonic crystal holes are patterned using interference lithography and a tri-layer resist process. After each lithography step, patterns are etched into hard-mask layers via Reactive Ion Etching (RIE). The fully-patterned hard-mask layers are then used to etch the substrate material via another RIE step. Figure 50(a) is a photograph of the patterned hard-mask layers on a silicon substrate. Two hard-mask layers have been used: 50nm chromium on top of 250nm HSQ (spin-on oxide). The chromium layer is patterned with the superprism hexagonal shape, while the open square area is patterned with the ~780nm period photonic crystal in HSQ. The diffraction pattern from the PC can be seen as a blue streak across the square area.

Figure 50(b) shows a microscope image (100x magnification) of the corner region of the photonic crystal area. The square grid of the PC is rotated 45 degrees with respect to the square region. The alignment accuracy between the photonic crystal orientation and the square region is critical for superprism performance. Figure 50(b) shows how a line of PC holes is aligned to the square edge with accuracy of less than one degree, thus, achieving our required tolerance.

Future work will include: calibrating the photonic crystal hole size during the interference lithography, finding a better hard-mask layer than chromium (which leaves behind post-wet-etch residue), and employing reactive ion etching of the silicon substrate material.

Coupling into Photonic Crystal Waveguides

Personnel

S. Assefa, P. Rakich, P. Bienstman, S. G. Johnson, and G. S. Petrich (J. D. Joannopoulos, L. A. Kolodziejski, E. P. Ippen, and H. I. Smith)

Sponsorship

Center for Material Science and Engineering and NSF

Large-scale photonic integrated circuits require a capability of guiding light around sharp bends with a radius of curvature on the order of the wavelength. In conventional index-guided waveguides, light is confined as a result of total internal reflection at the interface between the high-refractive-index waveguiding layer and its low index surroundings. However, conventional high-index-contrast waveguides are susceptible to large optical losses as the bend's radius of curvature decreases. Photonic crystals (PCs), which consist of a periodic arrangement of high and low-index dielectric material, have been proposed as a potential solution for guiding light around corners, including 90^{o} bends, with near perfect transmission.

The 2D photonic crystal consists of an array of cylindrical rods of high-dielectric material above a low dielectric material. Introducing a line defect, such as a row of smaller radius cylinders, into the 2D photonic crystal results in a linear waveguide. The forest of periodic dielectric rods surrounding the line defect creates a Photonic Band Gap (PBG), i.e. a range of frequencies over which light cannot propagate. Thus, an optical signal with a frequency inside the PBG has its energy confined within the line defect and becomes evanescent into the photonic crystal. The radius of the cylinders in the line defect remains large enough to provide index guiding in the third dimension (normal to the plane of periodicity). The localization of a mode inside the line defect can be utilized to guide light around sharp corners. This is illustrated in Figure 51.

The practical use of photonic crystal waveguides is limited due to the poor coupling efficiency between the photonic crystal waveguide, and conventional index-guided input and output waveguides. Coupling poses a challenge because the photonic crystal waveguide exhibits a significantly different mode profile and propagation mechanism compared to traditional waveguides that use index confinement. In the conventional waveguide, the field has only forward propagating components, while the field in the photonic crystal waveguide has both forward and backward propagating components. Furthermore, guiding in the conventional waveguide is in high index surrounded by low index; in the photonic crystal, guiding is in low index surrounded by two photonic crystal "mirrors".

Figure 52 compares three different designs for coupling into the photonic-crystal waveguide. The design in Figure 53(a) suffers from Fabry-Perot reflection at the edges of the photonic crystal region, which makes the transmission of the waveguide dependent on the waveguide length. By tapering the end of input and output index waveguides as shown in Figure 53(b), the reflection can be somewhat reduced. In the third design, the input waveguide is adiabatically converted into a strongly Coupled-Cavity Waveguide (CCW).

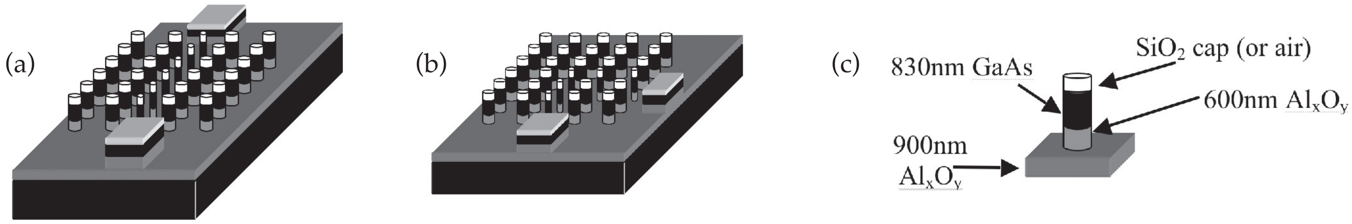
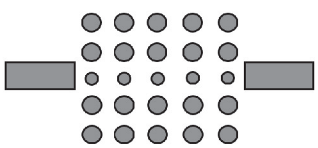


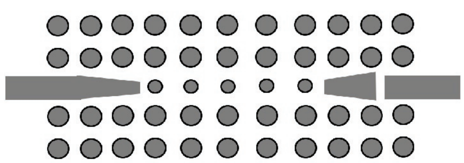
Fig. 51: (a) Schematic of a linear PC waveguide. (b) Schematic of a 90^{o} bend PC waveguide. (c) Schematic of a cylindrical pillar structure. For the bulk photonic crystal, the pillar diameter is 300nm; for the defects, the diameter is 250nm.

continued

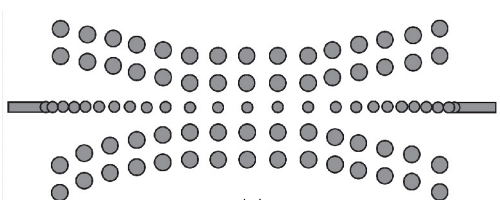
This adiabatically transforms the forward propagating component of the field into both forward and backward propagating components before reaching the photonic crystal. Also, the "cladding" is introduced slowly from the edge, thereby adiabatically transforming the mode from high-index guiding to gap guiding. 2D simulations show that this coupling scheme results in almost 100% transmission through the photonic crystal waveguide.



(a)



(b)



(c)

Fig. 52: a) Schematic of coupling from untapered dielectric waveguide. b) Schematic of coupling from a tapered dielectric waveguide. c) Schematic of adiabatic transition from a dielectric waveguide into strongly coupled cavities and tapered cladding.

The cylindrical rods of the photonic crystal consist of a high-index, 830nm epitaxial GaAs layer sandwiched between 100nm-thick SiO_2 cap layer and a 600nm-thick low-index Al_xO_y layer. An additional 900nm thick Al_xO_y layer is below the cylindrical rods, isolating the GaAs guiding layer from the GaAs substrate. The heterostructure is grown using gas-source molecular-beam epitaxy on a (100) GaAs substrate. The Al_xO_y is initially grown epitaxially as $Al_{0.9}Ga_{0.1}As$ and subsequently, converted (See Figure 52).

The fabrication process commences by sputtering 400nm thick SiO_2 on the sample. Next, the waveguide and photonic crystal are defined using direct-write scanning-electron-beam lithography. Each sample is coated with polymethylmethacrylate (PMMA) electron beam resist, and each cylinder is defined by exposing a square pattern (See Figure 53). The finite width of the beam rounds-off the corners of each square yielding a circular hole upon development. Simulations show that the largest band gap is obtained from a periodic arrangement of rods with diameter of 300nm. Exposure-dose experiments are done to find the optimal parameters for the exposures. A dose of 536 mC/cm^2, current of 250pA, and clock frequency of 0.20 MHz gave hole diameters close to the desired values. The input and output coupling waveguides and different-sized arrays of holes are written by stitching together 250μm fields.

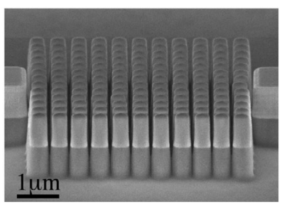
A 50nm-thick nickel film is evaporated on the sample after the PMMA is developed, and a liftoff process is performed. The pattern is transferred to the SiO_2 by Reactive-Ion Etching (RIE) in a CHF_3 plasma after which the nickel mask is removed using nickel etchant. Using the SiO_2 mask, the cylindrical rods are created by etching the GaAs and the AlGaAs to a total depth of 1.5 μm in a BCl_3/He plasma. Experiments were done using various metal masks as an alternative to the SiO_2 mask. However, the metal masks sputtered or degraded during the long duration of the GaAs/AlGaAs etch. Next, each sample is lapped and cleaved in order to create a smooth input facet to promote the efficient coupling of a test signal of 1.55μm wavelength. Finally, the AlGaAs is transformed into Al_xO_y using a wet thermal oxidation process.

continued

continued

Currently, the photonic crystal devices are being tested. The band gap is being mapped first by varying the number of columns in a bulk photonic crystal. Also, the three coupling mechanisms are being compared to confirm the best transmission through the photonic crystal waveguide (See Figure 54).

(a)



(b)

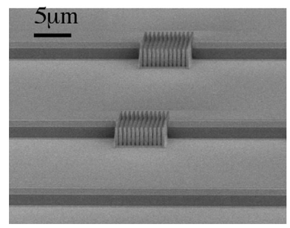
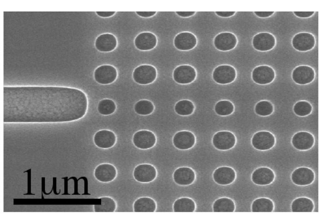
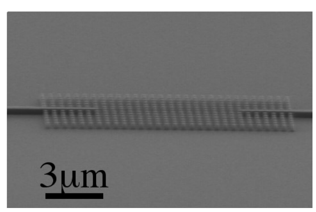


Fig. 53: a) Side view SEM of a bulk photonic crystal etched in GaAs/AlGaAs using BCl_3/He plasma. The AlGaAs is oxidized into Al_xO_y. The period is 500nm and the diameter of the pillars is 300nm. The input and output waveguides are 1.5µm wide. b) Photonic crystal devices on a single chip. The design contains a straight waveguide for normalization purposes.

(a)



(b)



(c)

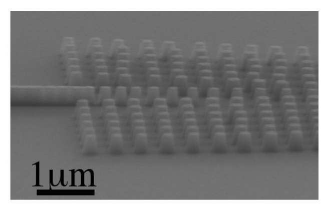


Fig. 54: a) Top view SEM of coupling design from Figure 51(a) after e-beam lithography in PMMA. The bulk photonic crystal has hole diameter of 307nm, while the defect has diameter of 244nm. b) Top view SEM of coupling designs from Figure 51(b) after SiO_2 etch. c) Top view SEM of coupling design from Figure 51(c) after SiO_2 etch.

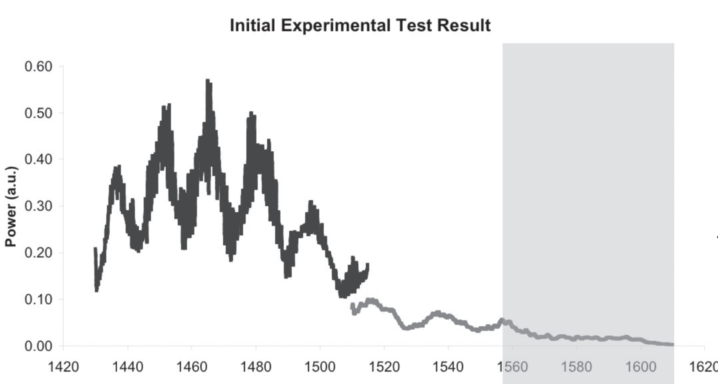


Fig. 55: Initial experimental data of a bulk photonic crystal with 7 columns and 13 rows of dielectric pillars. The darker grey data is for a tunable laser source of 1410nm-1510nm. The lighter grey data is for source wavelength of 1510-1610nm. The shaded region indicates the band gap covered by the tunable range. The band gap extends to 1725nm.

Development of Birefringence-free Ridge Waveguides for Waveguide Isolators

Personnel

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Sponsorship

Walsin-Lihwa Corporation

An optical isolator is a device to transport light in only one direction. They are required in optical communication systems to protect laser sources from reflections. Nowadays, microoptic isolators are available, but they are bulky and require expensive alignment. In contrast, a waveguide isolator which can be integrated with the source and other waveguide devices will be necessary for highly integrated photonics circuit, and may be much cheaper. The goal of this project is to develop an integrated waveguide isolator.
A nonreciprocal polarization rotation is the key to an isolator's performance. Faraday rotation is a well-known nonreciprocal polarization rotation. We have observed Faraday rotation in magnetically doped InP with F=6°/mm, and a loss of α=0.2cm^{-1} at 1550nm.The coupling ratio is calculated as below in a Faraday rotation;

$$R = \frac{F^1}{F^1 + (\Delta\beta/2)^1}$$

where R is the conversion ratio between TE and TM, F is the Faraday constant, and $\Delta\beta = \beta_{TE} - \beta_{TM}$ is the difference of propagation constants between TE and TM. In a waveguide with linear birefringence, the incomplete conversion of TE and TM will limit the polarization rotation to a small angle. Thus, a waveguide is required to have the same propagation constant for both TE and TM in order to have pure nonreciprocal polarization rotation. Linear birefringence arises from various sources including: stress, waveguide geometry, photoelastic effect, etc.

We have developed techniques for fabricating birefringence-free ridge waveguides for integrated waveguide isolators. The waveguides consist of a INGaAsP core layer and cladding layers of magnetically doped InP. Both stress-induced birefringence and photoelastic birefringence are negligibly small. To eliminate the shape birefringence, the ridge waveguide is designed to have a certain width and depth. The calculation of parameters for a birefringence-free waveguide is shown in Figure 56 from a program developed by Mike Watts and Prof. Hermann Haus.

In our process, a high-index-contrast mesa is used. The etched depth is 2.0-2.5μm and the width 1-1.5μm. The etching mask is 100 nm of Ti. The ridge waveguide is etched using reactive ion etching with a mixture of hydrogen and methane. An SEM micrograph of the etched ridge waveguide is shown in Figure 57.

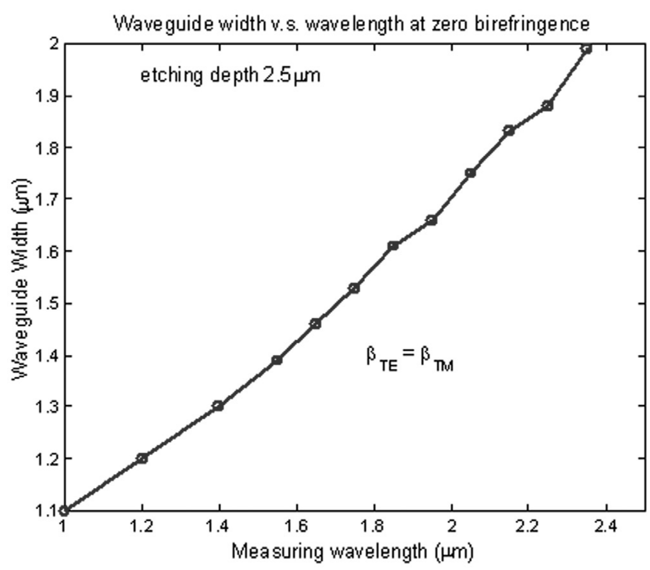

Fig. 56: Calculation of zero birefringence for different waveguide widths and measuring wavelengths (2.5 μm etch depth for all waveguides)

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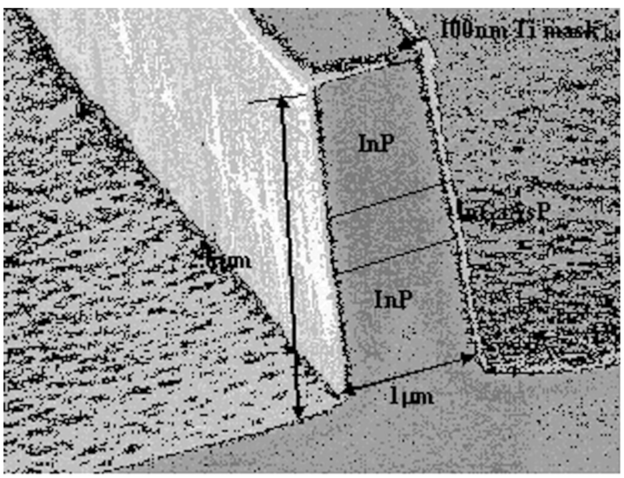

Fig. 57: Scanning-electron micrograph of a RIE etched ridge waveguide