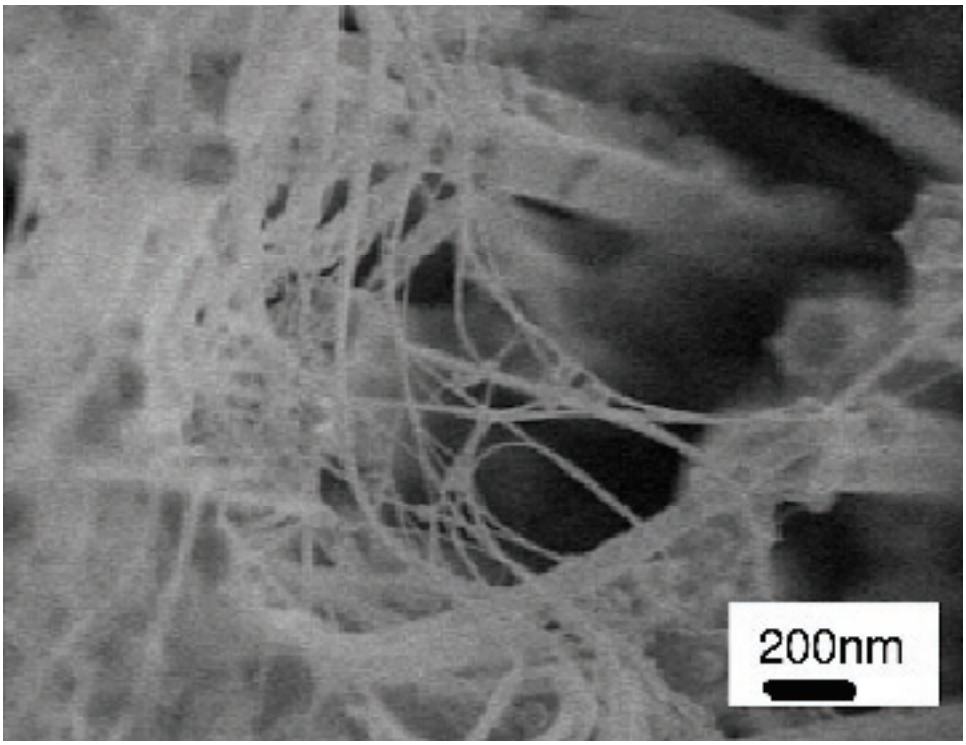
Opposite page:

Gold nano-wires (~20nm) grown by halide reduction in nano-porous alumina template. Template chemically etched to expose nano-wires.

Courtesy of R. Krishnan, R. Tadepalli, and A. Giermann (C.V. Thompson in collaboration. with K. Nielsch, C.A. Ross, and H.I. Smith).

Sponsor:
NSF and MARCO Focused Research Center on Interconnect (MARCO/DARPA)

Materials



Materials

- *Development of Processes and Technologies for Interconnects for 3D Integrated Circuits*
- *Interfacial Electromigration in Cu-Based On-Chip IC Interconnects*
- *Inelastic Deformation of Polycrystalline Films, Lines, and Dots*
- *Yellow-Green Emission for ETS-LEDs and Lasers Based on a Strained–InGaP Quantum Well Heterostructure Grown on a Transparent, Compositionally-Graded InAlGaP Buffer*
- *Ge Photodetectors for Si Microphotonics Circuits*
- *Epitaxial Growth of GaN on Silicon*
- *Integrated Materials Growth System*
- *Capillary Bonding of Nano-Structures*
- *Fabrication and Assembly of Metallic Nano-Wires, Rods, and Dots for Micro- and Nano-Systems*
- *Magnetic and Magnetooptical Films Made by Pulsed Laser Deposition*
- *Magnetic Thin Films*
- *Resonant Gas Sensors*
- *Stress Evolution During Reactive Film Formation*
- *Ferroelectrics for High Strain Actuation*
- *Stress Evolution During Volmer-Weber Growth of Thin Films*
- *Characterization of Electromigration-Induced Failure of Cu-Based IC Interconnect Trees for Circuit-Level Reliability Assessments*

Development of Processes and Technologies for Interconnects for 3D Integrated Circuits

Personnel

R. Tadepalli and R. Krishnan (L. R. Reif, S. M. Spearing, and C. V. Thompson)

Sponsorship

MARCO Focused Research Center on Interconnect (MARCO/DARPA)

The remarkable evolution of semiconductor technology has allowed production of integrated circuits with performance and functionality that have increased exponentially with time, while their cost has decreased exponentially with time. For this evolution to continue into the future, the critical dimensions in Ultra Large-Scale Integrated (ULSI) circuits must continue to shrink. As this happens, system performance will be increasingly dominated by interconnect delay. ICs laid out and fabricated in three dimensions, rather than the traditional two dimensions, can have reduced interconnect delay because of increased flexibility in system design and wiring placement and routing. The flexibility to place devices along the vertical dimension allows layout of circuits with higher device densities and reduced total interconnect lengths.

Wafer bonding is an attractive route to the fabrication of 3-D ICs. In this approach, previously processed device layers are bonded using metal-metal bonds that also serve as layer-to-layer interconnects. Evaluation of bond quality and reliability is critical to the implementation of wafer-bonded 3-D IC technology. Towards this end, we have developed techniques to measure the toughness of bonded copper interconnects. Bond toughness measurements were used to optimize the bonding process. High quality Cu-Cu bonds were fabricated at a low bonding temperature of 300 ^{0}C using a novel cleaning procedure.

A four-point bend technique has been employed to measure the toughness of Cu-Cu bonds. Cu line structures that were patterned on oxidized silicon wafers were thermo-compression-bonded in the EV501 bond chamber and then tested for bond toughness. The bonding temperature, chamber ambient, and the pre-bonding clean procedures were varied to identify the optimized bonding route.

The results from mechanical testing are summarized in Figure 1. While toughness was found to increase monotonically with increasing bonding temperature, there is an obvious dependence of bond toughness on the cleaning methods and chamber ambient. A reducing gas (5% H_2, 95% Ar) ambient improved the toughness and uniformity of Cu-Cu bonds. Best results were obtained by combining a glacial acetic acid pre-bond clean with a reducing gas chamber ambient, as is evident from the graph. A significant point of interest is that bonds created at 300 ^{0}C were comparable (17J/m^2) to industry-standard bonded SOI wafers (10J/m^2) in terms of toughness values. This favorable comparison accentuates the superior quality of bonds created at a low-k dielectric-compatible temperature of 300 ^{0}C. Poor chamber vacuum conditions limit the ability to maintain ultra-clean Cu surfaces, thereby, limiting the quality of bonds. *In-situ* cleaning procedures would, however, provide a solution to this bottleneck.

Having developed a robust technique to evaluate bond quality, we are now fabricating test structures to study bond reliability. These electrical/mechanical structures will allow us to study statistical bond toughness variations. Critical fabrication steps are: deep reactive ion etching to create through-wafer vias, electrodeposition for via filling, and CMP of Cu plated structures.

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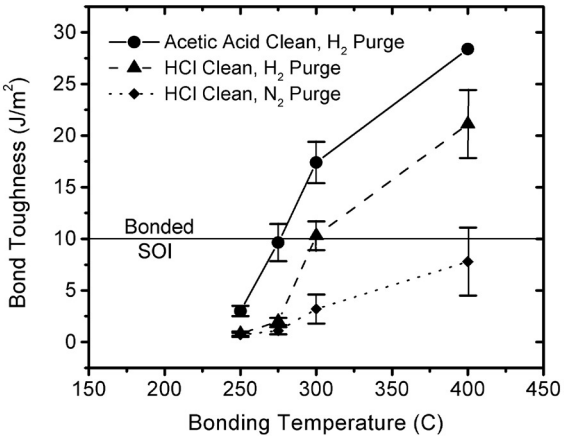

Fig. 1: Variation of bond toughness for wafers 0.4MPa thermo-compression bonded using 300nm-thick Cu films at different temperatures, after different surface preparations. Wafers bonded after an acetic acid pre-clean had higher bond toughness than bonded SOI wafers, even when bonded at temperatures below 300C. The point indicated by an '' is a lower bound.*

Interfacial Electromigration in Cu-Based On-Chip IC Interconnects

Personnel
Z. S. Choi, H. Verma, F. Wei, C. L. Gan, K. L. Pey, W. K. Choi, and R. Augur (C. V. Thompson)

Sponsorship
Intel Corp., SRC, and SMA

Electromigration in polycrystalline Al-based interconnects is known to preferentially occur along grain boundaries. This leads to a very strong dependence of the reliability of Al-based interconnects on their grain structure, with interconnects with bamboo grain structures having reliabilities orders of magnitude higher than interconnects with polygranular grain structures. The factors relating grain structures to the reliability of Al-based interconnects, and relating processing conditions to grain structures, are relatively well understood.

With the move to lower resistance Cu-based interconnects, it has become clear that the role of grain structures in determining reliability has become fundamentally different. Grain boundaries no longer provide preferred high-diffusivity paths for electromigration. Instead, the interfaces between Cu and the surrounding diffusion barriers provide higher diffusivity paths. This is a consequence of the relatively high diffusivity at these interfaces in current Cu technology, rather than due to relatively low diffusivities in Cu grain boundaries. The barrier-Cu interfaces also appear to be sites for relatively easy stress-induced void formation, and for rapid electromigration-induced void growth. It appears that the interface between Cu and the interlevel diffusion barrier (typically SiN in current technology) is an especially easy site for void nucleation and growth, as well as a path for relatively rapid electromigration.

We have developed several test structures for experimental characterization of interfacial electromigration in Cu. One structure, a 'drift structure', consists of Cu lines patterned along the length of a continuous underlying Ta line (See Figure 2). When current is passed through the Ta line, it shunts into the lower resistance Cu segments, when possible. At sufficiently high currents, this causes electromigration that leads the Cu to accumulate at the anode end of the segments and deplete at the cathode end, resulting in a 'drift' of the

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continued

Cu segments (See Figure 2b). Measuring the current density at which drift begins, as a function of segment length, as well as the rate of drift as a function of the current density, provides important information about interfacial electromigration. We are acquiring this information from drift structures that are not covered with a passivating layer, as well as structures with passivating layers (e.g., SiN) (See Figure 2c), to investigate the effects of passivation layers on the stress required to initiate drift, as well as the drift velocity and its scaling with current density.

In a different set of experiments, we are using via-to-via test lines in a second layer of metallization, with connecting lines and pads in the first layer of metallization, to characterize drift in fully-processed dual-damascene structures provided by Sematech International. In addition to providing fully processed structures, Sematech has also provided samples that have been processed through chemical mechanical polishing of the second level of metallization. We have developed a process within MIT that allows us to complete the fabrication of test structures. This, in turn, allows us to investigate the effects of different interlevel diffusion barriers on top of the Cu test lines, as well as the effects of different surface treatments. Experiments of both types are underway.

In a related study we have characterized electromigration drift in fully processed via-to-via test structures of the type shown in Figure 3, as well as in similar structures in which the test line is in the first layer of metallization (M1). In both types of structures, we observed that in a significant fraction of the test population, the resistance of the lines increased steadily over time, prior to failure. We postulate that this gradual resistance increase results from void growth and that the rate of resistance increase correlates with the electromigration drift velocity (See Figure 4). The values of the electromigration drift velocities determined in M2 lines were similar to those measured in M1 lines, though there was a broader range of variation in the former case. The larger variation is correlated with the larger range of void shapes and sizes in M2-type structures. Given that the stress for void nucleation should be the same, the observation that the rate of void growth is the same supports our earlier proposal that the asymmetry in reliability in these two different configurations is associated with differences in the void sizes required to cause failure.

Using the interfacial electromigration test structures described above, we also plan to investigate the effects of grain structures and grain orientations on interfacial electromigration. To do this we will use Scanned Laser Annealing (SLA) of Cu lines to produce long-grained-bamboo or near-single-crystal Cu interconnects for electromigration testing. This will allow characterization of electromigration and electromigration-induced voiding for single-via and multi-via structures that contact single Cu grains or crystals.

In earlier work in our group, Scanned Laser Annealing (SLA) was developed as a means of modifying and controlling the grain structures of polycrystalline interconnects. In this technique, a laser spot is scanned along the length of an interconnect, to create a moving hot zone in which grain boundary mobilities are significantly increased over those of boundaries in unheated regions (See Figure 5). This leads to a grain growth in the hot zone, and as the zone is scanned, grain boundary motion is caused to occur preferentially and specifically in the direction of zone motion. This technique can be used to produce bamboo grain structures in lines that would not develop bamboo grain structures in conventional anneals. Furthermore, the grain sizes obtained from scanned laser annealing can be significantly longer than those obtained from conventional annealing. Lines with bamboo grain sizes as long as 10μm were produced by scanned laser annealing of 0.5μm-wide Cu lines.

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continued

Modeling of the SLA process suggests that still longer bamboo grains can be obtained under the proper conditions. In ongoing research, we will investigate this possibility. We will also use SLA to produce large-grained structures in the dual-damascene drift structures described above. With Cu interconnects having 10μm-long grains or longer, contacted at either end with single vias, most vias will contact a single grain. By analyzing SLA grain structures before completing the processing of the electromigration test structures, we hope to assess the effect of grain crystallographic orientation on interfacial electromigration. The results will be used to develop models for interfacial electromigration in Cu interconnects that account for the effects of crystallographic orientations.

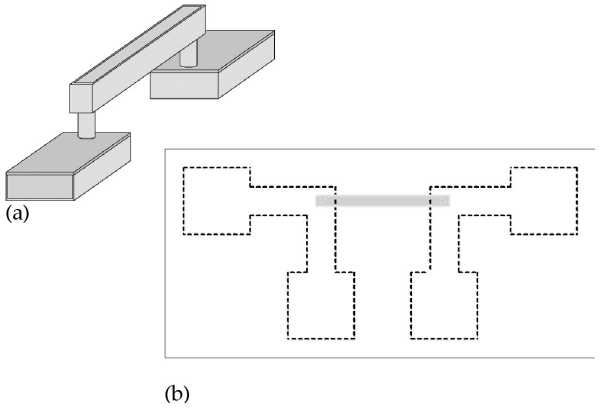

Fig. 3: A second structure for characterization of interfacial electromigration of Cu. A via-to via metal 2 test line connected to larger metal 1 lines, connected to bond pads. (a) Conventional dual-damascene processing through CMP of metal 2 is carried out at Sematech. Metal 2 surface treatment and passivation, and the rest of the test structure processing, are carried out at MIT.

Fig. 4: Void growth causes a gradual resistance increase during elec-

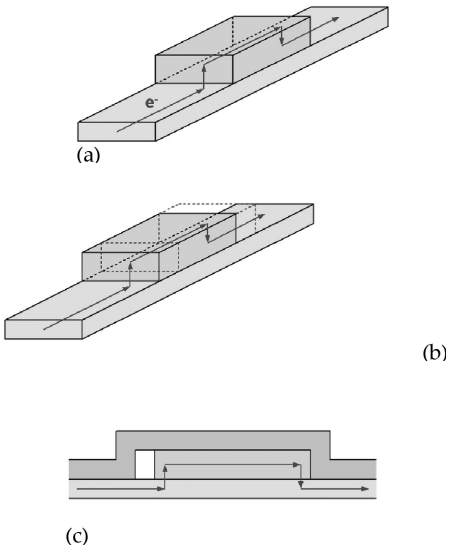

Fig. 2: Drift test structure for characterization of interfacial electromigration of Cu. (a) Cu segments are patterned on continuous Ta underlying lines. (b) Current shunts into the lower resistance Cu segment and causes it to drift. (c) Passivation will affect the rate and character of drift.

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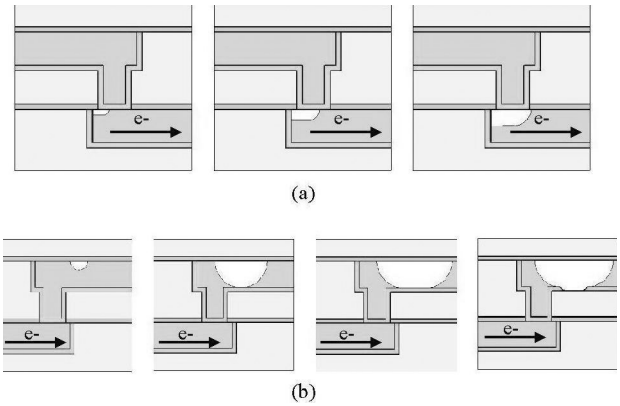

tromigration tests in (a) M1-type test structures and in (b) M2-type structures.

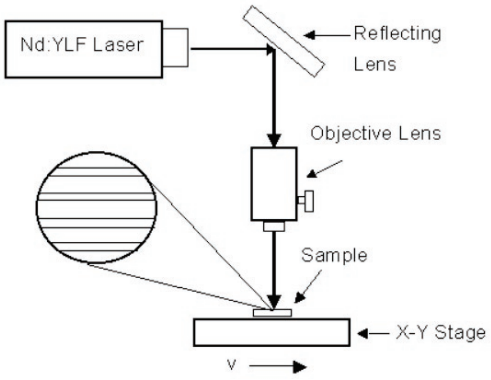

Fig. 5: An apparatus for scanned laser annealing (SLA) of Cu interconnects.

Figure 5: The grain structures that result from SLA depend on the

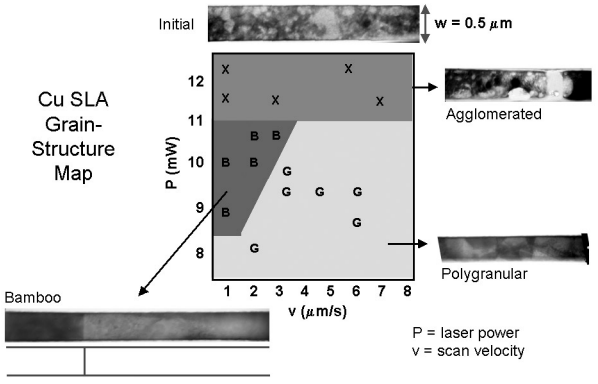

Fig. 6: The grain structures that result from SLA depend on the laser power and the scan velocity. Long-grained bamboo structures are obtained at intermediate powers and low velocities.

continued

Inelastic Deformation of Polycrystalline Films, Lines, and Dots

Personnel
R. Bernstein (C. V. Thompson)

Sponsorship
NSF and CMI

In earlier studies, we have characterized inelastic deformation of polycrystalline metallic films using *in-situ* Transmission Electron Microscopy (TEM), and *ex-situ* substrate curvature measurements during heating, cooling, and isothermal anneals. *In-situ* TEM studies were made possible through the use of micromachined silicon membranes. We have demonstrated that uncapped Ag and Cu films undergo rapid diffusional creep at temperatures as low as 0.25Tm, where Tm is the melting temperature in degrees Kelvin. At these temperatures, creep rapidly decreases with decreasing film thickness. This can lead to a decrease in the flow stress observed at room temperature as the film thickness is decreased. We have also demonstrated that dislocation-mediated plasticity dominates in capped films, or in uncapped films that are thicker or deformed at lower temperatures. We have shown that dislocation-mediated plasticity is thermally activated and controlled by pinning due to obstacles whose spacing is small compared to film thickness and grain size. This leads to the high flow stresses often observed in capped thin films. We have seen similar effects to those described above in Cu films patterned into lines through a damascene process. This work demonstrates that the inelastic properties of polycrystalline metallic films depend strongly on the film dimension, the surface condition of the film, and temperature.

We are currently investigating the use of micromachined cantilevers for isothermal studies of deformation of thin films and films patterned into dots. These cantilevers can be deflected at a set temperature, and the relaxation at that temperature can be studied. The deflection of the cantilevers can be measured with very high resolution (of order nm) using an optical profilometer at fairly high sampling rates (up to once every five seconds).

Yellow-Green Emission for ETS-LEDs and Lasers Based on a Strained–InGaP Quantum Well Heterostructure Grown on a Transparent, Compositionally-Graded InAlGaP Buffer

Personnel

L. McGill and J. Wu (E.A. Fitzgerald)

Sponsorship

NSF GOALI Program and ARO Program

Epitaxial-transparent-substrate light emitting diodes with a primary emission peak at 590nm and a secondary peak at 560nm have been fabricated in the indium aluminum gallium phosphide (InAlGaP) system. The active layer consists of an undoped, compressively strained indium gallium phosphide (InGaP) quantum well on a transparent $In_{0.22}(Al_{0.2}Ga_{0.8})_{0.78}P/\nabla_x[In_x(Al_{0.2}Ga_{0.8})_{1-x}P]/GaP$ virtual substrate. Light emitting diodes have been fabricated utilizing simple top and bottom contacts. The highest LED power of 0.18μW per facet at 20mA was observed for a quantum well composition of $In_{0.32}Ga_{0.68}P$ and a bulk threading dislocation density on the order of $7x10^6$ cm^{-2}. The spectrum of this device was composed of two peaks: a weak peak at the predicted 560nm wavelength and a stronger peak at 590nm. Based upon superspots present in electron diffraction from the quantum well region, we believe that the observed spectrum is the result of emission from ordered and disordered domains in the active region (See Figure 7). The same device structure grown with a bulk threading dislocation density on the order of $5x10^7$ cm^{-2} exhibited an identical spectral shape with a reduced power of 0.08μW per facet at 20mA. For a quantum well composition of $In_{0.37}Ga_{0.63}P$ and an overall threading dislocation density on the order of $5x10^7$ cm^{-2}, a single peak wavelength of 588nm with a power of 0.06μW per facet at 20mA was observed.

Work in the near future will focus on improving electrical characteristics and reducing the bulk threading dislocation density in the devices in order to maximize efficiency and brightness. We must suppress ordering in the quantum well in order to recover the observed 560nm emission as the peak wavelength of devices with a quantum well composition of $In_{0.32}Ga_{0.68}P$. Perhaps the fundamental factor limiting the development of high-brightness green LEDs in the InAlGaP system is the direct bandgap-to-indirect bandgap crossover problem. We believe that confinement within the quantum well active region, in conjunction with increased extraction due to the transparent substrate, will compensate for the reduction in internal efficiency expected at the compositions of interest for green LEDs, allowing for the production of a bright device. Ultimately, we hope to improve the overall material quality and design of these devices to the extent that they are a viable option both for high-brightness yellow and green LEDs and for yellow lasers.

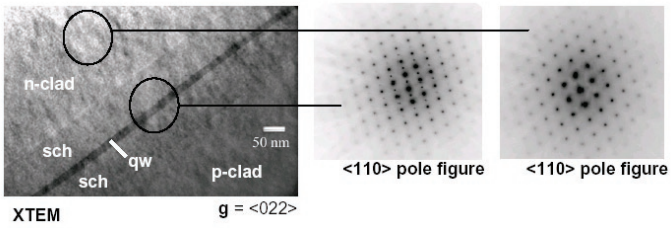

Fig. 7: X-TEM of device structure with an $In_{0.32}Ga_{0.68}P$ quantum well. Electron diffraction of the quantum well (center) shows ordering superspots, while the clad (right) does not.

continued

Ge Photodetectors for Si Microphotonics Circuits

Personnel

D. Cannon, D. T. Danielson, J. Liu, S. Jongthammanurak, A. Eshed, K. Wada, and J. Michel (L. C. Kimerling)

Sponsorship

Pirelli Labs and Analog Devices, Inc.

Epitaxially grown Ge on Si is a promising technology with significant technological applications. Because the direct bandgap of Ge is 0.8eV, it is highly absorbing at optical communications wavelengths. Because Ge is also compatible with existing Si technology, it offers the potential for high quality CMOS compatible integrated photoreceivers.

Current research is focused on increasing our fundamental understanding of epitaxial Ge growth and the influence of processing conditions on the film quality and properties. We have recently demonstrated the ability to decrease the direct transition energy of Ge films, thus extending the useful wavelength range for photoreceivers to longer wavelengths.

This transition energy reduction is achieved by increasing the biaxial strain in the film (See Figure 8). Deformation potential theory predicts a reduction in the direct transition energy of Ge with increasing biaxial strain. By varying the growth temperature, we are able to control the amount of residual strain in the films induced upon cooling to room temperature. Post growth annealing treatments are also effective in controlling strain. Our experimental results agree well with theoretical predictions.

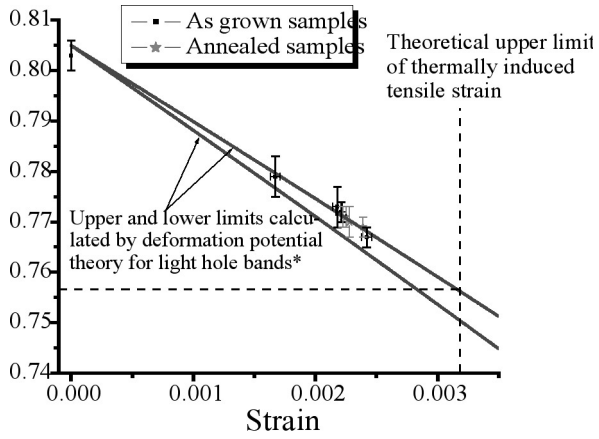

Fig. 8: Direct Ge bandgap vs. strain for several different as grown and annealed samples.

We have also demonstrated high quality selective growth of Ge mesas on Si substrates with a patterned SiO_2 layer (See Figure 9). Because Ge will not deposit from the gas phase onto SiO_2, film growth will only occur on those areas where the Si substrate is exposed. Because of the special cleaning and surface passivation procedures required for epitaxial Ge growth on Si, achieving high-quality, high-yield mesas is a significant accomplishment.

Selectively grown mesas are important, because they offer the potential for even higher quality Ge than for bulk films. Post-growth cyclic annealing of films reduces the dislocation density by two orders of magnitude in bulk films. In mesas, threading dislocations can glide to the edge of the mesa, where they leave the film. This allows for the potential of completely dislocation free mesas.

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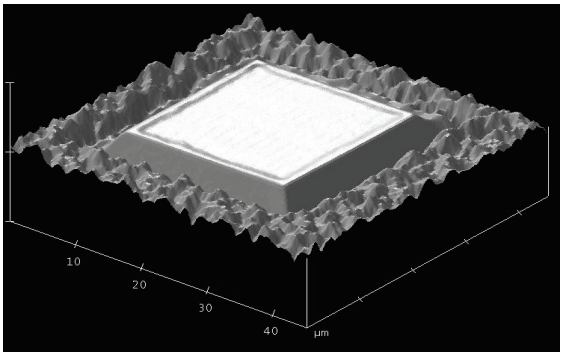

Fig. 9: AFM image of a selectively grown Ge mesa.

Epitaxial Growth of GaN on Silicon

Personnel
K. Zang and S. J. Chua (C. V. Thompson)

Sponsorship
SMA

GaN can be used for high power and high efficiency photonic devices. There is great interest in the possibility of monolithic integration of GaN and silicon for multi-chip optical communication and other applications. However, GaN and silicon have a lattice mismatch of 17%, which makes heteroepitaxial growth of low-defect-density GaN films on silicon difficult. We are investigating structure and stress evolution during the heteroepitaxial growth of GaN films on patterned silicon surfaces, and on silicon surfaces with different crystallographic orientations. We are also investigating the effects of changes in growth temperature or thermal variations during growth, as well as the use of surfactants and changes in film stoichiometry during growth. Our goal is to develop new techniques for monolithic integration of high performance GaN devices on silicon.

Integrated Materials Growth System

Personnel

S. Coe, C. Madigan, D. E. Mascaro, S. H. Kang, and J. Tischler (V. Bulovic)

Sponsorship

Defense University Research Instrumentation Program (DURIP) - Air Force Office of Scientific Research, and
NSF Center for Materials Science and Engineering SEED Grant

Vacuum growth of organic materials can generate atomically flat thin films of high purity, facilitating fabrication of complex multi-layer devices with excellent uniformity and sharp interfaces between adjacent layers. Such vacuum grown devices are highly reproducible from run to run, and can have complex structures containing thin layers of precisely controlled composition. Increased control over the growth parameter is essential for the better performance devices. Additionally, flexibility of van der Waal bonds in the organic thin films facilitate their integration with both conventional technologies and less conventional materials such as flexible, self-assembled, or conformable substrates.

We are in the process of developing a versatile materials growth system (See Figure 10) that combines conventional materials growth techniques with novel deposition methods developed in our laboratories. The completed growth system will integrate the method for physical and vapor phase deposition of hybrid organic/inorganic thin-films with a low-pressure RF/DC sputtering chamber, an evaporative growth chamber, and a chemical vapor deposition chamber. The completed vacuum system will be capable of depositing molecular organics, polymers, metals, metal oxides, inorganic nanodots, and colloids in a controlled layer-by-layer fashion. An *in-situ* shadow masking system enables fabrication of complex patterned structures inside a vacuum environment, while the integrated N_2-filled, dry glove box facilitates handling, measuring, and packaging of organic thin film samples that are susceptible to reactions with atmospheric oxygen and water vapor. When the analysis chamber is built, the completed samples will be in-situ tested by contacting them with an electrical probe attached to an X-Y-Z manipulator. Optical ports on the analysis chamber allow for a telescopic view of the devices and facilitate optical excitation of probed samples. Optoelectronic properties of the hybrid materials and structures will be investigated at a range of temperatures form 5 K to 600 K, generated by the liquid helium cryostat and the boron-nitride heater situated behind the sample stage. Existing chambers are presently connected to the central transfer system that has linear degrees of freedom. Maximum substrate size is 10 cm with a 5% variation in the thickness and composition of deposited films over the substrate area. The integrated growth system is the centerpiece of our materials growth effort, as in its completed form it will accommodate solvent-free deposition and co-deposition of polymers, colloids, and molecular organic materials in vacuum. Its versatility is unsurpassed in the field of organic/inorganic materials deposition, and it is among the first to integrate organic and inorganic material deposition methods.

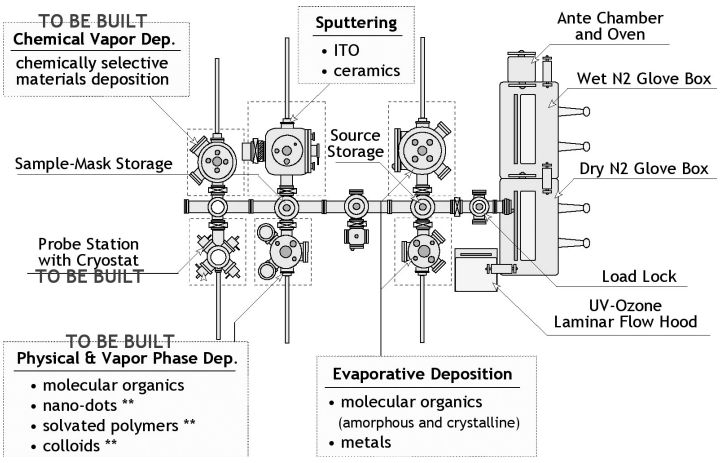

Fig. 10: Integrated Materials Growth System. Both present and projected chambers are indicated. Projected chambers and chambers in construction are labeled as "TO BE BUILT".

Capillary Bonding of Nano-Structures

Personnel

A. R. Takahashi, R. Tadepalli, S. C. Seel, N. Q. Hung, and M. Yeadon (C.V. Thompson)

Sponsorship

NSF and SMA

When small objects come into contact, capillary forces can lead to bonding that occurs at a rapid rate without atomic diffusion. Capillary bonding of curved surfaces can lead to elastic and inelastic deformation. This is most likely to occur when objects are very small (i.e., have high surface to volume ratios) because capillary forces scale with area, and the energy required for deformation scales with volume. We are studying the effects of capillary bonding through experiments on stress evolution during film formation. We are also developing both finite element models and molecular dynamics simulations of capillary bonding.

As discussed in detail in another section, during thin film formation through the Volmer-Weber mechanism, crystalline islands nucleate and grow to impinge and coalesce to form continuous films. When islands first come into contact, grain boundary formation can proceed from the point of contact (See igure 11), and leads to the reduction of the high-energy surface area of both coalescing islands. For small islands, with high surface-to-volume ratios, the energy-per-unit-volume released due to the replacement of two surfaces by one lower-energy grain boundary can be very high. The fastest way for this process to occur is for the islands to strain to close the gap between them, as the grain boundary 'zips' up from the substrate surface. The strain energy that can be accommodated is balanced by the accompanying surface energy reduction.

We have analyzed the zipping process using finite element models and molecular dynamics simulations. Finite element models have been used to calculate the strain energy as a function of zipping distance, z_0. The total energy associated with zipping (the strain energy plus the grain boundary energy, minus the energy of the replaced surfaces) is calculated and the zipping distance that minimizes the total energy is determined. The stress associated with the energy-minimizing zipping is then calculated. This allows calculation of the stress as a function of the size of the coalescing islands and leads to predicted stresses that are in better agreement with experimental observations than analytic models developed by others. Finite element analyses have been combined with simulations of island nucleation and growth to predict the average stress as a function of the mass-equivalent thickness. These calculations are quantitatively consistent with experimental observations for Ag films deposited on oxidized silicon. We have also modified finite element calculations to account for the effects of variable traction at the island-substrate interface, for different island-substrate contact angles up to 90 degrees (See Figure 12), and for coalescence of islands with different sizes.

Molecular dynamics simulations of the zipping process have also been conducted. So far, only islands bound to substrates *without* interface traction have been investigated. Islands composed of up to 5876 Ag atoms have been modeled using embedded atom potentials. Island-substrate interactions are modeled using a Leonard-Jones potential. We find that grain boundary formation occurs over time scales that are accessible through MD simulations, in that zipping occurs at very high rates. The observed zipping height is consistent with the results of finite element modeling, suggesting that the physical model on which the finite element calculations are based, grain boundary formation through island straining, is valid. Additional simulations have shown that the zipping height does indeed increase with increasing cluster size (See Figure 13), in qualitative agreement with continuum models.

We are further developing molecular dynamics simulations that will account for traction at the island-substrate interface. We also plan to conduct experiments involving in-situ Transmission Electron Microscope (TEM) observations of the early stages of polycrystalline film formation, using micromachined membranes. Through collaboration with Prof. Mark Yeadon of the

continued

Institute for Materials Research and Engineering in Singapore, we have observed deposition of Ni on both SiN membranes and on MgO substrates. More experiments are planned; as well as, more detailed analysis of the available data from earlier experiments.

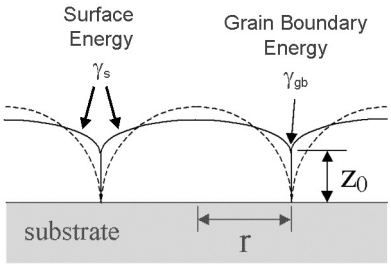

Fig. 11: When islands impinge, grain boundaries form as islands strain to close the gap between them, zipping a distance z_0 to replace two surfaces of energy γ_s with a boundary of energy γ_{gb}.

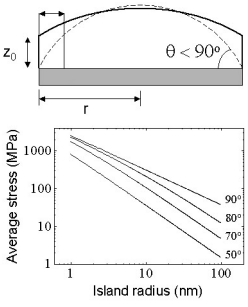

Fig. 12: Effects of the equilibrium island-substrate contact angle on the coalescence stress, as indicated by finite element analyses.

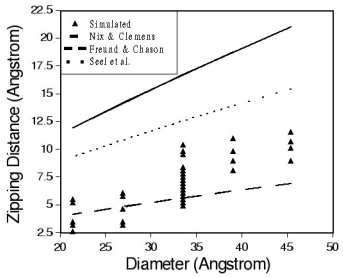

Fig. 13: Comparison of zipping height versus island size based on MD simulations, finite element simulations, and models of Nix and Clemens and Freund and Chason.

Fabrication and Assembly of Metallic Nano-Wires, Rods, and Dots for Micro- and Nano-Systems

Personnel

R. Krishnan, R. Tadepalli, and A. L. Giermann (C. V. Thompson in collaboration with C. Ross, H. I. Smith, and K. Nielsch)

Sponsorship

NSF and MARCO Focused Research Center on Interconnect (MARCO/DARPA)

Metallic nano-wires, rods, and dots can be used in a number of applications in micro- and nano-systems, such as nanowire-interconnects (wires), on-chip magnetic storage devices (rods), on-chip Peltier cooling devices (wires and rods), and plasmonic waveguides (dots). We are developing new methods for fabricating and assembling metallic nano-wires, rods, and dots, for new applications including nano-contacts for devices and interconnects for mixed-material and multifunctional micro- and nano-systems.

We have developed a new templating technique to produce metallic nano-structures on a silicon wafer. Highly ordered alumina nanopores with controlled symmetry have been grown by anodization of aluminum evaporated on lithographically-corrugated silicon surfaces (See Figure 14). We have used ordered porous alumina templates to grow nano-wires of copper and gold (See Figure 15) by electrodeposition and a halide reduction process. While nano-wire growth by electrochemical deposition has been shown previously by others, we have demonstrated for the first time the use of a novel halide reduction process to obtain metallic nano-wires. This technique can be used to obtain a wide range of materials suitable for nano-devices. Our goal is to fabricate nano-wire, rod, and dot arrays with controlled symmetry and spacing and characterize their electrical, mechanical, and thermal properties.

We are also investigating Templated Self-Assembly (TSA) as a route to fabrication of ordered arrays of nano-dots and nano-wires. Templated self-assembly is a self-assembly process on a surface patterned with conventional lithography techniques that leads to long-range periodic structures with a final characteristic length scale that is smaller than that of the initial pattern, thus overcoming the minimum size limitations of standard lithography. Our approach is to create ordered metallic nano-particles by annealing thin films at high temperatures on surfaces with artificial lithographically-defined surface topography. When a polycrystalline film is annealed at high temperatures, the grain boundaries form grooves at the surface. These grooves deepen to intercept the film/substrate interface. Once such voids form, the film proceeds to agglomerate into individual islands, resulting in a field of micro- or nano-particles. In earlier studies, we have characterized this process in films deposited on planar surfaces. We are developing methods to induce these islands to self-align during agglomeration by creating various periodic topographies on substrates. We are also investigating the use of such ordered arrays of nano-particles as catalysts for semiconductor nano-wire growth by the metal-mediated vapor-liquid-solid CVD technique.

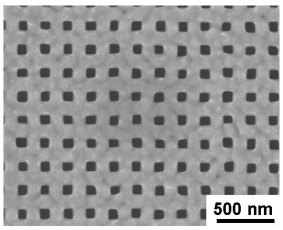

Fig. 14: Anodized alumina template on a Si wafer containing ordered nano-pores. (Pore spacing = 200nm, Pore diameter =80nm)

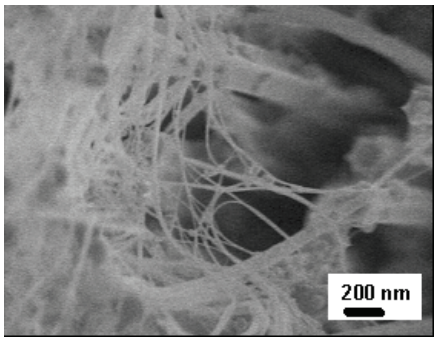

Fig. 15: Gold nano-wires (~20nm) grown by halide reduction in nano-porous alumina template. Template chemically etched to expose nano-wires.

Magnetic and Magnetooptical Films Made by Pulsed Laser Deposition

Personnel

T. Tepper, F. Ilievski, R. Ram, and G. Dionne (C. A. Ross)

Sponsorship

Pirelli and Ferry Fund

We have established a Thin Film Laboratory which includes a Pulsed Laser Deposition (PLD) system and a UHV Sputter/analysis system. In PLD, a high energy excimer laser is used to ablate a target, releasing a plume of material which deposits on a substrate to form a thin film. PLD is particularly useful for making complex materials such as oxides because it preserves the stoichiometry of the target material. We have used PLD to produce films of Cr and CoCrPt alloys to compare with films produced by sputtering, in order to understand the influence of energetic bombardment on the formation of the Cr (200) / CoCrPt (1120) preferred orientation. We have also been using PLD to deposit a variety of oxide films for magnetooptical devices such as isolators. These materials include iron oxide, which can adopt one of three different ferri- or antiferromagnetic structures depending on deposition conditions, and bismuth iron garnet (BIG, $Bi_3Fe_5O_{12}$), which is useful for magnetooptical isolators in photonic devices.

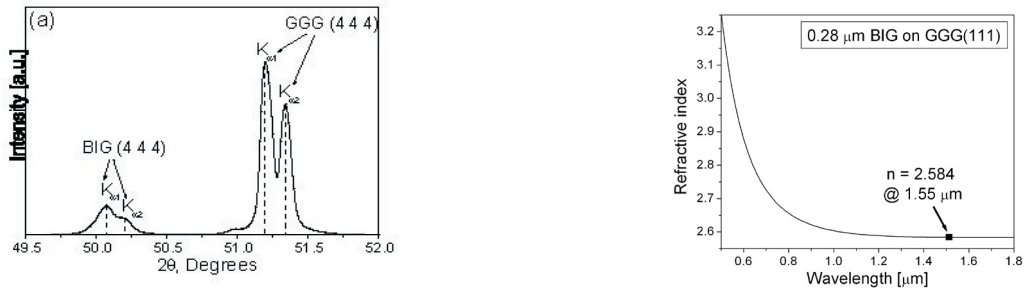

Fig. 16: Left: X-ray diffraction spectra from 300 nm thick BIG film deposited on (111) GGG (gallium gadolinium garnet) single crystal substrate, illustrating epitaxial growth. Right: Refractive index vs wavelength, measured from ellipsometry data, assuming zero absorption, for a 280 nm thick BIG film on (111)GGG.

Fig. 17: Left: XRD spectra of a 420nm maghemite (Fe_20_3) film deposited on a MgO (001) substrate, showing the cube-on-cube film-substrate epitaxial relationship. Right: Faraday rotation measurements of maghemite with different thickness at a wavelength of 645nm showing an average saturation rotation of about 1.9deg/μm.

Magnetic Thin Films

Personnel
C. A. Ross, P. Chambers, M. Shima, E. Lyons, and R. C. O'Handley

Sponsorship
NSF

Magnetic CoCrPtTa films on a Cr underlayer are used in hard disks to store data. The films are deposited at temperatures of 200˚C or above, which causes the b.c.c. Cr to grow with a (200) crystallographic texture. The hexagonal Co-alloy grows epitaxially on the Cr with a (11.0) texture, putting its c-axis parallel to the film plane. In such films, the presence of substrate roughness has significant effects on in-plane magnetic anisotropy. In particular, the presence of grooves or scratches in the substrate causes the coercivity, remanence and squareness of the film to be considerably higher parallel to the grooves compared to their values in the perpendicular direction. This effect is useful in hard disks, but the physical origin of this anisotropy is still debated.

We have measured the anisotropy in films deposited onto oxidised silicon substrates with well-controlled submicron surface topography, to explore the origins of the effect and to demonstrate how it can be enhanced by choice of substrate features. Substrates are patterned with shallow, parallel grooves, then coated with Cr/CoCrPt films. Both the stress in the films, and the preferred c-axis orientation, have been characterized. We find that magnetostrictive effects, due to the biaxial stress state of the Co-alloy films, account for about 1/4 of the measured anisotropy. The majority of the anisotropy, however, is caused by a preference for the Co c-axes to lie parallel to the grooves. This is thought to be a result of preferential nucleation of certain Co variants on the biaxially-strained Cr.

We have also been investigating the nucleation and growth of these Co and Cr films, to help understand their morphology and to control grain size for high-density media. This has been done by comparing films grown using pulsed laser deposition to those grown by sputtering under a range of conditions such as base pressure. The wide range in available processing parameters allows the importance of factors such as substrate bombardment and surface mobility to be investigated.

Another project involves the influence of strain in the magnetic anisotropy of Ni films grown epitaxially onto Cu. The lattice mismatch leads to in-plane strain which influences the anisotropy in the Ni, leading in some cases to a perpendicular anisotropy. By patterning the films into narrow lines, we are exploring how the relaxation of stress can influence the net anisotropy in the Ni nanostructures.

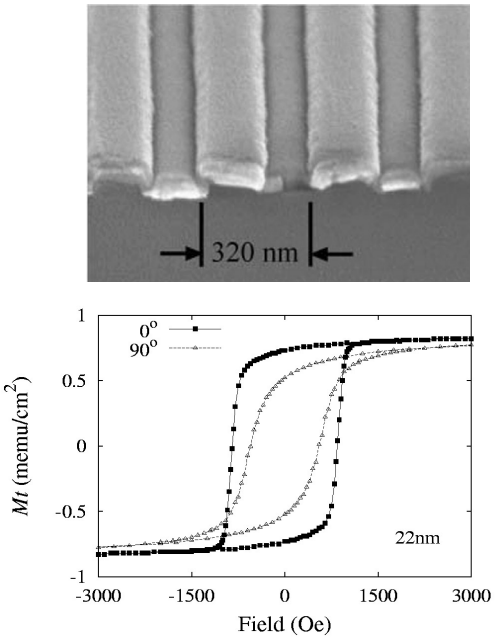

Fig. 18: Top: Example of a film sputtered over a substrate with 320 nm period grooves. Bottom: Magnetic hysteresis loops from a sample of Cr/CoCrPt sputtered onto a substrate with 200 nm period, 22 nm deep grooves. Coercivity, remanence and squareness are higher parallel to the grooves (filled symbols) compared to perpendicular to the grooves (open symbols).

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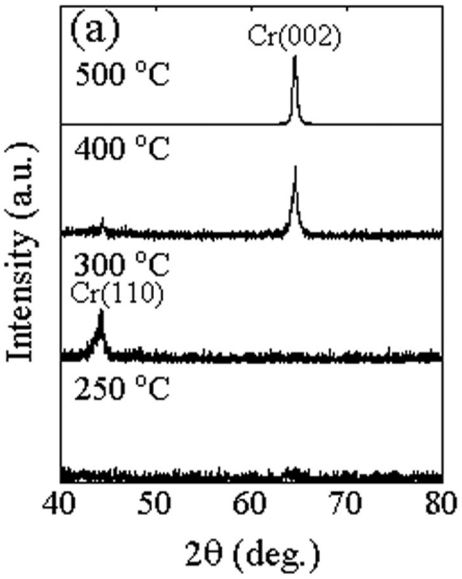

Fig. 19: Cr grown on Si by PLD. As the substrate temperature increases, the texture of the Cr changes from (110) to (200). A similar effect is seen in sputtered Cr films used in hard disks.

Resonant Gas Sensors

Personnel
H. Seh and H. Fritze (H. L. Tuller)

Sponsorship
NSF and DAAD

Langasite ($La_3Ga_5SiO_{14}$) exhibits piezoelectric properties comparable to quartz, but undergoes no phase transition below its melting temperature (1470°C), making it of interest as a potential gas sensor platform for high temperature operation. Measurements with TiO_2 films demonstrate strong sensitivity to hydrogen gas. As part of the evaluation of this material, the electrical conductivity and the electromechanical characteristics are being examined as functions of temperature and oxygen partial pressure and models are being developed which provide guidance for device optimization.

Stress Evolution During Reactive Film Formation

Personnel
K.-P. Liew, R. Bernstein, M. Yeadon, and Y. Li
(C. V. Thompson)

Sponsorship
Singapore-MIT Alliance (SMA)

Reactive film formation is widely used in the processing of micro- and nano-devices. Common examples include oxidation of silicon and formation of metal silicides through reactions between metallic films and silicon. The latter is an example of solid-state reactive film formation. During reactive film formation, the molar or atomic volume of the substrate material is significantly changed as it is incorporated into the reaction product. This volume change should lead to a large stress that would affect both the reaction rate and the stress state of the reaction product. The stress generated during reactive film formation may also affect what phase forms as a reaction product. We have studied stress evolution during reactive formation of nickel silicide films, using substrate curvature measurements. We find that the stress generated during reactions is partially relieved through mechanical relaxation, *as* the reaction proceeds. We have independently characterized the rates of stress generation and stress relaxation as a function of temperature, in order to better understand the stress conditions at the reacting interface. This allows determination of a lower bound for the instantaneous stress generated at the interface where the reaction is occurring. This was found to be 2 GPa in the case of nickel silicide formation.

Ferroelectrics for High Strain Actuation

Personnel
Y. Avrahami (H. L. Tuller)

Sponsorship
MIT Microphotonics Center

Perovskite and related oxide systems are being explored as potential candidates for high strain actuators with good thermal stability and low hysteresis and as electro-optic modulators. Several techniques are investigated for the preparation of polycrystalline, single crystalline and thin films materials. Integration into microphotonic devices is examined with emphasis on MEMS structures and electro-optic modulators. The integration of these ferroelectric films on silicon is investigated. The work is being performed in conjunction with a multidisciplinary group that is working on the integration of microphotonic devices onto silicon wafers.

Stress Evolution During Volmer-Weber Growth of Thin Films

Personnel
C. Friesen, A. R. Takahashi, and S. C. Seel (C. V. Thompson)

Sponsorship
NSF and SMA

The earliest stages of thin film formation have a profound effect on the evolution of film structures, and ultimately on the properties of films used in micro- and nano-systems. In most circumstances, epitaxial and polycrystalline (and perhaps amorphous) films grow through a Volmer-Weber mechanism, in which adsorbed atoms (adatoms) form stable clusters through a stochastic nucleation process. These clusters grow as islands on the substrate surface, eventually impinging and coalescing to form continuous films. During these processes, very high forces on the substrate can result in large residual stresses in the as-grown films. We have developed several new methods for making highly-sensitive stress measurements during Volmer-Weber growth of thin films, and used them to characterize adatom and island dynamics before, during, and after island coalescence. We are also developing simulations of adatom-substrate interactions and island coalescence processes.

We have developed several new techniques for measuring forces associated with growing films. One is a microelectromechanical device with which stresses in single crystal cantilever substrates are measured through piezoresistance measurements (described in more detail in another section). A second device allows

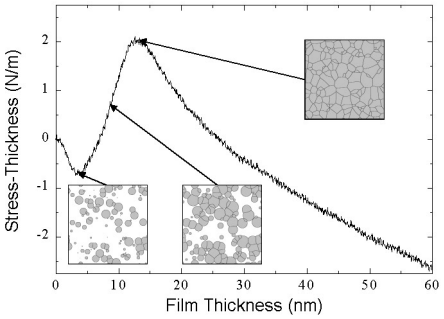

Fig. 20: Stress-thickness product measured during deposition of a Cu film. The stress is compressive as islands nucleate and grow, becomes tensile as islands coalesce, reaching a maximum when the film is continuous, and becomes compressive at higher thicknesses.

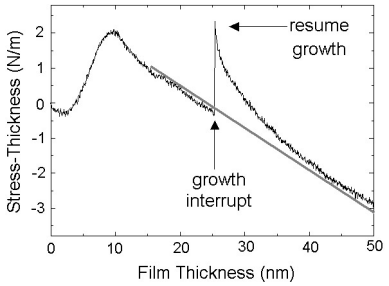

Fig. 21: Interruption of post-coalescence growth leads to a reversibly relaxed stress.

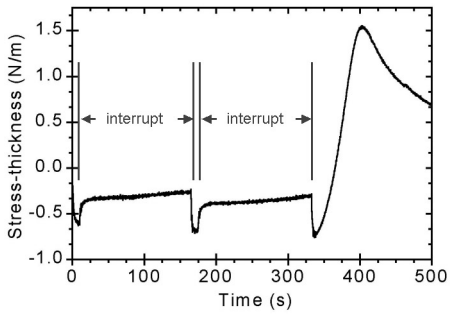

Fig. 22: Interruptions in pre-coalescence growth also leads to a reversibly relaxed stress.

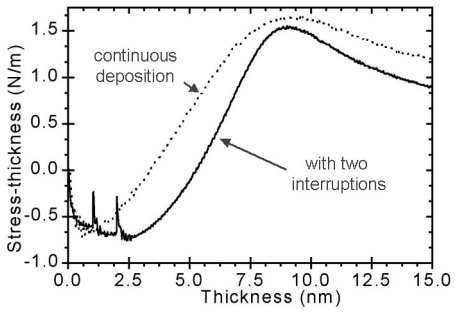

Fig. 23: The onset of coalescence occurs at a higher film thicknesses when growth is interrupted, presumably due to island coarsening during the interruptions.

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measurement of the deflection of the tip of a cantilever substrate by measuring the displacement of a laser beam reflected from the cantilever tip onto a diode detector pair. By placing both the laser and detectors in pressure vessels and assembling all components of this system on a rigid frame that is immersed completely in the deposition system, tip displacements of a few nanometers can be measured. The third device is also a cantilever-curvature based stress monitor and functions by measuring the changes in capacitance between the cantilever and sensor. Tip deflection can be measured with nanometer scale accuracy with this device as well. These devices have relative advantages and disadvantages, and we have used all three to study stress evolution during deposition of polycrystalline Cu films.

Figure 20 shows stress evolution observed during evaporative deposition of polycrystalline Cu films, and Figure 21 shows results for a similar deposition processes that was interrupted for 120 minutes when the film was 25nm thick. Others have reported similar behavior for Cu as well as other polycrystalline metallic films. The initial compressive stage is known to occur before significant island coalescence has occurred. The development of a tensile stress is known to correlate with island coalescence, and the peak tensile stress correlates with formation of a continuous film. In some materials and under some deposition conditions, a high tensile stress (of order GPa) develops and is retained in thicker films after deposition is complete. However in Cu, and similar materials, a compressive stress develops during further film growth.

The tensile stress that develops during island coalescence is associated with grain boundary formation and is an example of capillary bonding, which is the subject of a separate research project. The compressive stress that develops both before and after coalescence of Cu and similar materials, and the reversible stress change that occurs during growth interruptions, are less well understood.

It has been postulated that the reversibly-relaxed stress observed during post-coalescence growth interruptions (Figure 21) is associated with trapping and out-diffusion of excess atoms at grain boundaries. Using our improved ability to make very highly sensitive in-situ stress measurements, we have shown, for the first time, that there is also a reversible stress relaxation during growth interruptions in the pre-coalescence regime (Figures 22 and 23). We have also shown that the magnitude of the reversibly relaxed stress in both the pre-coalescence and post-coalescence regimes scales with the atomic flux prior to the interruption, and that the initial rate at which the stress during deposition increases is extremely high, corresponding to stress change rates of order GPa per monolayer. These results have lead us to postulate that the reversible stress change observed during growth interruptions is the result of changes from a high steady state adatom concentration during deposition, to a lower equilibrium concentration attained during interruptions in growth. The reversible stress then gives a measure of excess adatom concentration during growth. This interpretation is consistent with calculations of the effects of individual adatoms on surface stress, as determined through molecular dynamics simulations with embedded atom potentials. Calculations based on ab-intio simulations are under development.

High-sensitivity *in-situ* stress measurements during film formation provide a powerful tool for real time characterization of the dynamics of adatom populations, and during growth interruptions of adatom diffusion and island coarsening. They also provide quantitative tools for analysis of stress evolution during film coalescence and during post-coalescence structures evolution. The use of these tools will lead to better understandings and control of the film formation processes that so strongly affect film properties and performance in micro- and nano-systems.

Characterization of Electromigration-Induced Failure of Cu-Based IC Interconnect Trees, for Circuit-Level Reliability Assessments

Personnel

C. L. Gan, F. Wei C. Y. Chang, S. Alam, Z. Choi, K. L. Pey, W. K. Choi, R. Augur, T. Marie, D. Barr, C. Hau-Riege, S. P. Hau-Riege, J. J. Clement, and O. Olowolafe (D. Troxel and C. V. Thompson)

Sponsorship

SRC and SMA

Delay associated with over a kilometer of metallic interconnections in a single high-performance integrated circuit now limits the overall circuit speed. The delay associated with interconnects is due to parasitic capacitances that can be reduced by reducing the resistivity of the metal (until recently, Al) and by decreasing the dielectric constant of the material between interconnects (currently SiO_2). Because Cu has lower resistance than Al, this has driven the development of new Cu-based IC interconnection technologies. The major limitation on the reliability of interconnects is associated with electromigration-induced failure. Electromigration is a current-induced diffusion, and it results in interconnect failure when it causes the formation of voids or extrusions. Cu is expected to have intrinsically lower rates of electromigration. However, aspects of the technology changes associated with the introduction of Cu lead to new reliability issues. To accurately assess the reliability of circuits made using Cu-based interconnections, it is necessary to understand the effects of electromigration on the reliability of the collections of complexly connected interconnect segments, known as interconnect trees. Toward this goal we are investigating the reliability of both standard two-terminal test structures as well as more complex multi-terminal test structures.

The standard electromigration test structure consists of a straight line of uniform width, that terminates at vias at either end and has no other terminals. We refer to these as 'i' structures (see Figure 24). The simplest interconnect tree is a straight line with vias at either end as well as a terminal in between, so that the line is broken into two segments that can carry different currents. We call these structures "dotted-i" structures. Width changes in a line can also lead to a change in current density, so that an "i" structure with a width transition can also be considered to be a simple tree. Other simple trees are 'T' and '+' structures. Test chips with all of these structures have been fabricated for us by the Institute for Microelectronics (IME) in Singapore and International Sematech Inc. in the U.S. In the last two years we have carried out experiments on 'i' structures in the first layer of metallization (M1) as well as in the second layer (M2). We have also carried out experiments on symmetric and asymmetric dotted-i and T structures, as well as width-transition and "+" structures. Testing was carried out in collaboration with IME, Sandia National Laboratory, Intel, and Advance Micro Devices.

Highlights of results found so far include:

- M2 'i' structures have consistently higher lifetimes than M1 'i' structures. This is thought to be due to differences in the locations of void formation, and corresponding differences in the time required for voids to grow large enough to cause failure.
- Short M1 and M2 'i' structures have increased median lifetimes below a critical current density line-length product (jL). This critical jL product is larger for M2 lines than for M1 lines.
- The median lifetimes of long M1 and M2 'i' structures increases with increasing line length. This is thought to be due to liner rupture at one or both of the terminating vias, resulting in Cu flow from the lead lines and into the lead lines, so that the lead lines act as reservoirs and sinks for Cu.
- The lifetime of a segment of a dotted-i structure is very strongly dependent on the current density in the linked segment (Figure 25), indicating that reliability analyses must be tree-based rather than segment-based (as they commonly are now).
- The lifetime in a segment in a dotted-i can be increased if the linked segment is unstressed or if it is stressed so as to replace electromigrating Cu.

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- The segment that fails first is not always the most highly stressed segment, and can in some cases be an unstressed linked segment.
- Trends are similar in dotted-i and T structures.
- The reliability of the central via in dotted-i, T and + structures with the same segment characteristics, with the central via acting as the cathode for all segments, is very similar.

To better and more quantitatively understand the implications of these studies, we are developing a new tool for simulation of electromigration and electromigration-induced damage in Cu-based interconnects. This tool tracks stress evolution that results from current -induced atomic transport, and allows for void nucleation, growth, and drift. The new tool is based on the same basic model as an earlier tool developed for assessment of the reliability of Al-based interconnects (EmSim), but is faster and more stable solution algorithm. The new code also addresses issues that are especially important in Cu, including the effects of voids that only partially span a line. This work is being carried out in collaboration with Prof. Jacob White.

All of the experimental results cited above were obtained for Cu interconnects with SiO_2 as the embedding dielectric. In the coming year we plan to carry out comparative studies on Cu interconnects embedded in low-k dielectrics. Some of these low-k dielectrics also have lower elastic moduli, and may flow inelastically under test conditions. These properties can profoundly affect the measured lifetimes as well as their interpretation for use in assessing reliability at service conditions. In anticipation of these issues, we have begun to study the mechanical properties of the Cu/low-k materials systems, using, among other tools, nano-indentation. This work is being carried out in collaboration with Professor Olowolafe.

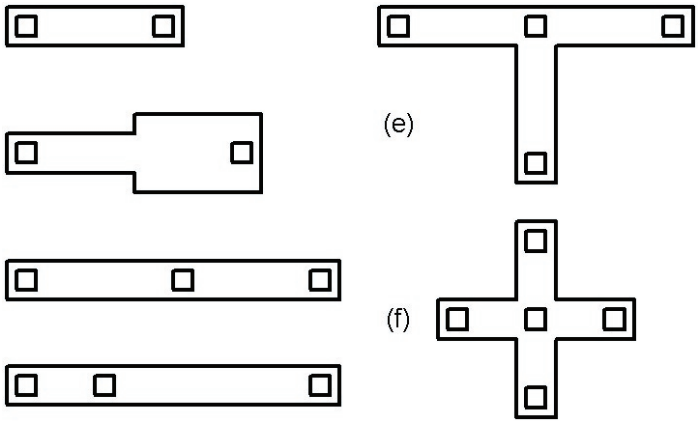

Fig. 24: Test structures used for development of circuit-level reliability assessment methodologies for Cu based interconnects: (a) 'i' structure with 2 terminals, (b) 'i' structure with a width transition, (c) symmetric 'dotted-i' structure with 3 terminals, (d) asymmetric 'dotted-i' structure, (e) 'T' structure with 4 terminals, and (e) '+' structure with 5 terminals.

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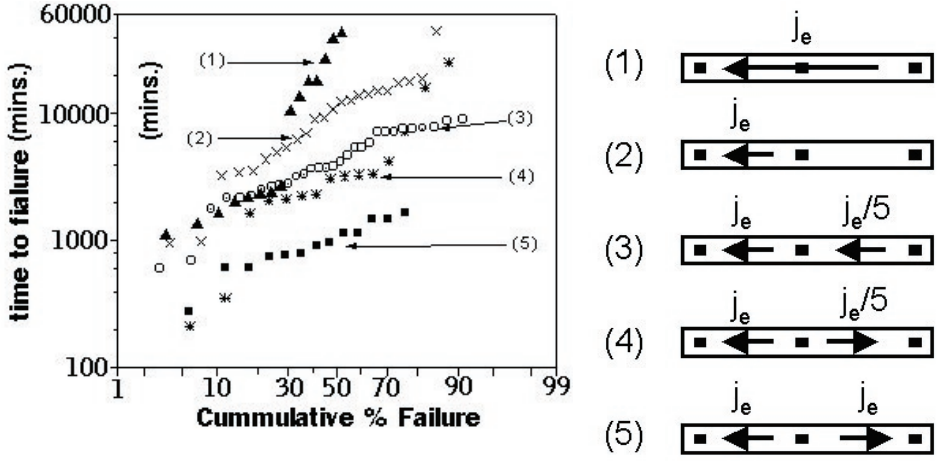

Fig. 25: Failure times (right) for 3-terminal Cu interconnects tested under different current configurations (left).