Opposite page:

Normalized wafer-scale DRIE etch rates. Uniform grid of circles etched with diameter Φ *and separation distance* Δ *(mm/mm): A (0.6/16); B (2/16); C (2/8); D (2/4).*

Courtesy of T. Hill, H. Sun, H. Taylor, D. Boning, and M.A. Schmidt.

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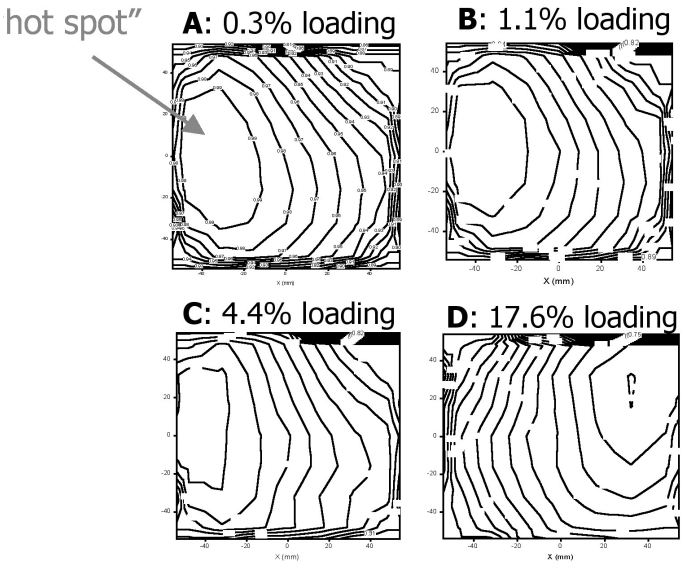
Manufacturing, Modeling and Simulation



Manufacturing, Modeling and Simulation

- *Characterizing Process Variation Using a Ring Oscillator Based Test Chip*
- *Modeling of Deep Reactive Ion Etching (DRIE) for MEMS Manufacturing*
- *Modeling of Pattern Dependencies in the Fabrication of Multilevel Copper Metallization*
- *Modeling of Nanoscale Advanced Devices*
- *Modeling of Shallow Trench Isolation CMP*

Characterizing Process Variation Using a Ring Oscillator Based Test Chip

Personnel

K. Gonzalez-Valentin and J. Panganiban (D. Boning)

Sponsorship

SEMATECH and IBM

Process variation is an increasingly difficult challenge in the design of high-yielding integrated circuits, and techniques are needed to measure and extract variation in a given process and link it to circuit performance. A test chip implemented in the MOSIS 0.25 μm TSMC process has been designed and fabricated, containing test structures aimed at extracting gate-length, interconnect geometry, threshold voltage, and other process variations. The core test structure is a Ring Oscillator (RO) composed of an odd number of cascaded inverters; since the RO frequency is dependent on device parameters and the load between stages, distributions of measured RO frequencies can be used to characterize variation in the devices and interconnect loads.

The 2.5 mm by 4.0 mm test chip is composed of forty-five unique ring oscillator types, which are replicated throughout the chip to incorporate over two-thousand RO test structures. Approximately half of the test structures are used to extract Front-End-Of-Line (FEOL) variation, such as gate-length and threshold voltage, while the other half concentrates on interconnect and Back-End-Of-Line (BEOL) process variation. A scan chain architecture, as shown in Figure 1, is used to enable frequency measurement of each structure. The basic building block is a "tile" which includes a single ring oscillator test structure as well as control circuitry responsible for enabling the RO and outputting the RO signal onto a horizontal bus which feeds into frequency dividers. These tiles are cascaded side by side to compose a row, and these rows are replicated vertically. In addition to increased RO density, this architecture allows for efficient data collection on the board level using Labview-based digital I/O without the need to probe the die for individual RO measurements.

Testing of fabricated chips confirms the functionality of the control architecture. Table 1 summarizes a subset of device variation ROs. Density vs. isolation analysis shows that as the number of fingers increases, the variation increases for all types of structures, likely due to ΔL changes. The polysilicon effect analysis shows that both local and global density of polysilicon affect circuit performance, with decreasing frequency as the poly proximity or density around the ROs increases. The proximity or local effect has a more drastic impact than the global or polysilicon density effect. All vertical structures have a larger standard deviation and lower frequency than their corresponding horizontal structures; designers should take the orientation of digital circuits seriously to achieve good matching. Chip-to-chip variation has proven to be larger than the within-chip variation for almost every structure. Future work includes further investigation of random and systematic device and interconnect variation sources, and relating these to circuit impact.

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Description	Mean Freq. [MHz]	σ Total [KHz]	σ wafer [KHz]	σ within-chip [KHz]	Variation Effect
Three Finger RO	4.42	130	122	45	Canonical Structure
2 Fingers, 1.5x Min L	4.21	76	73	19	Density vs. Isolation Effect
4 Fingers, Min L	2.76	77	71	28	
2 Fingers, 2x Min L	2.64	39	36	15	
1 Finger, 4x Min L	2.7	29	25	13	
1.2x Spacing	4.3	132	123	48	Proximity of Polysilicon Finger Effect
1.5x Spacing	4.2	127	122	34	
2x Spacing	4.13	129	120	46	
3x Spacing	4.12	135	126	49	
Vertical Canonical FEOL	4.36	144	135	51	
Vertical, 3x Spacing	4.05	143	134	49	
Vertical Single Finger	4.22	59	51	30	
0% Polysilicon Density	4.38	126	124	27	Polysilicon Density
12% Polysilicon Density	4.36	127	125	23	
25% Polysilicon Density	4.32	129	125	30	
50% Polysilicon Density	4.29	128	124	33	
Canonical at end of Density	4.38	126	120	40	
Single Finger	4.25	52	47	22	Single Finger
Small Single Finger	4.23	51	48	18	

Table 1: Comparison of differently laid out ring oscillators with the same gate length

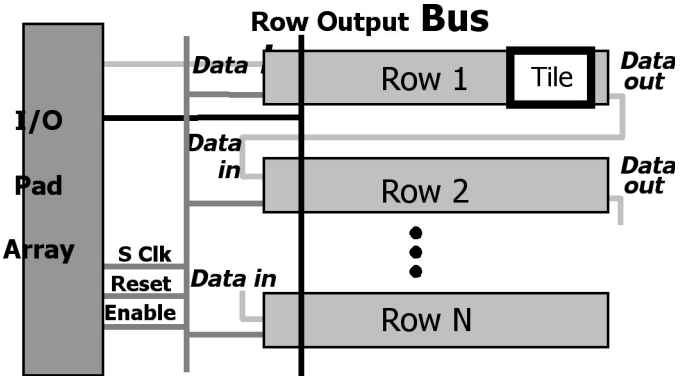

Fig. 1: Variation test chip architecture.

Modeling of Deep Reactive Ion Etching (DRIE) for MEMS Manufacturing

Personnel

T. Hill, H. Sun, and H. Taylor
(D. Boning and M.A. Schmidt)

Sponsorship

CMI, ARO, and DARPA

MEMS devices have become increasingly prevalent in recent years. An important distinction between MEMS and conventional IC fabrication is a need for high aspect ratio structures. Deep Reactive Ion Etching (DRIE) can successfully produce such features. However, wafer and feature level non-uniformities may result when multiple devices are placed on a single wafer. Understanding uniformity issues is critical to high volume MEMS manufacturing. While the immediate benefit of this project would be better yield for the Microengine Project, the knowledge gained here can be applied to many current and future MEMS devices.

We have developed a software model to simulate DRIE uniformity given a mask design. The basic idea of the model is to develop a filter based on the physical flow behavior of etchant in the etch chamber. The filter transfer function can then be convolved with the mask map to obtain an etch map. Currently, the filter is based on the diffusion equation. In this equation, there are two important parameters: the reaction coefficient **k** and the diffusion coefficient **D**, which represent the consumption rate of silicon and transport rate of etchant to the etching area. A set of test masks has been designed to identify parameters **k** and **D** for a specific recipe. We assume the etching occurs in the transport limited regime. The assumption behind this model is that the etch rate variation is caused by etchant density variation along the wafer. The area close to the etch area will be etched more slowly than the area away from the exposed etch area due to a depressed etchant density. The inputs of this model are a mask design layout, **k** and **D** (based on the specific recipe), filter (current diffusion model), and a global etch map. The output is an etch variation map.

Experiments have been conducted to verify/debug the model. There appears to be a connection between the wafer loading (ratio of etched/un-etched area) and the uniformity pattern (See Figure 2). We are specifi-

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cally focusing on the Bosch method of etching, which includes cycles of SF_6 etching, followed by C_4H_8 passivation. Test patterns were etched for 30 minutes in a Surface Technology Systems (STS) etcher with 11 and 13 second etch and passivation cycles, respectively. Masks with a loading ratio below 10% exhibit a "hot spot" with higher than average etching, while those with higher loading have a "cold spot." Other experiments include examination of aspect ratio (feature size) dependence, depth dependent etch rate, photoresist wafer mounting, and the effect of dummy fill on etch rate.

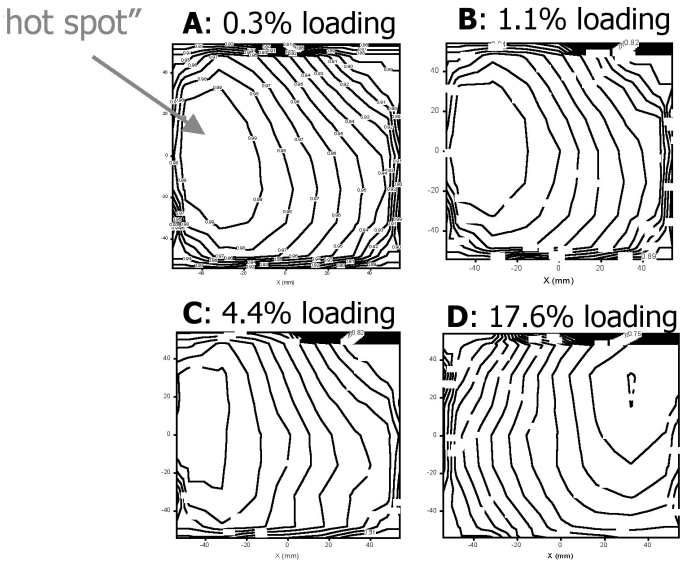

Fig. 2: Normalized wafer-scale DRIE etch rates. Uniform grid of circles etched with diameter Φ and separation distance (mm/mm): A (0.6/16); B (2/16); C (2/8); D (2/4).

Modeling of Pattern Dependencies in the Fabrication of Multilevel Copper Metallization

Personnel

H. Cai and T. Park (D. Boning)

Sponsorship

Hynix Semiconductor, NSF/SRC ERC for Environmentally Benign Semiconductor Manufacturing, Praesagus, Inc.

Multilevel copper metallization is an active and critical area of research and development in industry and academia to meet performance requirements for future advanced interconnect technologies with sub-micron dimensions. It is well known that multilevel topography resulting from pattern dependencies in plating, deposition and CMP is a major problem in interconnects. An integrated pattern-dependent chip-scale modeling of multilevel copper metallization is needed to help optimize the design of multilevel copper metallization to achieve higher yield and performance. The existing integrated chip-scale model of pattern dependencies developed by Park and Gbondo-Tugbawa is the basis to further develop the copper plating and CMP models for multilevel copper metallization for realistic interconnect. New model development and tuning make use of the existing MIT-developed 854 multilevel mask. At the same time, a simple model for pattern dependent inter-level dielectric (oxide) deposition is being developed and incorporated into the model to help address topography creation in multilevel interconnects. CVD or spin-on processes eventually will also need to be characterized for future low-K dielectric deposition, and the multilevel copper metallization modeling will be applied to more aggressive and advanced multilevel copper/low-K metallization processes.

Cooperation with Hynix is in progress and provides access to fine feature multilevel interconnect processes and data. The electroplating process is characterized by using an MIT-designed test mask. The pattern-dependent electroplating model is first applied to fit experimental data, extract model parameters, and finally, to perform topography profile simulation across an entire chip. Wafers are patterned with the MIT 854 mask (metal 1 layer) and electroplated with two baseline processes of different target thicknesses: 8500 Å and 11500 Å. It has been found that the model root-mean-square errors are generally less than 300 Å. To perform

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chip-scale simulation, a layout extraction tool is used to obtain relevant layout information, such as pattern density and line width distributions, from the MIT 854 test mask. Using the extracted model parameters and the layout information, topography height is simulated for each grid cell of the entire chip, and the result shows good match between the model result and measured data. The simulated result for the entire chip (target thicknesses 8500 Å) is shown in Figures 3 and 4.

CMP process simulation and model verification are in progress for metal 1; the next stage of work will focus on multilevel effects with electroplating and CMP of metal 2 test structures.

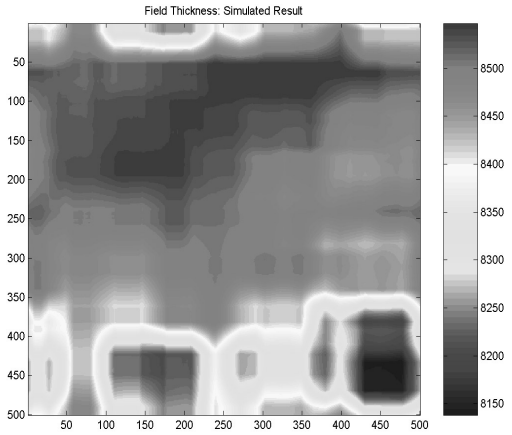

Fig. 3: Field Thickness: Simulation Result

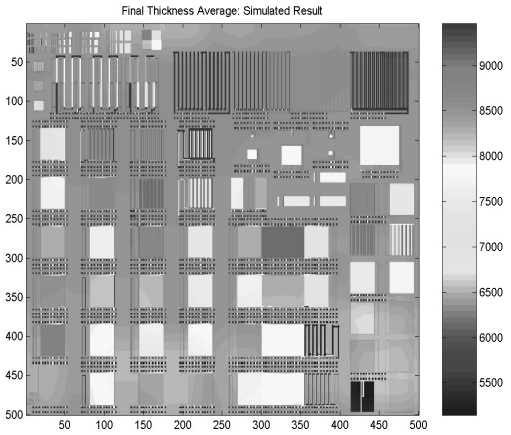

Fig. 4: Final Thickness Average: Simulation Result

Modeling of Nanoscale Advanced Devices

Personnel
O. M. Nayfeh and S. Yu (D. A. Antoniadis)

Sponsorship
SRC

Demand for miniaturization and higher performance have pushed Modern Electronic Devices into the sub-50 nanometer regime. Minimum feature sizes have been continuously reduced, and new mobility-enhanced materials have been engineered by modern epitaxial technology to increase a devices functional complexity and improve performance.

However, at the nanometer scale, electrons come under the influence of High Electric Fields, and the Quantum Mechanical wave nature of electrons is exposed. These effects have a direct impact on the design of high performance "well-tempered" devices; devices that exhibit large on-current while still maintaining electrostatic integrity by minimizing the current in the off-state.

Computer simulation is a dominant mechanism in direct quantitative 2-D characterization of sub-50nm devices; exploring new possible "well-tempered" device structures, and in studying transport and electrostatic phenomenon in materials/devices in general. Simulation models must be fast and accurate.

Correct quantum mechanical correction is critical in the inverse modeling methodology. Quantum Correction of Subthreshold IV, Cgsd-V, and the Cgg of the gate-stack, are all crucial elements in extracting the elaborate 2-D doping profile and oxide thickness of a modern device. Accurate inverse modeling enables robust calibration of carrier transport models that can then predict device behavior. For treating the quantum mechanical nature of electrons, a full-Schrodinger solution is accurate, yet extremely time-consuming. Other methods, including the Density Gradient and the VanDort approximation, have have been shown to be extremely robust in capturing these effects, yet more time-friendly than a full-Schrodinger treatment. In this research, we explore the effect of different quantization models on 2-D device characterization.

With correct device characterization, we then use computer simulation ranging from Full Band Monte Carlo techniques to widely used device TCAD tools to explore high-field transport and electrostatics in materials/devices at the Nanoscale. We are evaluating the benefit from mobility enhanced materials such as Strained-Silicon, and Germanium, in terms of drive current in real device substrates in the sub-50 nanometer regime.

Modeling of Shallow Trench Isolation CMP

Personnel
X. Xie (D. Boning)

Sponsorship
National Semiconductor Corporation

As advancing technologies increase the demand for planarity in integrated circuits, nanotopography has emerged as a new challenge in Shallow Trench Isolation (STI) on wafers polished by means of Chemical-Mechanical Planarization (CMP). Nanotopography – starting silicon surface height variations 100 nm in amplitude extending across millimeter-scale lateral distances – can result in CMP-induced localized thinning of surface films such as the oxides or nitride used in STI.

Two alternative approaches for simultaneous simulation of both pattern and nanotopography effects are implemented to better understand the impact of nanotopography on STI CMP. In the first approach, we perform a "pure" contact wear simulation on a finely discretized grid. Because of high computational demands, this approach is only feasible for one-dimensional cut lines. In the second approach, an integrated model incorporating contact wear and density/step-height effects in STI CMP is used. A contact-wear component on a coarsely discretized grid accounts for pressure differentials across the chip due to long-range nanotopography and other surface height variations. Patterned feature effects are then captured by a pattern density and step-height dependent component. This makes feasible 2D simulations of patterned structures over underlying uneven surfaces to study the effect of realistic nanotopography maps on the CMP of STI patterns. The simulation shows that nanotopography results in longer oxide clearing time, in agreement with previous work. Depending on the specific random configuration of any given nanotopography map, either more or less nitride erosion may result despite the increased polishing time (as illustrated in Figure 5). Thus, nanotopography effects should be considered an additional component of STI nitride loss budgets, in addition to that required by layout pattern dependencies.

Applying the contact mechanics-based model formulations, we re-examine the physical basis of several chip-scale CMP models proposed by our group. Planarization length, as the key concept of all pattern density related models, is the characteristic length of an elliptic weighting function based on the long-range pad deformation and pressure distribution during CMP. This semi-physical model is often adequate and usually gives a fitting error of a few hundred angstroms. A more physical understanding of the model will enable us to develop a chip-scale CMP model with better accuracy. We also investigate different weighting shapes, including square, cylinder, Gaussian, and elliptical filters by comparing the results with experimental data.

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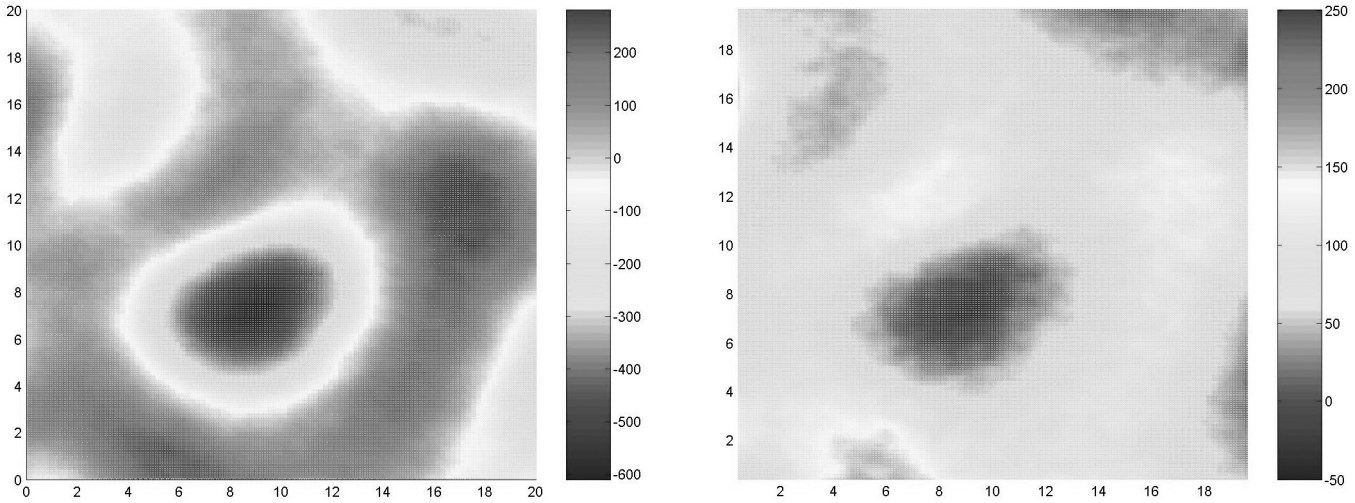

Fig. 5: (a) Nanotopography map measured on a chip size region on bare wafer; (b) Additional nitride erosion caused by the nanotopography shown in (a); height variation is shown in color bar and is in angstroms