Opposite page:

These SEM images show a prototype microphotomultiplier. Three levels of conformable-contact photolithography, which includes two aligned levels, were carried out in fabricating this device. A large-area view is shown in (a), and a close-up view of the lower left corner of the device is shown in (b).

Courtesy of J. Daley, J.G. Goodberlet, H. Kavak, and V.H.S. Moorthy (H.I. Smith)

Sponsor:
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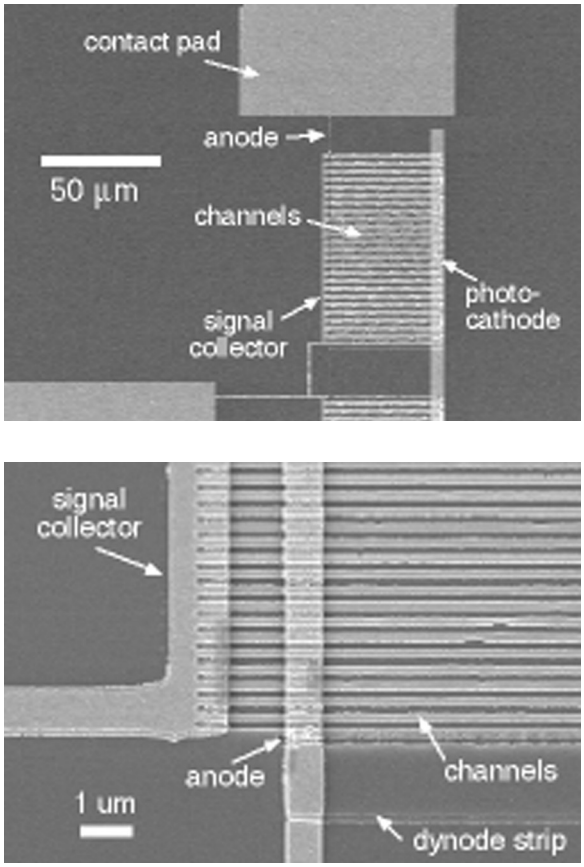
Fabrication Technology



Fabrication Technology

- *A Silicon Through-Substrate Interconnect Technology and Applications*
- *Alternative Chemistries for Wafer Patterning*
- *Solventless Lithography*
- *Fabricating Advanced Microsystems with Conformable-Contact Photolithography*
- *Hot Filament Chemical Vapor Deposition of Polyoxymethylene as a Sacrificial Layer for Fabricating Air Gaps*

A Silicon Through-Substrate Interconnect Technology and Applications

Personnel

J. H. Wu (J. A. del Alamo, in collaboration with K. A. Jenkins, IBM, and R. Livengood and P. Winer, Intel)

Sponsorship

MARCO Focused Research Center on Interconnect (MARCO/DARPA) and Intel

Si CMOS and HBT device technologies have shown their potential for use in systems operating in the millimeter-wave (mmw) range. A Si-based mmw mixed-signal IC technology would make available a large portion of bandwidth for affordable and pervasive applications. Perhaps the greatest challenges in front of this technology are low-loss interconnects (especially power and ground), substrate isolation in the millimeter-wave regime, thermal management, and cost-effective, low-loss packaging. Several of these problems arise from the Si substrate under the active devices. MEMS-like engineering of the substrate can effectively deal with these challenges. Exploring these opportunities for operation in the mmw regime is the goal of this project.

We have developed a high-aspect ratio, substrate-via technology that allows for ground distribution with very low impedance. We have also shown that this technology has the potential for compact, yet effective substrate crosstalk isolation. Both applications have been demonstrated up to 50 GHz. This simple, through-wafer interconnect technology has potential for addressing other substrate issues in the mmw regime (See Figure 1).

In addition to ground connections, through-wafer vias could be used to distribute power as well as ground through the substrate on the same chip. In ICs, decoupling capacitors used to minimize power and ground bounce are discrete components external to the chip package. As clock frequencies increase, more capacitance is required ever closer to the chip. Decoupling capacitors could be integrated on-chip using the very substrate vias that are used to distribute power and ground.

Our substrate-via concept is currently based on solid vias filled with Cu. These vias represent ideal heat shunts from the wafer surface to its back. Vias strategically located around the chip can minimize hot spots on a chip and ease thermal management. Finally, in the millimeter waver regime, system-in-package concepts will have to be utilized to integrate entire systems from chips fabricated using specialized Si processes. A small-footprint substrate-via technology will allow the compact stacking of multiple chips using flip-and-bond concepts.

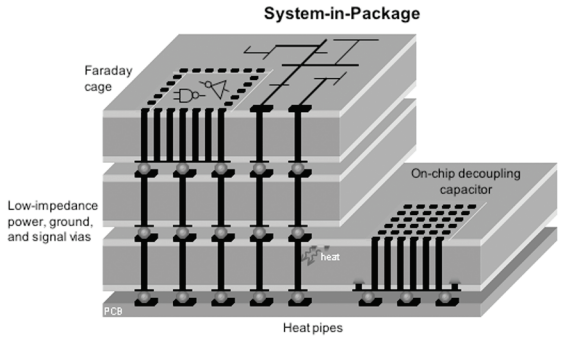


Fig. 1: Conceptual picture of a system-in-package utilizing through-substrate vias as low-impedance power, ground, and signal interconnects, heat pipes, on-chip decoupling capacitors, and a Faraday cage for substrate crosstalk isolation.

Alternative Chemistries for Wafer Patterning

Personnel
R. Chatterjee and A. Somani (R. Reif)

Sponsorship
NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

The goal of this project is to identify possible alternatives for perfluorocompound chemistries for wafer patterning of dielectric films that do not pose long term environmental problems. The etch viability of a variety of alternatives has been determined, and the most promising candidates from the etch viability study will be further tested to define an alternative wafer patterning process. The effluents are identified with Fourier Transform Infrared Spectroscopy (FTIR) to assess their potential ESH impact. Beta testing of alternative processes are performed at the facilities of industrial collaborators.

Gases such as fully fluorinated alkanes - CF_4, C_2F_6, C_3F_8 - as well as inorganic compounds like NF_3 and SF_6, collectively termed as PerFluoroCompounds (PFCs), are used heavily by the semiconductor industry for the etching of dielectric films in wafer patterning applications. Their use and emission is problematic, however, from an environmental standpoint because of the global warming nature of these substances coupled with their long atmospheric lifetimes.

This report highlights recent work accomplished in the development of etch processes with alternative chemistries, specifically C_4F_6, for etching Dow-Corning XLK spin on low-k films. The experimental work has taken place on an Inductively coupled Plasma Etcher (IPS) at Motorola; diagnostic tools include optical emission spectroscopy for plasma analysis and FTIR spectroscopy for effluent analysis.

The dielectric stack of the ultra low-k XLK films is shown in Figure 2. This is one of the most complex film stacks. There is a thin Bottom Anti-Reflective Coating (BARC) underneath the 4000 A photoresist. Under the BARC is a thin oxide layer and a thin hard SiCN capping layer, followed by the ultra low-k film, and finally, a SiCN stop layer.

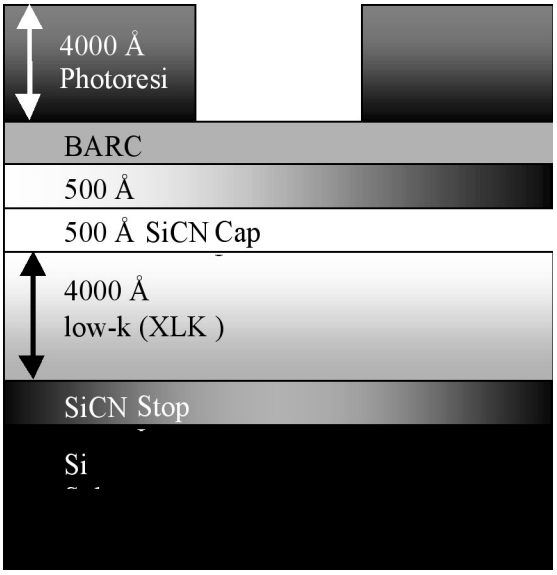


Fig. 2: XLK and LKD wafer film stack with via test structure critical dimensions as low as 0.25 μm (not drawn to scale).

The *c*-C_4F_8 reference process on the IPS (IPS-LK3-XLK), as shown in Figure 3, exhibits high selectivity to SiCN underlying film, as well as good etch selectivity to the photoresist. There was no evidence of CD blowout on this process. The total global warming emissions from this process run on the LKD film were 0.120 kgCE.

The cross-sections of the 0.25 μm CD vias of the hexafluro-1,3-butadiene process are shown in Figure 4. They look very similar to the *c*-C_4F_8 process of comparison,with a similar via profile; selectivity to the underlying SiCN stop layer, and selectivity to photoresist. The hexafluoro-1,3-butadiene process (IPS-LK4-XLK) has a slightly reduced CD blowout. The total emissions from this process were 0.026 kgCE, which represents a 78.7% reduction compared to the *c*-C_4F_8 process of comparison. Etch rates of both the process look alike.

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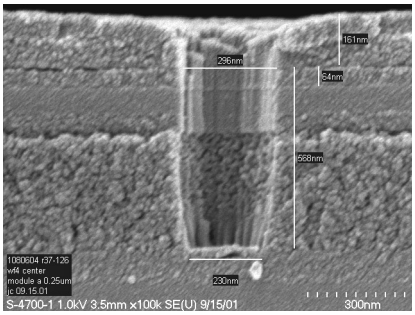
The quantity of each effluent emitted for two different IPS process is shown in Figure 4. It is evident that these films have similar emissions in similar conditions. It also shows that *c*-C_4F_8 is one of the major contributors to emissions because of its poor destruction efficiency. Thus, shifting to low global warming gas such as C_4F_6 is beneficial.



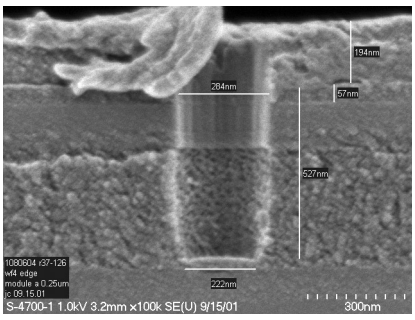
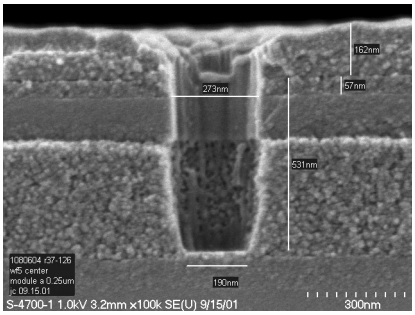


Fig. 3: 0.25 μm via cross sections for IPS c-C_4F_8 process of comparison for LKD film. BARC BT: 800 W Outer, 400 W Inner, 300 W Bias, 4 mT, 5 sccm c-C_4F_8, 10 sccm O_2, 100 sccm Ar, 15s; SiCN BT: 1000W Outer, 200 W Inner, 300 W Bias, 15 sccm c-C_4F_8, 5 sccm O_2, 100 sccm Ar, 25s; Main Etch: 1540 W Outer, 260 W Inner, 1800 W Bias, 7 mT, 8 sccm c-C_4F_8, 100 sccm Ar, 60s. (IPS-LK3-XLK)



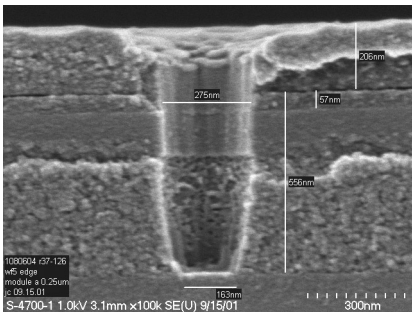


Fig. 4: 0.25 μm via cross sections for the best IPS hexafluoro-1,3-butadiene process for LKD film. BARC BT: 800 W Outer, 400 W Inner, 300 W Bias, 4 mT, 5 sccm C_4F_6, 10 sccm O_2, 100 sccm Ar, 15s; SiCN BT: 1000W Outer, 200 W Inner, 300 W Bias, 10 sccm C_4F_6, 5 sccm O_2, 100 sccm Ar, 25s; Main Etch: 1540 W Outer, 260 W Inner, 1800 W Bias, 7 mT, 12 sccm C_4F_6, 100 sccm Ar, 60s. (IPS-LK4-XLK)

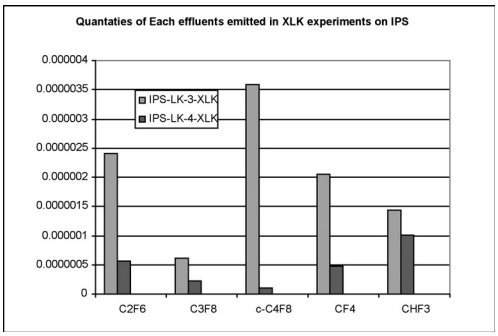


Fig. 5: Quantity of each effluent emitted for XLK and LKD processes on IPS.

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Solventless Lithography

Personnel

Y. J. Mao (K. K. Gleason in collaboration with P. Nguyen and Prof. C. K. Ober of Cornell University)

Sponsorship

NSF/SRC Engineering Research Center for Environmental Benign Semiconductor Manufacture

Current semiconductor manufacturing uses a solvent intensive photoresist processing to lithographically define features at every mask level. In each of the dozens of mask levels per wafer, significant volumes of liquid waste are generated during the deposition, development, and stripping of the photoresists. Thus, photoresist processing presents a clear need and opportunity to reduce environmental, safety, and heath impact of the microelectronics industry. The strategic solution is to design a patterning process that completely eliminates wet chemical steps. Moving towards sustainable, solventless lithography is advantageous since this "dry" processing requires less materials usage, fewer processing steps, lower energy consumption and waste disposal; translating to lower overall cost.

Solventless lithography was demonstrated by integration of two novel technologies: The resist layer was applied using Hot Filament Chemical Vapor Deposition (HFCVD) and subsequently, developed in supercritical carbon dioxide ($scCO_2$). Vapor deposition of "dry" resists of sensitivity comparable to conventional spin-on materials requires promotion of those reactions that form linear polymeric chains over reaction pathways which would normally lead to either crosslinked networks or to the destruction of sensitive functional groups. Such selective control is extremely difficult to achieve using conventional plasma enhanced CVD. In contrast, hot filament excitation can be much "gentler" and thus, possesses a greater potential for achieving selective control over vapor deposition process. The low excitation energies of HFCVD allow for the design of film stoichiometry through control over precursor fragmentation and polymerization pathways. HFCVD from the precursor, glycidyl methacrylate (GMA), requires only modest filament temperatures of 200-250 °C. Even though < 0.05 W/cm^2 power is utilized, the HFCVD rates from the precursor mixture of GMA with an initiator can exceed 200 nm/min.

Calculation shows that the material utilization efficiency exceeds 10% in this HFCVD process. The films also demonstrate excellent uniformity and smoothness with thickness variation less than 2% and rms roughness less than 2 nm which is very promising for potentially deceasing Line Edge Roughness (LER).

Dry resists created by HFCVD from GMA demonstrated high sensitivity (<5 μC/cm^2). The plasma enhanced CVD film deposited from GMA could not be similarly patterned. Thus, the structural characteristics of the HFCVD film, including the absence of crosslinks and retention of functional groups, appear to be crucial for creating CVD resists.

To achieve dry development, the HFCVD process was engineered to enhance the polymer's solubility in sc CO_2. Specifically, a fluorine containing monomer, fluoroalkyl acrylate (FAA) was introduced along with GMA as a precursor feed. The result was a high sensitivity dry resist composed of the copolymer of GMA with FAA which could be developed by sc CO_2 after e-beam exposure. A scanning electron micrograph of line and spaces for this solventless lithography process is shown in Figure 6.

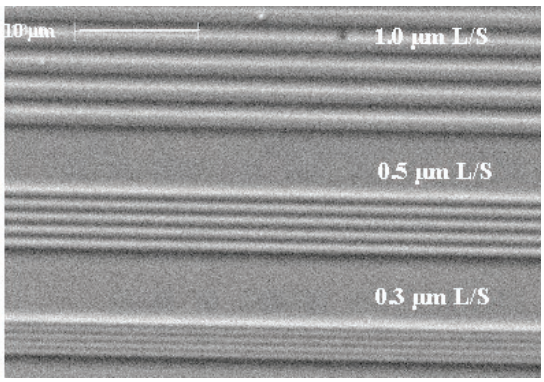

Fig. 6: Solventless lithography using a dry resist developed by supercritical CO_2 after e-beam exposure, demonstrating 0.5 μm and 0.3 μm line/spaces pattern in the vapor deposited copolymer of GMA and FAA.

Fabricating Advanced Microsystems with Conformable-Contact Photolithography

Personnel
J. Daley, J. G. Goodberlet, H. Kavak, and V. H. S. Moorthy (H. I. Smith)

Sponsorship
DARPA

The goal of this research program is to apply Conformable-Contact Photolithography (CCP) to the fabrication of novel or technologically advanced sub-micron devices. In a previous program under the same sponsor, it was shown that CCP enables low-cost, sub-100-nm patterning with sub-100-nm overlay capability. A particular thrust of this program is to use CCP in the development of a novel integrated photomultiplier termed the "microphotomultiplier." This device would enable on-chip, ultrasensitive, and ultrafast photodetection for potential applications in optical, biochemical sensing, communications or low-light-level imaging technologies. Also during this program, the CCP technology has been transferred to a company that is developing grating-based, integrated-optical devices for signal multiplexing/demultiplexing, and to a foreign university with an active program in near-field photolithography. Additionally, a local company has begun manufacturing equipment to make CCP available to universities or small businesses with interests in deep sub-micron patterning, but constrained by limited budgets.

The microphotomultiplier, illustrated in Figure 7 and described in last year's report, poses several fabrication challenges. Long, deep, narrow channels, which provide electron amplification, must be patterned and etched into the substrate. Channels with high aspect ratio, defined as length divided by width, provide greater electron multiplication or device gain and are preferred. To reduce the overall size of the device, and reduce the difficulty in sealing the channels for vacuum operation, narrower channels are preferred. After etching the channels, the walls must be coated with a resistive film that enhances secondary electron emission and prevents their charging. Further, a photocathode must be fabricated at one end, and two closely-spaced electrodes, the anode and signal collector (not shown in the figure), must be defined at the opposite end to enable photodetection, device bias, and signal detection.

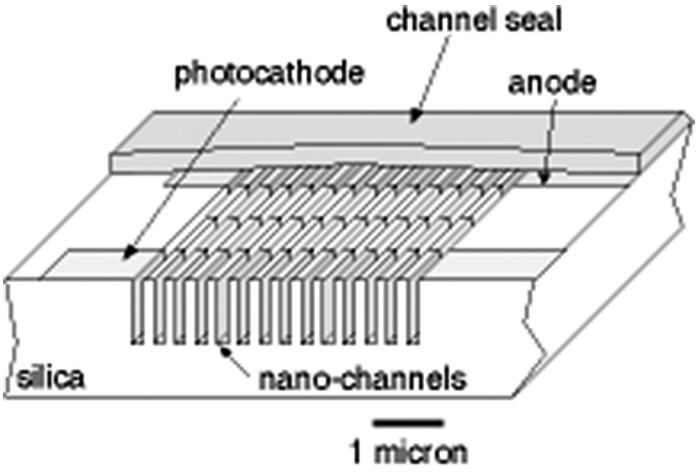

Fig. 7: This cut-away illustration of the integrated microphotomultiplier shows the electron-amplifying channels and device electrodes. This device offers the promise of ultrasensitive and ultrafast photodetection in a micro-scale package.

For the first fabrication attempts, the microphotomultiplier's channel width was chosen to be about 125 nm, and several device lengths, ranging from about 3 μm to 50 μm were trialed. There were typically 200 or more channels in a single device. The channels were defined in the first level of lithography and subsequently, etched into an oxide substrate. In the second level of lithography, a resistive strip was aligned to the channels with better than 200 nm overlay accuracy. (In a separate alignment evaluation experiment, it was shown that sub-50-nm overlay accuracy could be achieved.) Amorphous silicon was deposited to define the resistive strip. In a third level of lithography and subsequent processing, the photocathode, anode, and signal collector were defined in gold. The use of gold enabled photoemission, at short-wavelength radiation, and would not rapidly degrade upon exposure to air. The anode was spaced about 800 nm from the signal collector. A prototype device, fabricated through these three levels of lithography is shown in Figure 8. All levels of patterning and alignment were done using CCP techniques.

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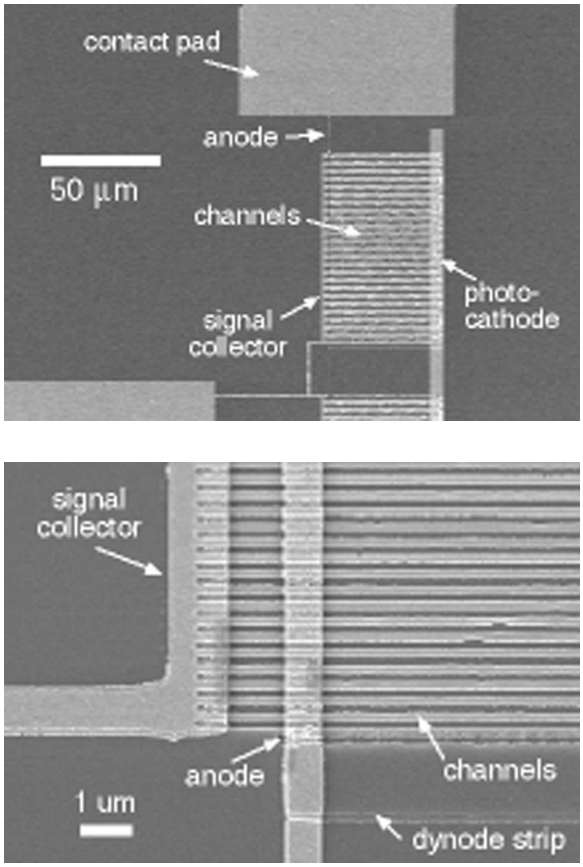

Fig. 8: These SEM images show a prototype microphotomultiplier. Three levels of conformable-contact photolithography, which includes two aligned levels, were carried out in fabricating this device. A large-area view is shown in (a), and a close-up view of the lower left corner of the device is shown in (b).

Preliminary device testing was carried out in a small, custom-built vacuum chamber that housed contact probes and positioning stages. Devices were illuminated with a deep ultraviolet radiation source located outside the chamber. Four initial measurements were carried out to test for (1) resistivity of the amorphous silicon, (2) photoconduction between the photocathode and anode, (3) electrical breakdown when high voltage is applied between the cathode and anode, and (4) continuity of electrode leads across the narrow channels. The first three tests were carried out on test devices located on flat surfaces, i.e. without the presence of the channels, and the last test was carried out with the channels present.

The results from the resistivity measurement yielded 31 MΩ-cm for the strip. The measured resistivity was four orders of magnitude higher than expected and reported in other work. [J. Sangrador, et al, Thin Solid Films 125 (1985) 79.] This is believed to be due to poor e-beam deposition conditions. In our deposition chamber, the base pressure was 10-5 Torr, and we expected the dynode strip to be rich in oxide. Photoconduction was readily measured between the photocathode and anode, and is graphed in Figure 9. For this measurement, the device was illuminated with a small pencil lamp, $\lambda = 253$ nm, while a +9V bias was applied to the signal collector. The graph reports the measured photocurrent from cathode to anode as a function of time. The change in photocurrent, despite constant illumination intensity, is due to surface contamination effects on the photocathode, and has been observed in similar work with gold photocathodes. [S. Gosavi et al, J. Vac. Sci. Technol. B 19 (2001) 2591.] The amount of photocurrent suggested a quantum efficiency in the 10^{-3} range for gold which agrees with previously reported values. [A. H. Sommer, *Photoemissive Materials*, John Wiley & Sons, Inc., New York, NY (1968) 33.] Measurements of breakdown voltage showed an average device failure about 500V bias, based upon testing of eight devices. This result was encouraging because sufficient device gain would be expected at such a high potential along the amplifying channels. The results from the continuity measurements showed no devices with continuous electrical leads across the narrow channels. This problem, which precluded further testing, was traced to a lithographic error at the edge of the channel regions. By augmenting fabrication procedures, this problem can be eliminated and future prototype devices can be fully demonstrated.

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A secondary objective of this research program was to extend conformable-contact photolithography to other microfabrication applications. Accordingly, the technology has been successfully transferred to a California-based company that is developing a novel integrated-optical mux/demux device. This company has patterned 500-nm-pitch gratings and micron-sized waveguides, and successfully implemented multi-level alignment using CCP techniques. Mask making procedures, a critical component to CCP, were transferred to the University of Canterbury in Christchurch, New Zealand where an active research program in near-field photolithography is ongoing. Additionally, a local company has begun manufacturing conformable-contact photolithography equipment which will enable low-cost pattern replication and multi-level alignment at the sub-200-nm level.

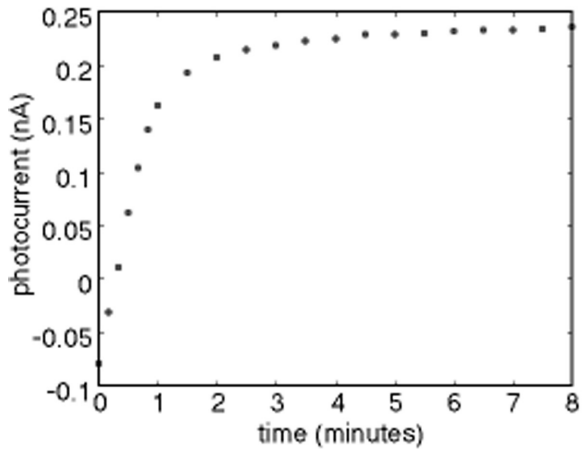

Fig. 9: The typical photocurrent measured in test devices shows an increase with time. This is due to a reduction of surface contamination at the photocathode.

Hot Filament Chemical Vapor Deposition of Polyoxymethylene as a Sacrificial Layer for Fabricating Air Gaps

Personnel

K. Chan (K. K. Gleason)

Sponsorship

MARCO Focused Research Center on Interconnect (MARCO/DARPA)

In the rapid evolution towards electronic devices with smaller feature sizes and faster speed, the factor limiting overall performance is no longer gate delay, but the Resistance-Capacitance (RC) delays due to interconnects. To reduce the capacitance part of the problem, novel low dielectric constant, κ, materials have been introduced to replace traditional silicon dioxide (κ = 4.0). Air is a "material" with the lowest dielectric constant (κ = 1.0). Air gaps can be formed by the removal of a sacrificial layer deposited in an earlier processing step. The properties of the sacrificial layer material must satisfy the following criteria: ease of synthesis and integration, thermal stability for compatibility with existing processing while having rapid decomposition at low to moderate temperatures, removal in the absence of oxygen, and negligible residue left behind after decomposition.

Polyoxymethylene, $-(CH_2O)-_n$ or POM, has great potential to be used as a sacrificial layer. POM was chosen because of its clean decomposition via an unzipping mechanism in the absence of oxygen to form its monomer formaldehyde (CH_2O) gas at less than 300˚C. Hot Filament Chemical Vapor Deposition (HFCVD) utilizes an array of heated wires to cleanly decompose the incoming precursor gas, trioxane, into lower three formaldehyde units which then react on a cooled substrate to form POM. Polymer initiation chemistry has also been used to deposit POM from trioxane with no thermal or plasma excitation of the precursor gases.

A new method for synthesizing polyoxymethylene (POM) film at high deposition rates was achieved via HFCVD and initiation chemistry. Spectroscopy shows that the structure of the deposited polymer is linear rather than cross-linked (which plasma enhanced CVD would have produced). The linear structure is critical for clean complete depolymerization. Air gaps were fabricated with lateral dimensions of 1 to 10 micron using a vapor deposited POM layer. A

continued

cross-sectional view of one such structure is shown in Figure 10. The vertical dimension of the void space, 100 nm, corresponds to the thickness of the sacrificial POM deposited. The bridge layer is 300 nm of plasma enhanced CVD silicon dioxide.

Polymethylmethacrylate (PMMA) is another candidate sacrificial material and is deposited via pulsed plasma enhanced CVD (pulsed-PECVD) and low power continuous PECVD. PECVD is the process currently used for dielectric deposition in device fabrication.

FTIR and NMR of deposited PMMA films show good agreement with bulk PMMA indicating structural similarity with the bulk polymer. PMMA undergoes a depolymerization reaction to pure monomer via thermal degradation between 280 and 320°C making it a good candidate sacrificial material. Large scale air gap structures have been fabricated using PPECVD PMMA and an organosilicate glass (OSG) overlying dielectric material and are shown in Figure 11. By using OSG, the dielectric constant of the overlayer is reduced in comparison to silicon dioxide.

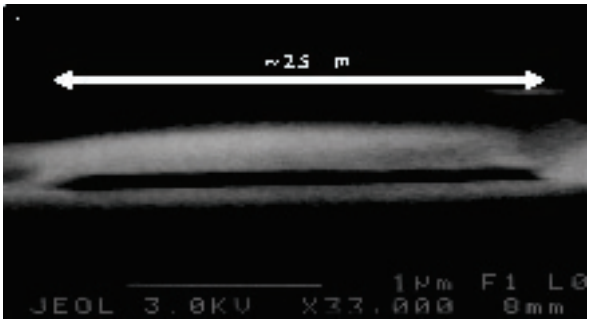

Fig. 10: Scanning electron micrograph of the cross section of air gap having lateral dimension of 2.5 micron fabricated using an HFCVD POM sacrificial layer and CVD oxide.

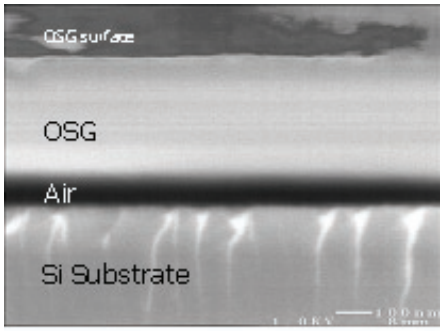

Fig. 11: ~400 nm OSG deposited over ~100nm PMMA annealed at 350°C to create void of the same ~100nm thickness.