Opposite page:

Plan-view and tilted scanning-electron micrographs of four arrays of Co rings with diameters and linewidths of (a) 520 nm and 120 nm, (b) 190 nm and 30 nm, (c) 360 nm and 160 nm, (d) 180 nm and 50 nm.

Courtesy of C.A. Ross, H.I. Smith, F.J. Castaño, Y. Hao, M. Walsh, D. Gil, A. Eilez, E. Lyons, in collaboration with F. Humphrey and M. Redjdal (Boston University)

Sponsor:
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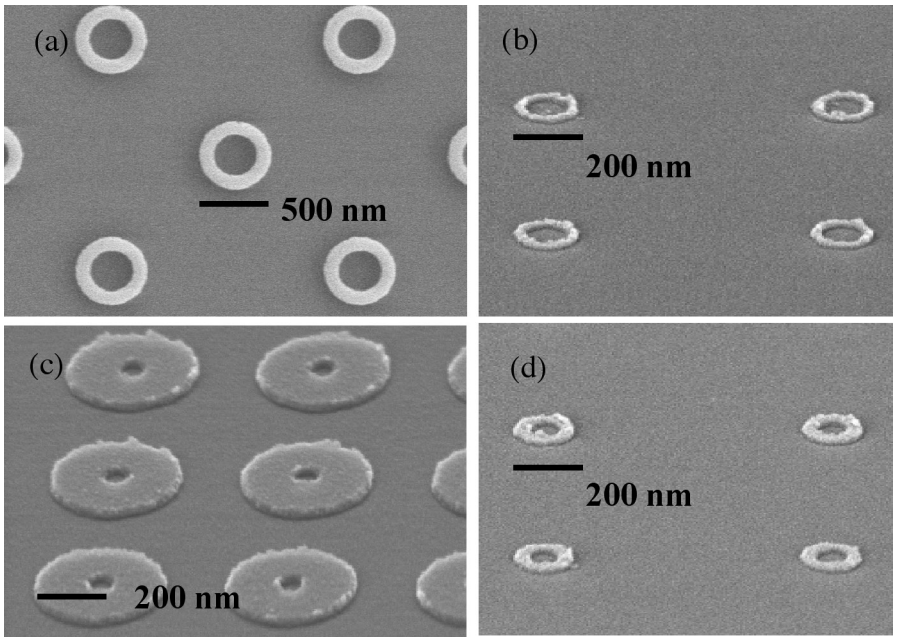
Electronic Devices



Electronic Devices

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- *Ultra-Thin Strained Silicon on Insulator*
- *Germanium MOSFETs for CMOS Applications*
- *Impact Ionization in Strained-Si/SiGe Heterostructures*
- *Impact of Ion Implantation Damage and Thermal Budget on Mobility Enhancement in Strained Si n-MOSFETs*
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- *The MIT Microelectronics WebLab v. 5.0*

Exploring Transport in Ultra-Thin Silicon Films for Double-Gate CMOS

Personnel

I. Lauer (D. Antoniadis)

Sponsorship

SRC

Deeply-scaled Double-Gate (DG) and Ground-Plane (GP) MOSFETs require ultra-thin silicon channels in order to maintain electrostatic integrity. Experimental evidence has shown reduced mobility compared to bulk for silicon films between 15 nm and 7 nm. However, theory indicates that between 5 nm and 3 nm increased occupancy of the 2-fold valleys results in increased mobility compared to bulk. This work seeks to gather experimental evidence for the increased mobility in sub-5 nm films.

A schematic of a process to build ultra-thin channel DG/GP MOSFETS is shown in Figure 1. Starting with SOI wafers (1-1), LOCOS isolation is performed (1-2), followed by silicon thinning (1-3). Then a gate oxide is grown, polysilicon is deposited, and the over-sized bottom gates are patterned (1-4). LTO is then deposited, planarized (1-5), and the wafer is bonded to a handle wafer (1-6). The bulk of the original SOI wafer is then removed by mechanical grinding and chemical etching, using the buried oxide as an etch stop. The buried oxide is then removed with a timed etch, exposing the silicon channel (1-7). The top gate oxide is grown, polysilicon is deposited, and the short top gate is patterned (1-8). Spacers are defined (1-9), followed by raised source/drain growth (1-10). Salicide is then formed (1-11). Interconnects are added to finish the device.

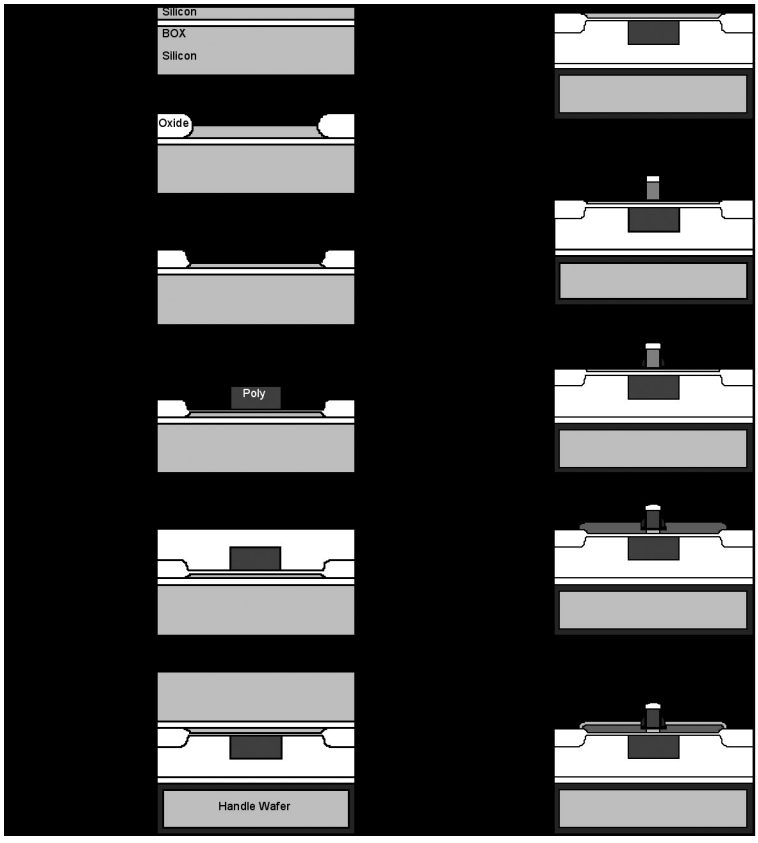

Fig. 1: Ultra-Thin Si DG MOSFET Fabrication

Ultra-Thin Strained Silicon on Insulator

Personnel
T. Drake (J. L. Hoyt)

Sponsorship
SRC and MARCO Focused Research Center on Materials, Structures, and Devices (MARCO/DARPA)

Epitaxial strained Si films grown on relaxed epitaxial SiGe exhibit biaxial tensile stress. MOSFETs fabricated with strained Si channel layers exhibit significantly enhanced mobility and current drive. Incorporating strained silicon in ultra-thin body and double-gate MOSFET structures offers potential advantages. First, these structures enable reduction of channel doping compared to bulk MOSFETs. Second, double gate transistors enable operation of the device at low vertical effective fields where the strain-induced mobility enhancement for holes is maximized. Finally, if strained Si is incorporated directly on insulator, without the presence of SiGe in the final structure, some of the problematic effects of SiGe (e.g. Ge diffusion and enhanced n-type dopant diffusion) can be eliminated. Thus, there is strong motivation to study the fabrication and material properties of ultra-thin strained Si films on insulator. This work focuses on the creation of strained silicon layers directly on insulator and the critical issue of whether the strain remains *after* the SiGe layer that originally induced the strain has been removed.

Fundamental limits to CMOS scaling are rapidly approaching as devices are scaled below the 50 nm range. Therefore, new methods and materials for CMOS fabrication must be investigated to allow continued device improvement. It is well known that SOI devices provide benefits of reduced parasitic capacitance allowing for high-speed operation while minimizing power dissipation. Ultra-thin body SOI devices have the added benefit of improved electrostatic integrity, and thus, can be scaled to the shortest channel lengths. Recent work on surface-channel strained Si MOSFETs fabricated on relaxed $Si_{1-x}Ge_x$ show significant performance improvements. Most notably strain-induced transconductance leads to up to 60% enhancement for NMOSFETS over Si controls. In this work, a novel fabrication method for ultra-thin strained silicon on insulator substrate is demonstrated. Thermal stability of these films is also investigated.

Our research is focused on both the fabrication of strained Silicon Silicon On Insulator (SSOI) as well as the investigation of an ultra-thin body devices. In order to fabricate high quality ultra-thin body strained Si MOSFETs, thin strained silicon on insulator layers must be produced. In this work the fabrication of ultra-thin strained silicon directly on insulator is demonstrated, and the thermal stability of these films is investigated. Ultra-thin (~13 nm) strained silicon on insulator SSOI layers were fabricated by epitaxial growth of strained Si on relaxed SiGe, wafer bonding, and an etch back technique employing two etch-stop layers for improved across across-wafer thickness uniformity. The epitaxial heterostructure used in this work is shown in Figure 2.

A cross sectional transmission electron micrograph of the final strained silicon on insulator structure is shown in Figure 3. Raman analysis of SSOI using 325 nm excitation shows the strained Si peak at 512 cm^{-1}. The shift from the relaxed Si peak at 521 cm^{-1} corresponds to a strain of 1.2%, in excellent agreement with the strain in the as-grown film prior to layer transfer. In addition, no shift in the strained Si peak is observed after Rapid Thermal Annealing (RTA). Using 325 nm Raman spectroscopy, no strain relaxation is observed following rapid thermal annealing of these layers to temperatures as high as 950ºC (Figure 4). The thermal stability of these strained silicon films after removal of the strain inducing SiGe layer which induced the strain is promising for the future fabrication of enhanced performance strained Si ultra-thin body and double-gate MOSFETs.

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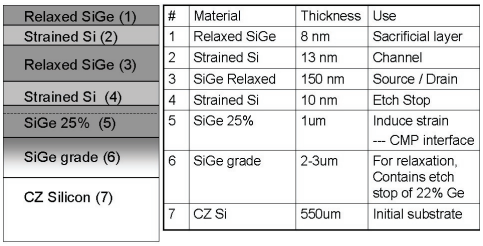

#	Material	Thickness	Use
1	Relaxed SiGe	8 nm	Sacrificial layer
2	Strained Si	13 nm	Channel
3	SiGe Relaxed	150 nm	Source / Drain
4	Strained Si	10 nm	Etch Stop
5	SiGe 25%	1um	Induce strain --- CMP interface
6	SiGe grade	2-3um	For relaxation, Contains etch stop of 22% Ge
7	CZ Si	550um	Initial substrate

Fig. 2: As grown epitaxial heterostructure for creation of ultra thin strained-silicon on insulator via a bond and double etch stop process.

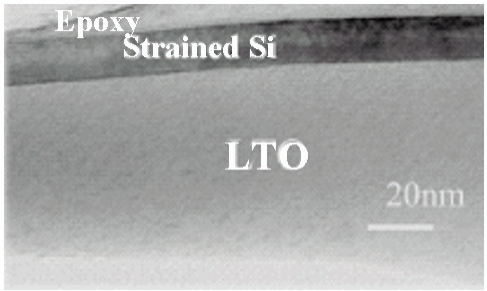

Fig. 3: XTEM of ultra-thin strained-Si on insulator. Strained Si thickness is 13-15 nm

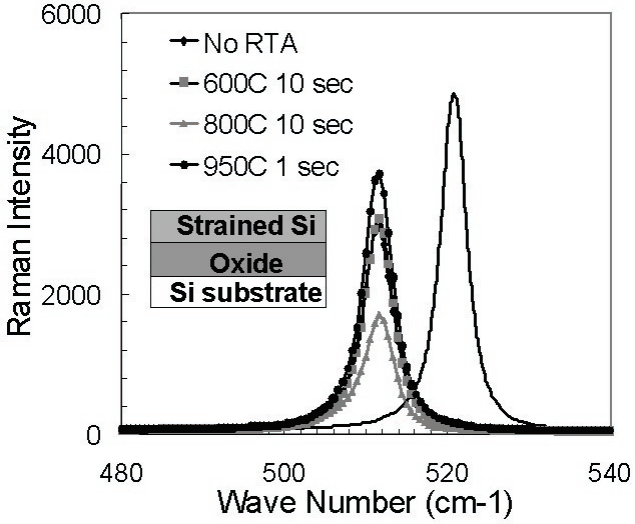

Fig. 4: Raman analysis of SSOI using 325 nm excitation shows shift of 9 wavenumbers between silicon and strained-silicon peak corresponding to a strain of 1.2%, in excellent agreement with the strain in the as-grown film prior to layer transfer. In addition, no shift in the strained-Si peak is observed after RTA. Raman data courtesy N. Klymko, IBM Microelectronics.

Germanium MOSFETs for CMOS Applications

Personnel

A. Ritenour and M.L. Lee (D.A. Antoniadis and E.A. Fitzgerald in collaboration with S. Yu, Intel Corporation)

Sponsorship

MARCO Focused Research Center on Materials, Structures, and Devices (MARCO/DARPA)

New material systems are playing an increasingly important role in MOSFET scaling. Strained-silicon and silicon germanium have received significant attention because they offer improved carrier transport relative to bulk silicon. However, neither material offers enhancement in both electron and hole transport. Germanium, on the other hand, has a bulk electron mobility that is a factor of 2.6 larger than silicon and a hole mobility that is a factor of 4 larger. The advent of high-k dielectrics presents a new opportunity to reconsider high mobility semiconductors like germanium that have been dismissed in the past because they lacked a high quality thermal oxide.

The goals of this project are to demonstrate enhanced carrier transport in germanium and strained germanium MOSFETs, develop process technology suitable for ultra-scaled germanium MOSFETs, and explore fundamental issues associated with germanium devices. Germanium PMOSFETs have been fabricated on both bulk germanium wafers and epitaxial germanium-on-silicon. Figure 5 shows the layer structure of the epitaxial germanium-on-silicon substrates. Hafnium dioxide and tantalum nitride were used for the gate stack. These films were deposited through a collaboration with Professor D.L. Kwong at the University of Texas at Austin. Silicon fabrication processes were modified to make them compatible with germanium. Figure 6 shows the extracted hole mobility from a bulk germanium PMOSFET. The mobility is enhanced by a factor of two compared to silicon. Future work will focus on the fabrication of short-channel germanium CMOS on epitaxial germanium-on-silicon.

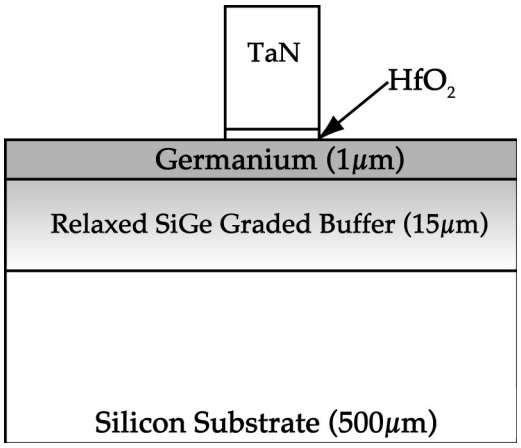

Fig. 5: Layer structure of epitaxial germanium-on-silicon. The 1 μm germanium device layer was grown on a relaxed SiGe graded buffer using UHVCVD.

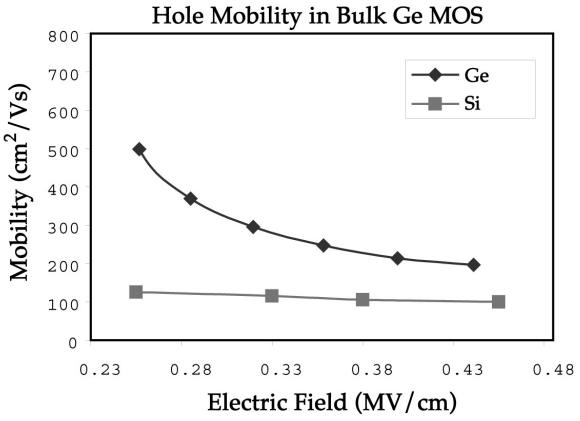

Fig. 6: Comparison of hole mobility in Ge and Si PMOSFETs. The germanium devices show a factor of two enhancement in mobility.

Impact Ionization in Strained-Si/SiGe Heterostructures

Personnel
N. Waldron (J.A. del Alamo)

Sponsorship
DARPA

Strained-Si is actively being pursued as a technology that can continue to drive CMOS further along the scaling road map. The resulting enhancement in the fundamental transport properties of Si due to the introduction of strain yields improved device speed and diminished power dissipation. Currently, the main focus of research for strained-Si/SiGe MOSFET technology is for digital applications. However, the potential exists to use strained-Si for analog mixed-signal applications such as wireless communication products. The development of high-performance Si-based RF power devices that can operate in the 10-20 GHz range at power levels of 100s of mW would rival the performance of GaAs technology, but with a lower associated cost and with the potential for System-on-Chip integration.

Impact ionization is an important consideration for RF power devices. It determines the breakdown voltage and by extension the maximum power that a device can deliver. Impact ionization will be of particular concern to strained-Si technology. The strained-Si/SiGe heterostructure comprises of a relaxed SiGe buffer layer on which the thin strained-Si layer is epitaxially deposited. The bandgap of SiGe and strained-Si is lower than that of bulk Si. Also, the strain induced in the thin Si layer breaks the degeneracy of the conduction band, resulting in reduced scattering compared to bulk Si. Both will have the effect of increasing the impact ionization rate.

Test structures were designed and fabricated in order to investigate impact ionization effects in the strained-Si/SiGe heterostructure (see inset in Figure 7). The heterostructure comprises of a fairly thick relaxed SiGe buffer (4 μm) with a thin strained-Si layer on top. In this p-type structure an n-type resistor-like device is made. As higher voltages are applied to the device, the field and electron velocity increase, and impact ionization takes place towards the drain. The hole current thus induced is collected by the body contact which is on the backside of the wafer.

The figure summarizes the results obtained from the test structures. M is the impact ionization multiplication factor, and M-1 is a useful figure of merit to gauge how much extra current is generated by impact ionization. It is clear that the strained-Si samples have much higher II compared to bulk Si as would be expected. What is more interesting is that strained-Si exhibits a strong positive dependence on temperature, which is opposite to what is seen in bulk Si. Both of these results could be problematic for the implementation of strained-Si technology to RF power devices.

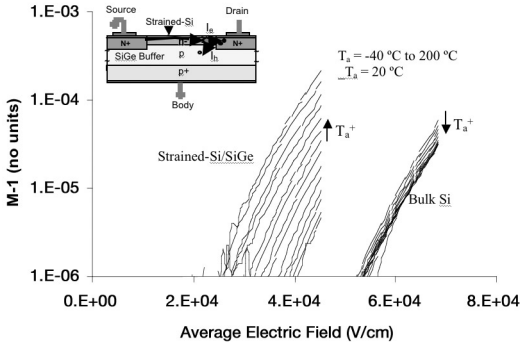

Fig. 7: Impact ionization as a function of average field and temperature for bulk and strained-Si/SiGe samples. $M = (I_s+I_b)/I_b$. II increases with temperature in the strained-Si samples, but decreases with increasing temperature in the bulk samples. Inset shows test structure.

Impact of Ion Implantation Damage and Thermal Budget on Mobility Enhancement in Strained-Si n-MOSFETs

Personnel
G. Xia (J. L. Hoyt)

Sponsorship
SRC and IBM Corp.

Strained-Si technology is a promising method to enhance MOSFET performance. It improves the carrier transport properties by introducing strain to the silicon channel. Enhanced mobility and current drive have been demonstrated in strained Si n-MOSFETs, down to the smallest channel lengths fabricated thus far (~45 nm).

As the scaling of strained-Si MOSFETs continues, the mobility enhancement is more susceptible to degradation during processing. The channel ion implant dose must be increased with scaling. In addition, the lateral damage associated with the source/drain extension regions comprises a larger portion of the channel. Both of these effects increase the possibility of loss of mobility enhancement in scaled strained-Si CMOS. Two processing techniques, ion implantation and thermal processing are of most importance. Ion implantation damage may supply point defects that assist Ge diffusion and the relaxation of strain. Thermal processing can cause strain relaxation by the formation of misfit dislocations and Ge out-diffusion. Residual ion implantation damage, remaining after annealing, may act as carrier scattering centers.

To investigate the impact of these processing factors on strain and mobility enhancement, long-channel strained-Si and bulk n-MOSFETs were fabricated with different Si and Ge implant conditions and thermal budgets. In order to avoid Coulomb scattering effects associated with ionized impurities, neutral Si and Ge were implanted into the channel at six different doses ranging from 4×10^{12} to 1×10^{15} atoms/cm^2. The ion implants were performed prior to gate oxidation. Three Rapid Thermal Annealing (RTA) splits, 1000C-1s, 1000C-10s, and 950C-10s, were used to anneal the implantation damage and activate the source/drains. After processing, effective electron mobility measurements were made using the split-CV method.

For strained-Si n-MOSFETs with implantation, the strained-Si mobility enhancement factor (compared with the universal electron mobility of bulk Si n-MOSFETs without implantation) is degraded depending upon the implant dose and RTA. At a vertical effective field of 0.75MV/cm, the mobility enhancement factor is degraded from 1.6X to 1X for Si implant dose of 5×10^{14} and 1000C-1s RTA (See Figure 8). For each RTA condition, there is a threshold implantation dose, above which the strained-Si mobility starts to degrade significantly (See Figure 9). The threshold dose is smaller for devices with higher thermal budget. For 1000C-1s RTA and Si implant doses up to 3×10^{13} cm^{-2} (damage similar to 10 KeV B, 5×10^{14} cm^{-2}) no impact on strained -Si electron mobility is seen. For 1000C-10s RTA, the Si implant threshold dose is reduced to 3×10^{12} cm^{-2} (damage similar to 10 KeV B, 7×10^{13} cm^{-2}). For bulk Si control devices with implantation, mobility is degraded by 15% at most. The residual ion implantation damage in the channel observed by cross section Transmission Electron Microscopy (TEM) indicates that the scattering by residual damage degrades the mobility. Raman spectroscopy and Secondary Ion Mass Spectroscopy (SIMS) are being performed to investigate the impact of strain relaxation and Ge diffusion on mobility degradation.

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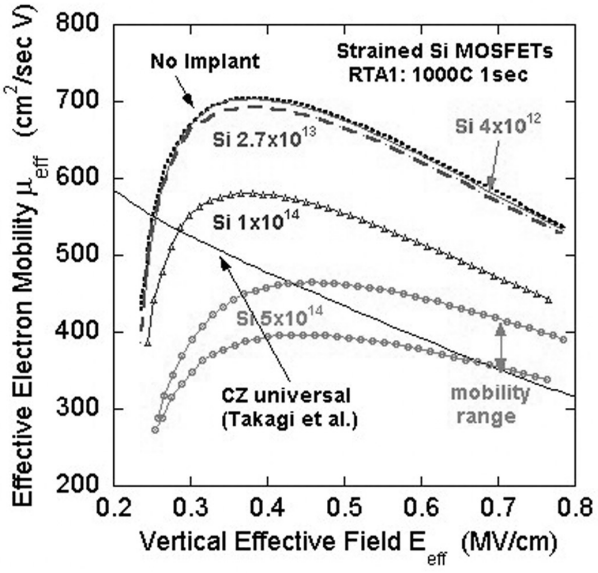

Fig. 8: The effective mobility μ_{eff} vs E_{eff} for the strained Si devices with RTA1 (1000 C for 1 sec) and different implantation conditions.

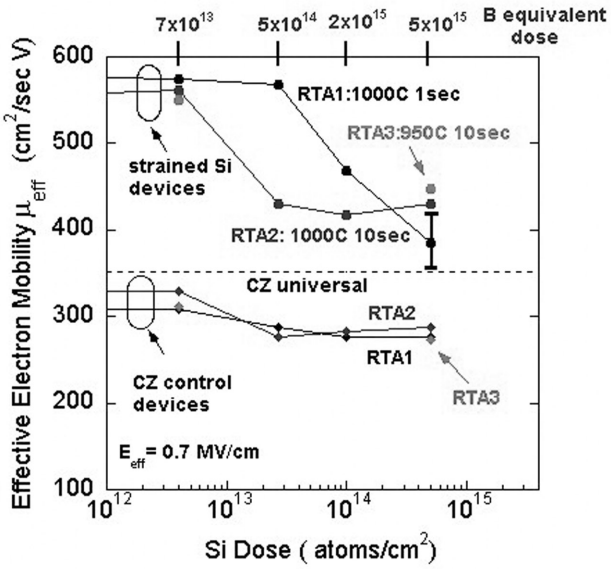

Fig. 9: The effective mobility μ_{eff} at E_{eff} = 0.7MV/cm for strained Si and CZ control devices vs. Si implant dose with different RTAs. The equivalent B doses (in terms of damage profiles) are shown above in blue.

MOSFET Channel Engineering Using Strained Si, SiGe, and Ge

Personnel

M. L. Lee (E.A. Fitzgerald)

Sponsorship

MARCO Focused Research Center on Materials, Structures, and Devices (MARCO/DARPA) and Singapore- MIT Alliance

Strained-Si (ε-Si) grown on relaxed $Si_{1-x}Ge_x$ buffers is drawing ever closer to widespread commercialization due to its ability to improve circuit performance without scaling. Holes in ε-Si show significant mobility gains, but I_d enhancements tend to vary with gate overdrive, and recent reports show that much of the performance gain is lost at the high vertical fields commonly seen in deeply scaled devices. Our work is motivated by the desire to understand hole transport in heterostructures grown on $Si_{1-x}Ge_x$ and to apply this understanding to improving performance in *p*-MOSFETs.

One of the key results from our research is the demonstration of a εSi *p*-MOSFET that exhibits much higher effective mobility in strong inversion than those previously reported. At an inversion carrier density of 1.35×10^{13} / cm^2, we observed a mobility enhancement of 2.9 times over bulk Si. We accomplished this by growing a thin (~30Å) layer of ε-Si upon a $Si_{0.3}Ge_{0.7}$ relaxed buffer. In inversion, the hole wave function is pulled towards the surface, combining the low effective mass of the Ge-rich buffer with the valence band splitting in the ε-Si cap, thus replicating the band structure of a high-mobility compressed $Si_{1-y}Ge_y$ layer. Second, instead of a single layer of ε-Si on the surface, we grew a digital alloy consisting of alternating layers of ε-Si and relaxed $Si_{0.3}Ge_{0.7}$. As the hole wave function is pulled towards the surface, the periodic nature of the digital alloy fixes the effective valence band that the hole "sees." ε-Si *n*-MOSFETs exhibit little variation in mobility enhancement with inversion strength, and the digital alloy channel allows the *p*-MOSFET to perform similarly. Figure 10 shows that mobility enhancements in ε-Si heterostructures can now be engineered to increase, decrease, or remain constant with inversion strength.

Dual-channel heterostructures, in which a Ge-rich buried layer is grown beneath the ε-Si cap, have been shown to give considerably larger hole mobility enhancements than ε-Si alone. We have demonstrated nearly symmetric mobility *p*- and *n*-type MOSFETs where ε-Si and ε-Ge are grown on a $Si_{0.5}Ge_{0.5}$ relaxed buffer (See Figure 11). Taken together, heterostructures incorporating ε-Si, ε-SiGe, and ε-Ge delineate a new scaling roadmap for MOSFET performance.

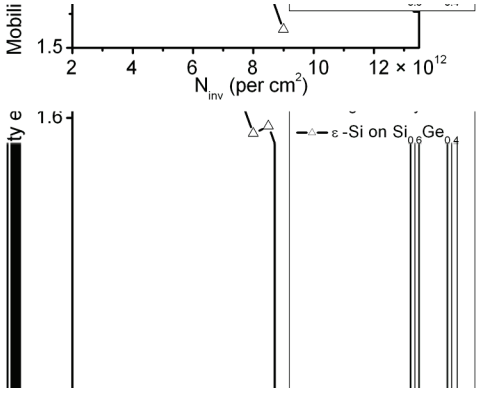

Fig. 10:

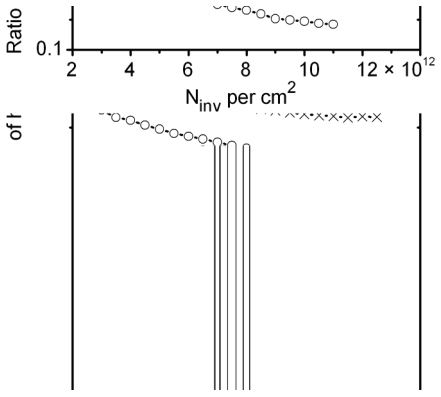

Fig. 11:

Implementation of Both NMOS and PMOS Having High Hole and Electron Mobility in Strained Si /Strained Si_{1-y} Ge_y on Relaxed $Si_{1-x}Ge_x$ (x<y) Virtual Substrate

Personnel

J. Jung and M. Lee (J. L. Hoyt, E. A. Fitzgerald, and D. A. Antoniadis in collaboration with S. Yu, Intel)

Sponsorship

MARCO Focused Research Center on Materials, Structures, and Devices (MARCO/DARPA)

Si/SiGe heterostructure with relaxed SiGe buffer layer, or virtual substrate, has potential advantages for both n-channel and p-channel MOSFET compared to the rival pseudomorphic layer structure on Si which has only PMOS benefit. Recently, high hole mobility in a strained $Si_{1-y}Ge_y$ layer on relaxed $Si_{1-x}Ge_x$ (y> x) virtual substrate was demonstrated in our group. In this work, we proposed implementing both NMOS and PMOS transistors with high electron and hole mobility in strained-Si on top of strained $Si_{0.4}Ge_{0.6}$, both grown on a relaxed $Si_{0.7}Ge_{0.3}$ virtual substrate (See Figure 12). In this structure, the buried $Si_{0.4}Ge_{0.6}$ serves as a high mobility p-channel, and the strained-Si cap serves as a high mobility n-channel. Figure 13 shows the drain current as a function of gate drive of NMOS and PMOS from our first results. It shows about 2.5 and 2.0 times enhancement in drain current of PMOS and NMOS, respectively owing to increased mobility. Ongoing work includes implementation of both NMOS and PMOS with suitable threshold voltage and subthreshold characteristics by applying metal gate or doped poly-Si, and comparison of its characteristics with Si bulk device.

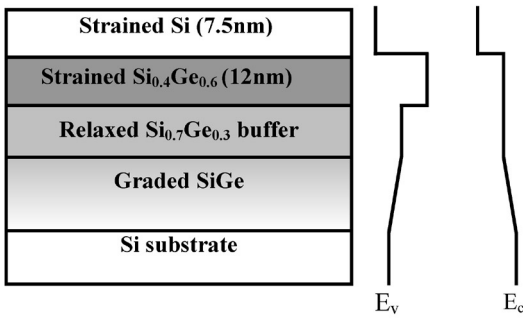

Fig. 12: Schematic CMOS layer structure and band alignment for this proposal. The buried compressively strained-$Si_{0.4}$ $Ge_{0.6}$ channel is channel for holes while the surface strained-Si is channel for electrons.

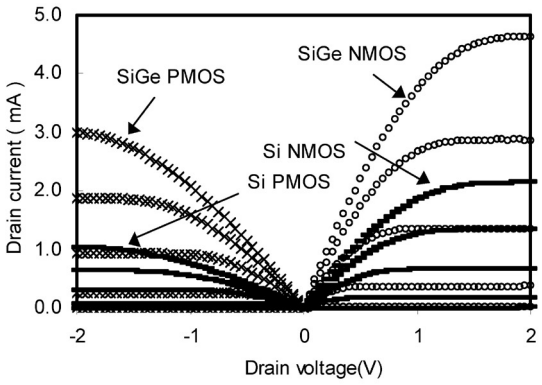

Fig.13: Drain current versus drain voltage as a function of gate drive of SiGe NMOS and PMOS transistors along with Si control device (Gate length =20μm, gate width= 213μm, and 3.8 nm-thick gate oxide). Gate overdrive starts from V_g-V_t = 0V, to |Vg-V_t| = 2V, with 0.5V step. SiGe PMOS and NMOS shows about 2.5 and 2.0 times current enhancement respectively owing to increased mobility.

RF Power CMOS

Personnel
J. Scholvin (J. A. del Alamo in collaboration with S. Parker and D. Greenberg, IBM)

Sponsorship
IBM

This project focuses on fundamental research on the RF power suitability of logic CMOS. The big questions that we wish to be able to answer are: What does it take to bring the power amplifier on chip in wireless system-on-chip applications? When does it make sense to do this?

We will answer these questions by mapping out the potential of deeply scaled standard CMOS or RF-enhanced CMOS to fulfill the RF Power Amplifier (PA) function for wireless applications. The technologies of interest are 0.25 μm and beyond (with emphasis beyond 0.18 μm), and the frequency of interest is between 2 and 10 GHz (primarily 5 GHz). This will involve both measurements of different CMOS technologies and simulations to develop good models as well as an understanding of how CMOS devices behave under large signal operation.

Over the course of the last few months, we have set up a Maury Load-pull system at MIT that allows us to measure the RF power behavior of devices up to 18 GHz (See Figure 14). The system will also be able to measure linearity (through ACPR and IM_3). Preliminary measurement results were obtained on 0.25 μm CMOS technology for 2.4, 4.8, and 7.2 GHz, as shown in Figure 15. As one would expect, the gain decreases as we move to higher frequencies. Also, the gain begins to roll off at lower power levels for higher frequencies. Because of this, the maximum possible PAE (which lies outside the measured range here) will be lower for higher frequencies.

These measurements highlight the potential of 0.25μm CMOS to perform well even at high frequencies. We are currently building models that explain in detail the behavior of the measurements and also take linearity (through IM3) into account. We are also in the process of designing 90 nm technology devices in collaboration with IBM, which should highlight the trade-offs and challenges of RF CMOS in a more dramatic way.

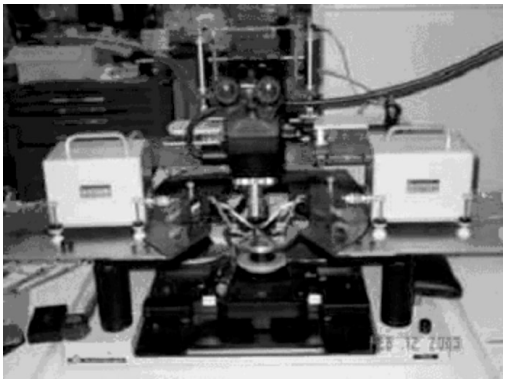

Fig. 14: Probe station and tuners of a new load-pull system assembled at MTL to carry out on-wafer RF power characterization.

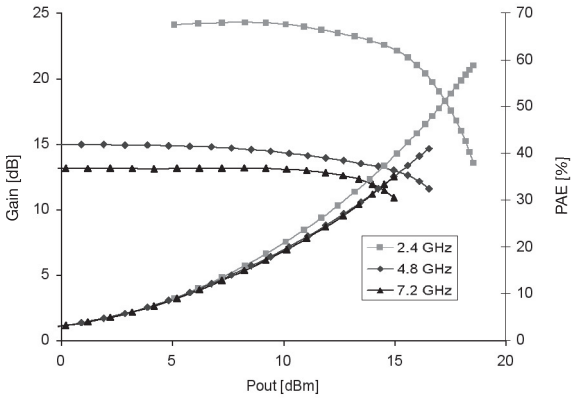

Fig. 15: Gain and Power-Added Efficiency (PAE) as a function of output power for a 300 µm wide NMOS in a 0.25 µm technology at three different frequencies.

A Metal/Polysilicon Damascene Gate Technology for RF Power LDMOSFETs

Personnel
J. G. Fiorenza (J. A. del Alamo)

Sponsorship
SRC and DARPA

RF Lateral Double-diffused Metal Oxide Semiconductor Field-Effect Transistors (LDMOSFETs) are used today at frequencies between 900 MHz and 2 GHz for a wide variety of RF power amplifier applications, including cellular handsets and base stations. In these devices, a low gate sheet resistance is essential to achieve high RF power gain while using wide gate fingers, as needed, to produce the large output power levels demanded by these applications. In order to further enhance LDMOSFET performance at these frequencies and to push the frequency limits of LDMOSFETs to the 5-6 GHz range where new applications are emerging, a new ultra-low resistance gate technology is required. This is the goal of this work.

We have developed a metal/polysilicon damascene gate technology implemented in an SOI LDMOSFET process (See Figure 16). Though promising in digital CMOS, the merits of the metal/polysilicon gate for RF power applications have never been previously demonstrated. The essential advantage of the metal/polysilicon damascene gate is that it is implemented in the back end of a fabrication process. This allows the use of metals with very high conductivity, such as aluminum or copper, enabling a gate sheet-resistance that is far lower than what can be achieved with refractory metals or refractory metal polycides, commonly used in CMOS devices. The metal/polysilicon damascene gate is also self-aligned and therefore, does not increase gate-to-source/drain overlap capacitance, as do aluminum gate strap technologies and T gates that have previously been used with LDMOSFETs.

The suitability of the metal/polysilicon damascene gate for RF power applications was evaluated by comparing the characteristics of an SOI LDMOSFET with a metal/polysilicon damascene gate to that of a co-processed SOI LDMOSFET with a degenerately-doped polysilicon gate. 0.6 μm long devices were fabricated. RF power load-pull measurements were performed at 1.9 GHz. The figure shows the gain and Power-Added Efficiency (PAE) for two typical devices with the different gate technologies. The use of the metal/polysilicon damascene gate greatly improves the gain and PAE, especially for large gate finger widths. For 90 μm finger width, as shown in the figure, the peak PAE is improved from 36% to 55%.

This work demonstrates that the metal/polysilicon damascene gate is very effective for RF power applications. It may prove to be a critical technology for enhancing RF LDMOSFET performance in present applications and for leading LDMOSFET technology to applications beyond 2 GHz.

Fig. 16: Left: sketch of fabricated RF power SOI-LDMOSFETs with metal/polysilicon damascene gate technology. Right: gain and power-added efficiency vs. output power of 0.6 µm SOI LDMOSFETs at 1.9 GHz. The use of a metal/polysilicon damascene gate greatly improves the gain and PAE of the device.

Partially- and Fully-Depleted Strained-Si/Strained-$Si_{1-y}Ge_y$ MOSFET's Fabricated on Relaxed $Si_{1-x}Ge_x$-On-Insulator (SGOI)

Personnel

Z. Cheng, J. Jung, A. J. Pitera, M. L. Lee, and H. Nayfeh (J. L. Hoyt, D. A. Antoniadis and E. A. Fitzgerald)

Sponsorship

Singapore-MIT Alliance (SMA) program, DARPA HGI program, A*STAR Fellowship

Two $Si_{1-x}Ge_x$-On-Insulator (SGOI) CMOS structures are studied: a surface channel strained-Si SGOI structure and a dual-channel (strained-Si/strained-$Si_{1-y}G_y$/relaxed-$Si_{1-x}G_x$) on SGOI structure. In a surface channel SGOI CMOS structure, the strained-Si surface channel provides mobility enhancement for both electrons and holes. To further boost hole mobility, a dual-channel structure can be utilized, where a compressively strained $Si_{1-y}Ge_y$ layer and then a tensile strained Si cap layer are grown on the relaxed $Si_{1-x}Ge_x$–On-Insulator (SGOI) substrate (y>x). The strained-Si layer is used as the electron channel layer for *n*-MOSFET's (surface channel) and the strained-$Si_{1-y}Ge_y$ is used as the hole channel for *p*-MOSFET's (buried channel). *n*- and *p*-MOSFET's SGOI structures were demonstrated in this work. The gate oxide thickness was 5 nm.

Partially depleted surface strained-Si *n*- and *p*-MOSFETs show well-behaved characteristics, with mobilities comparable to those measured on bulk relaxed SiGe virtual substrates, as shown in Figure 17. However, the measured sub-threshold swing for *fully-depleted devices* is larger than that of partially-depleted SGOI MOSFETs. This effect is related to traps at the interface between the relaxed $Si_{0.78}Ge_{0.22}$ and the buried oxide. The measured interface trap density at this bonding interface is 5.2E12 $cm^{-2}eV^{-1}$.

Dual-channel structures consisting of strained-Si/strained-$Si_{0.4}Ge_{0.6}$/relaxed-$Si_{0.7}Ge_{0.3}$ on SGOI were also fabricated. Although the hole mobility was enhanced, the enhancement was dramatically reduced for devices that received an 850C-30 min source/drain annealing step compared to those annealed at 600°C.

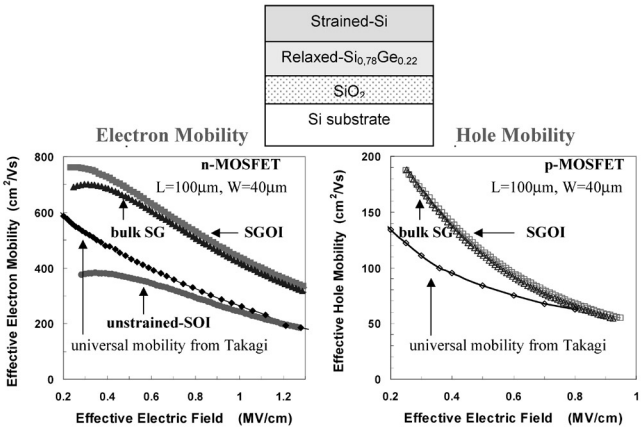

Fig. 17: Partially depleted surface strained-Si n- and p-type MOSFETs on relaxed SGOI substrates show enhanced electron and hole mobilities comparable to those measured on bulk SiGe virtual substrates (bulk SG).

InP-HEMTs for Ultrahigh-Frequency Power Devices

Personnel
T. Suemitsu (J. A. del Alamo)

Sponsorship
NTT

InP High Electron Mobility Transistors (HEMTs) exhibit highest speed characteristics in any kind of transistor. Indeed, a cutoff frequency of over 400 GHz and a maximum frequency of oscillation of over 600 GHz have been reported so far. These high-frequency characteristics are realized by means of the particular property of this material system such as the high electron mobility of InGaAs and large carrier concentration produced by the InAlAs/InGaAs quantum well. The small bandgap of InGaAs, however, leads to a large impact ionization rate at relatively low drain voltages that is regarded as a cause of low breakdown voltage of InP-HEMTs. Generally speaking, the breakdown voltage and the speed performance are a trade-off because the former decreases with, but the latter is improved by, reducing the gate length. Mitigating this trade-off is, therefore, a key issue to help the design of the ultrahigh-speed InP-HEMT circuits, particularly for high-power applications.

Although the physical mechanism of the breakdown is still under investigation, the detailed study using numerical analysis tells us that the accumulation of impact-ionized holes in the body of the device plays an important role on the breakdown. Since the device is surrounded by the n-type ohmic contacts and the semi-insulating buffer, holes are difficult to be extracted from the body of the device. This situation results in the accumulation of holes under the gate that shifts the threshold voltage of the devices. Similar effects are observed in the Silicon-On-Insulator (SOI) MOSFETs, for which the body contact is found to be an effective way to enhance the breakdown voltage.

The InP material system usually consists mainly of arsenides (InAs, GaAs, and AlAs), and it occasionally contains phosphides (InP, GaP, and AlP) for some purposes. Another group of materials, antimonides (InSb, GaSb, and AlSb), on the other hand, has a unique property from the viewpoint of band engineering. The alloys of antimonides, such as GaAsSb and AlAsSb, have relatively high valence band energy that makes the type II junction to InGaAs. The type II junction enables us to produce the quantum well for holes separated from that of electrons and to make an additional electrode to extract the holes like the body contact in SOI MOSFETs.

An approach under consideration is shown in Figure 18. The GaAsSb layer underneath the InGaAs channel acts as the hole path as shown in the band profile in Figure 19. The additional contact to the GaAsSb layer, which is an extension of the source electrode in Figure 18, prevents the impact-ionized holes from accumulating in the body of the intrinsic device.

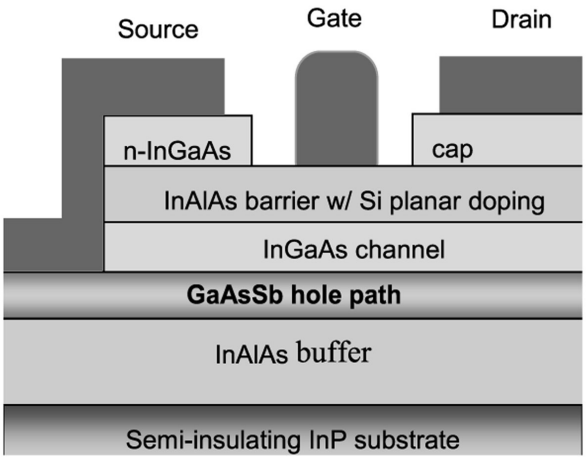

Fig. 18: Cross sectional view of InP-HEMT with hole collector.

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Hydrogen Degradation of InP High Electron Mobility Transistors

Personnel

S. D. Mertens (J. A. del Alamo in collaboration with T. Suemitsu and T. Enoki, NTT)

Sponsorship

NTT, Triquint, and ARL

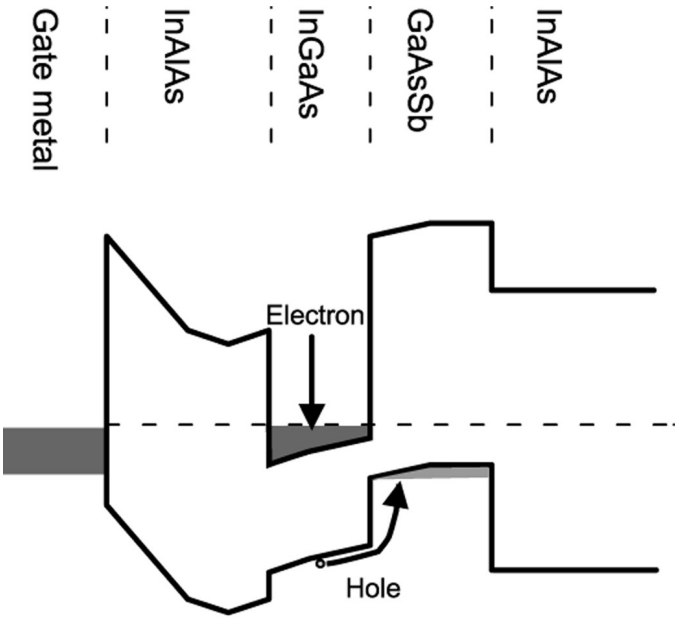

Fig. 19: Band profile of heterostructure under gate.

GaAs and InP High Electron Mobility Transistors (HEMT) hold promise for ultra-high-speed photonics and millimeter wave power-applications. A major reliability concern in some of these devices is the shift of the threshold voltage that is observed when the device is exposed to hydrogen. The goal of this project is to understand this reliability problem and find device level solutions to mitigate it.

Recent research at MIT has shown that H exposure results in the formation of TiH_x in Ti/Pt/Au gates. This produces compressive stress in the gate, which generates a tensile stress in the heterostructure underneath. The resulting piezoelectric polarization charge in the semiconductor causes a threshold voltage shift. For InP HEMTs with Ti/Pt/Au gates of short gate lengths (around 0.1 μm) shifts of several hundred mV have been observed.

In this project, we developed a model for H-induced piezoelectric effect in InP HEMTs that explains the gate length dependence of ΔV_T and provides design guidelines for minimizing H sensitivity. Our modeling approach involves: i) performing two-dimensional mechanical stress simulations in typical heterostructures, ii) computing the resulting piezoelectric charge, and iii) estimating its effect on V_T. Figure 20 shows the piezo-electric charge distribution that is induced in an InP HEMT by an expansion of its 1 μm gate. This calculation framework provides results that are consistent with the experimental measurements and illuminates the key dependencies of ΔV_T on heterostructure and gate design.

We are currently studying InAlAs/InGaAs HEMTs with a thick Ti-layer in the Ti/Pt/Au gate stack. One would expect a very large H-induced piezoelectric ΔV_T in these devices. A thick expanding layer would induce a lot of mechanical stress in the semiconductor, which would result in significant piezoelectric charge underneath

continued

continued

the gate and thus, a large ΔV_T. However, we found that the impact of hydrogen on the threshold voltage of these devices is one order of magnitude smaller than conventional Ti/Pt/Au-gate HEMTs. This can be explained if the formation of TiH_x only occurs in a thin sheet close to the Ti/Pt interface. We have confirmed this through Auger Electron Spectroscopy experiments. Our simulations are also consistent with this picture. They suggest that the separation of the expanding TiH_x-layer from the semiconductor by the thick Ti-layer significantly reduces the stress in the device heterostructure and thus ΔV_T, as is shown in Figure 20.

This work will allow us to better understand the impact of layer structure and gate design on the H-induced V_T shift in GaAs and InP HEMTs. Our ultimate goal is device design guidelines that minimize the H sensitivity of these devices.

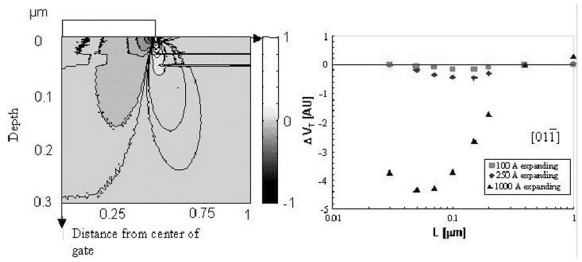

Fig. 20: The left figure shows the relative 2D piezoelectric charge distribution in a 1 μm InP HEMT stressed by an expanding gate. Only half of the device is simulated, as the other half shows a symmetric charge distribution. The right figure shows the calculated value of ΔV_T vs. gate length for an InP HEMT with a Ti/Pt/Au gate stack with a thick Ti layer. Three data sets are shown: 1) the complete Ti layer expands, 2) only the top 250 Å of the Ti layer expands' and 3) only the top 100 Å of the Ti layer expands.

Electrical Reliability of RF Power GaAs PHEMTs

Personnel

A. A. Villanueva (J. A. del Alamo in collaboration with T. Hisaka and K. Hayashi, Mitsubishi Electric)

Sponsorship

Mitsubishi Electric and Lucent Technologies Fellowship

GaAs pseudomorphic High-Electron Mobility Transistors (PHEMTs) have great potential for RF power applications. A major concern with these devices is their gradual degradation that occurs as a result of biasing the device at high voltages for extended periods of time. Although previous research has linked the electrical degradation to impact ionization and hot carrier effects, the details of the underlying physical mechanisms are not known. The goals of this research project are to provide a fundamental physical understanding of the electrical degradation in these devices, and to suggest design strategies that mitigate these effects.

In our study, experimental RF power PHEMTs (non-commercial devices provided by our sponsor, Mitsubishi Electric) were electrically stressed at room temperature. A stressing scheme that keeps the impact ionization rate constant was utilized. Specifically, this consisted of keeping the drain current I_D constant, and the intrinsic drain-to-gate voltage V_{DGo} constant (relative to the threshold voltage). In order to maximize the productivity of our experiments, the bias voltage $V_{DGo}+V_T$ was initially set at a high voltage and then stepped up in regular time periods. During stressing, the devices were characterized at frequent intervals.

Our results showed several forms of degradation; the most significant changes being in the drain resistance, the source resistance, and the threshold voltage. After initial short transients, R_D increased while R_S decreased, and V_T decreased (See Figure 21). Throughout our experiments, we have found these three phenomena to be uncorrelated with one another. In an attempt to isolate all the different degradation mechanisms involved, we also performed stressing experiments on Transmission-Line Model (TLM) structures. TLMs are much simpler devices to study degradation, since they have the same structure as a PHEMT, but do not have a gate (and thus are less complicated to characterize and analyze). Our main observations from the TLM degra-

continued

dation experiments (an initial increase in sheet carrier concentration, followed by ohmic contact degradation) were found to be correlated to corresponding mechanisms in PHEMTs.

Our general findings are that there are three independent mechanisms affecting the three regions of the device: the source, the drain, and the gate. The decrease in R_S can be explained by an increase in sheet carrier concentration on the source side. The increase in R_D can be attributed to ohmic contact degradation, and possibly a decrease in sheet carrier concentration on the drain side. The decrease in V_T can be explained by charge modulation underneath the gate—most likely, hot holes generated by impact ionization neutralizing trapped electrons in the AlGaAs layer. More experiments are being performed to identify the physical causes of these effects.

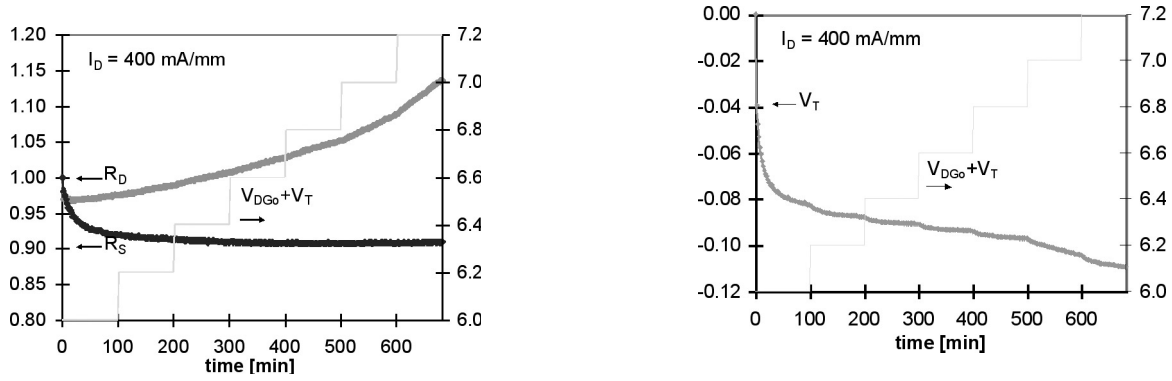

Fig. 21: Time evolution of the normalized drain resistance and source resistance (left) and change in threshold voltage (right), for a voltage step-stress experiment on a PHEMT at constant drain current of 400 mA/mm.

Coplanar Integration of Lattice-Mismatched Semiconductors with Silicon by Wafer Bonding Ge/SiGe/Si Virtual Substrates

Personnel

A.J. Pitera, G. Taraschi, M. L. Lee, C. W. Leitz, and Z. Cheng (E. A. Fitzgerald)

Sponsorship

ARO, DARPA, and Heterogeneous Integration Program

The current challenge in monolithic integration of lattice-mismatched semiconductors with CMOS is fabrication of high-quality device layers on Si substrates. Using SiGe compositional grading to pure Ge, high-quality (TDD=10^6 cm^{-2}) Ge and GaAs can be realized on a Si wafer. These virtual substrates have enabled monolithic integration of the first compound semiconductor laser and the first optical circuit on a Si substrate. More practical hetero-integration with CMOS requires removal of the thick (~10μm) graded buffer. One solution is film transfer using wafer bonding. However, traditional wafer bonding is limited to small diameter substrates due to the size mismatch between bulk Si and Ge/III-V wafers. Using Ge virtual substrates, Ge or GaAs films can be transferred to Si from large diameter wafers while eliminating the large thermal strain energy that arises during bulk wafer bonding. We have successfully transferred monocrystalline Ge films from Ge virtual substrates to Si with the aid of a SiO_2 CMP layer and the SmartCut™ process. Difficulty in CMPing thin Ge layers requires a novel approach for removal of the exfoliation-damaged Ge layer. Therefore, a buried $Si_{0.4}Ge_{0.6}$ etch-stop layer was used to selectively etch the damaged Ge surface after layer transfer. The final result is a Ge On Insulator (GOI) structure fabricated using an epitaxial Ge transfer process which takes advantage of the full wafer diameter of Si. (See Figure 22)

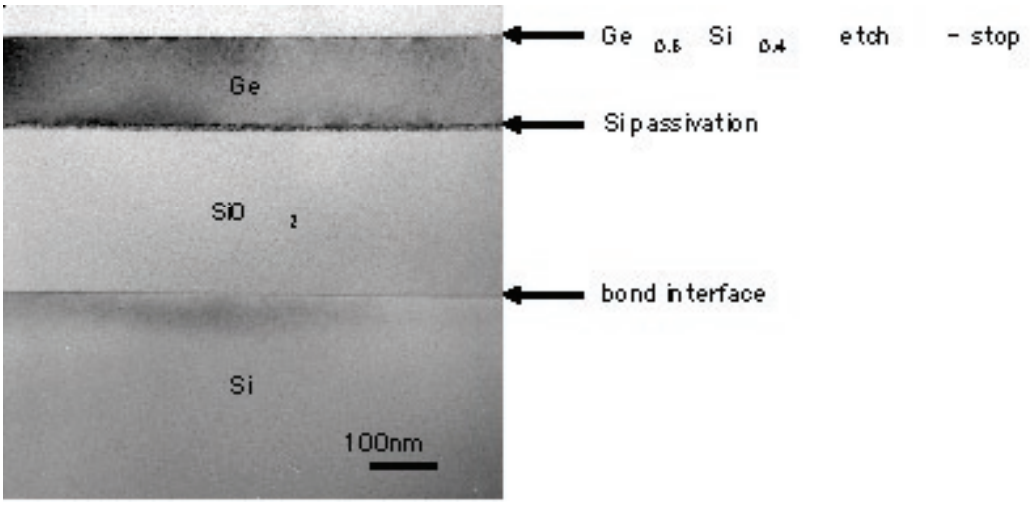

Fig. 22: Ge on Insulator (GOI) structure fabricated by wafer bonding and epitaxial layer transfer from a Ge/SiGe/Si virtual substrate.

CMOS-like Fabrication of InP-HEMTs for 100 Gbit/s Photonics Applications

Personnel
J. Knoch (J.A. del Alamo)

Sponsorship
SRC, Triquint, ARL, and IBM

InP High-Electron Mobility Transistors (HEMTs) have been shown to exhibit the fastest transistor operation of any microelectronics technology. It is believed that InP-HEMT-technology is the only one suitable for fiber optics communication systems at 100 Gbit/s operation and beyond. However, InP-HEMTs suffer from low reliability and manufacturability since the evolution of these devices has mostly been driven by millimeter-wave rather than photonics applications. This is reflected in the fact that only recently, digital ICs for 40 Gbit/s optical fiber communications systems have been demonstrated with a complexity of ~10^2 gates. On the other hand, CMOS-technology is the most advanced microelectronics technology, having achieved integration levels of order ~10^7 gates recently. Hence, it is appealing to explore the possibility of using CMOS-like process techniques for the fabrication of InP-HEMTs.

This project deals with the development of a CMOS-like, fully self-aligned process technology for InP-HEMTs that aims to achieve improved device manufacturability and reliability. In particular, fabrication techniques such as a fully planar process by means of chemical-mechanical polishing, the use of spacers for self-alignment and electroplating, play a key role in this project. Figure 23 shows a cross-section of a tentative device design. This particular design exhibits three main features: i) a shallow-trench-isolation (STI), ii) a self-aligned, high aspect ratio gate, and iii) non-alloyed ohmic contacts.

The benefits of this design are as follows: 1) the shallow-trench isolation provides for device isolation while keeping the wafer surface flat and minimizing parasitic capacitance; 2) the use of spacers allows the generation of a small gate footprint from a larger mask opening that is self-aligned to source and drain; 3) non-alloyed ohmic contacts have a smooth surface and allow well-defined contact geometries, mandatory for scaling-down the devices. As a further benefit of this device design, the gate recess region – known to cause reliability problems – is always covered.

The high manufacturability of InP-HEMTs achievable with the proposed CMOS-like device and process architecture will enable us to significantly improve the reliability, as well as, the uniformity of these devices needed in order to realize complex integrated circuits operating at 100 Gbit/s and beyond.

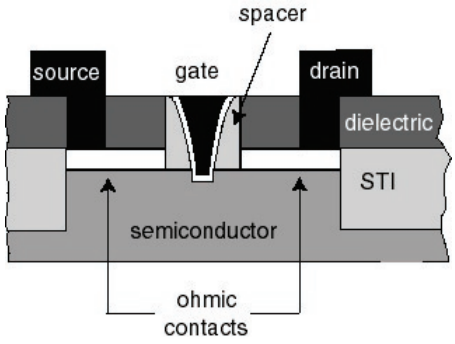

Fig. 23: Cross-sectional view of a tentative device design for an InP-HEMT fabricated using a CMOS-like process.

Nanomagnets and Magnetic Random Access Memories

Personnel

F.J. Castaño, Y. Hao, M. Walsh, D. Gil, A. Eilez, E. Lyons, and W. Jung (C.A. Ross and H.I. Smith in collaboration with F. Humphrey, M. Redjdal, Boston University, and J. Bland, Cambridge University)

Sponsorship

Cambridge-MIT Institute and NSF

We are using a variety of lithography techniques (electron-beam lithography, interference lithography, block copolymer lithography and X-ray lithography) to produce arrays of pillars, bar-shaped, and ring-shaped 'nanomagnets'. These tiny structures have thicknesses of a few nanometers and lateral dimensions typically smaller than 100 nm. Arrays of these elements are made with spatial periods of 100 nm and above. Nanomagnets have been made by electrodeposition, by evaporation and liftoff, or by etching of a sputtered film. We are exploring the switching mechanisms of the particles, the thermal stability of their magnetization, and interparticle interactions, and we are assessing their suitability for various data-storage schemes. The behavior of individual particles can be measured using magnetic-force microscopy, while the collective behavior of arrays of particles can be measured using magnetometry. Comparison of these data shows how the behavior of one magnet is affected by its neighbors, and how much intrinsic variability there is between the particles as a result of microstructural differences. We have also performed micromagnetic simulations to explore the remanent magnetic states, and mechanisms for magnetization reversal in these structures. Small particles have near-uniform magnetization states, while larger ones develop more complex structures such as magnetization vortices or domain walls. Good agreement is obtained between modelled and observed remanent states, taking the shape and crystal orientation into account. We are investigating, in particular, the behavior of multilayered nanomagnets, magnetoresistive structures, and the effects of patterning on strain in magnetostrictive films.

These nanomagnets have potential uses in 'patterned media', Magnetic-Random-Access Memories (MRAM) and other magneto-electronic applications. Current MRAM devices rely on bar-shaped multi-layered magnetoresistive nanomagnets in which a bit of data is stored, depending on the relative orientation between the magnetization of the different magnetic layers in the structure. An alternative possibility for high-density MRAMs is to use a ring-shaped nanomagnet, in which a bit of information is stored by magnetizing the ring clockwise or counterclockwise.

As an example, we have explored, for the first time, the magnetic switching mechanisms of rings with deep sub-micron dimensions (See Figure 24). The experimental results reported to date on micron-sized ring magnets support the existence of just two different magnetic states: one being the flux-closure or 'vortex' state (with clockwise or counter-clockwise magnetization) and the other a state with two domain walls, known as an 'onion' state. Unexpectedly, we found that magnetic rings with small diameters display new metastable states, called twisted states, consisting of a vortex state containing a 360° wall (See Figure 25). The existence of twisted states in nanorings has interesting consequences for the design of magnetoelectronic devices. We are measuring the magnetoresistance of these structures with the aim of incorporating them into magnetic memory or logic devices.

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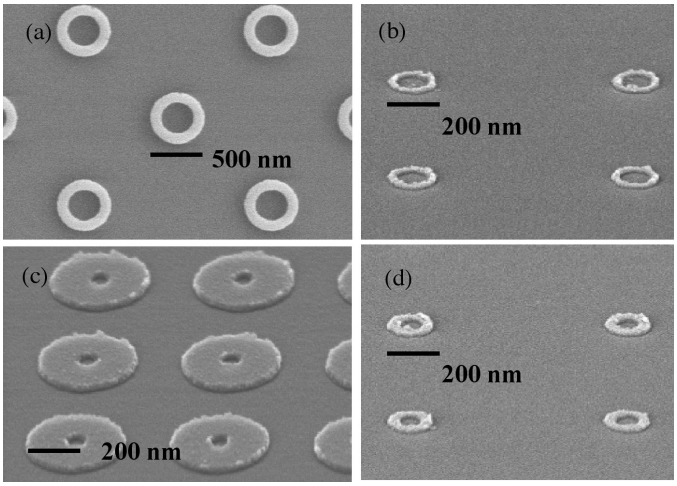

Fig. 24: Plan-view and tilted scanning-electron micrographs of four arrays of Co rings with diameters and linewidths of (a) 520 nm and 120 nm, (b) 190 nm and 30 nm, (c) 360 nm and 160 nm, (d) 180 nm and 50 nm.

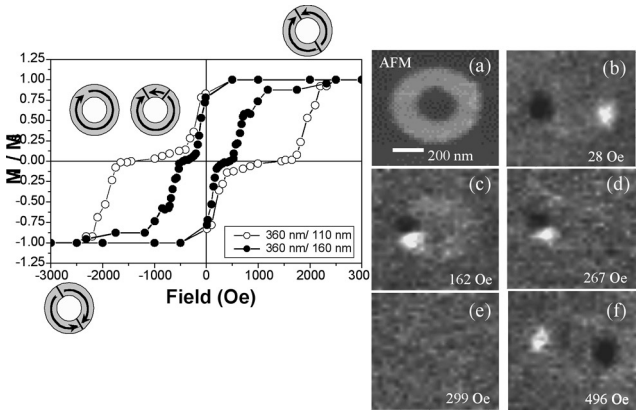

Fig. 25: At left, hysteresis loops calculated from magnetic force microscopy data, as well as a schematic representation of the different magnetic states present in Co nanorings with outer diameter of 360 nm and widths of 110 nm and 160 nm (onion state, top right and bottom left; twisted and vortex states at center). On the right, data from a 520 nm-diameter ring: (a) an atomic force micrograph. (b-f) a sequence of MFM images measured at remanence after first saturating the sample at 1000 Oe, then applying and removing a reverse field of (b) 28 Oe, (c) 162 Oe, (d) 267 Oe, (e) 299 Oe and (f) 496 Oe. After saturation, the ring is in an onion state which is characterized by dark and light contrast at opposite sides of the ring originating from the two domain walls. At a reverse field of 299 Oe, the ring 'disappears' from the image as a vortex state forms, Fig. 25(e). However, over a range of fields smaller than that needed to produce the vortex state, a new state is visible, which we call a twisted state. This state, which can be seen in Fig. 25(c) and (d), is characterized by adjacent light and dark contrast at one side of the ring. Fig 25(f) shows the reversed onion state.

AlGaAs/GaAs HBT with enhanced forward diffusion

Personnel

K. Konistis (Q. Hu and C.G. Fonstad in collaboration with M. Melloch at Purdue University)

Sponsorship

AFOSR

One of the key limits of high-frequency operation of bipolar transistors is the base transient time, which is proportional to the square of the base width when the base transport is dominated by diffusion. Consequently, high-frequency bipolar transistors tend to use thin bases (<100 nm) that result in a short base transient time and a high cut-off frequency f_T. However, for high frequency operations, it is not the current gain that matters most. Rather, it is the unilateral power gain that determines the operating frequency of any three-terminal devices. The frequency f_{max}, at which the power gain is unity, is determined by both f_T and RC time constant. Because of the peculiar geometry of bipolar transistors, the electrical contact to the base is always made from the side. Thus, a thin base, which is important to yield a high f_T, will inevitably result in a high sheet resistance and a lowering of f_{max}. It is this difficult trade-off between f_T and f_{max} that led Prof. S. Luryi and his co-workers to propose a novel heterostructure bipolar transistor, whose band diagram is shown in Figure 26.

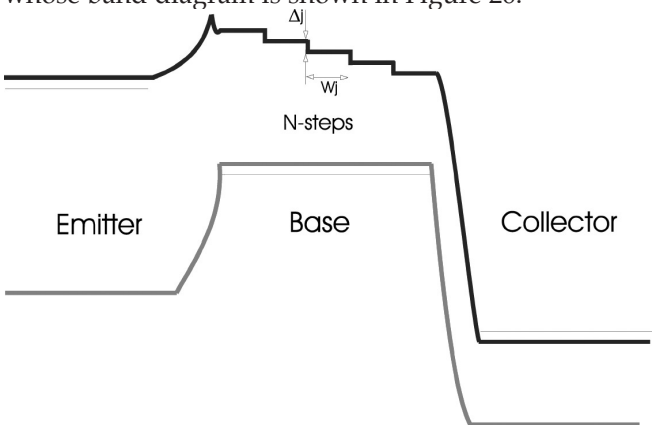

Fig. 26: Energy band diagram of an HBT with stepwise base. The energy drop Δ at each step is slightly greater than the LO-phonon energy (36 meV) in GaAs. Thus, electrons encounter very fast LO-phonon emission scattering (with a time ~0.1 ps) when they go over the edge of a step. Consequently, backward diffusion is significantly reduced and forward diffusion is enhanced.

The main feature of this novel HBT is that its base is graded like a staircase. The height of each step Δ is slightly greater than the LO-phonon energy in GaAs (36 meV). Thus, electrons will encounter very fast LO-phonon emission scattering (with a time ~0.1 ps) when they go over the edge of a step. Consequently, backward diffusion is significantly reduced. In a way, the edge of each step resembles and performs a similar function as the base-collector interface; any injected excess minority carrier will be quickly swept down the energy potential. As a result, each step acts like a minibase as far as the diffusion transport is concerned. The resulting minority carrier concentration assumes a nearly periodic distribution, provided that the energy drop is greater than the sum of LO-phonon and thermal energy to ensure a fast scattering and prohibit backward diffusion. The total base transient time is, therefore, approximately N times the transient time of each step, whose width can be as narrow as 30 nm, yielding a high f_T. On the other hand, all the N steps are connected in parallel for the base contact, reducing the base resistance by an approximate factor of N. The combination of a thin effective base and small base resistance will yield a high f_{max}.

One interesting result of our analysis is the existence of resonances of the unilateral power gain. Their physical mechanism is closely linked with the current-phase delay. A base structure introduces both phase delay and magnitude attenuation of current. As the frequency of operation increases, the phase delay increases, and at a certain frequency, the voltage and current acquire opposite phases which will yield a resonance if the amplitude attenuation is not too overwhelming. A short base offers small phase delay, and resonance occurs at high frequencies where the magnitude attenuation is strong. On the other hand, a long base may provide a large phase delay, but the heavy attenuation at low frequencies smooths out the unilateral gain peaks. For a multi-step base, the total phase delay is the sum of each step, while the total attenuation is the product of each

continued

step, enhancing the possibilities of achieving resonance. As can be seen in Figure 27, the unilateral power gain exhibits multiple resonances beyond typical cut-off frequencies (f_T) for multiple-step HBTs. These resonances can be achieved above 100 GHz, which is promising for the development of high-frequency amplifiers and fundamental oscillators.

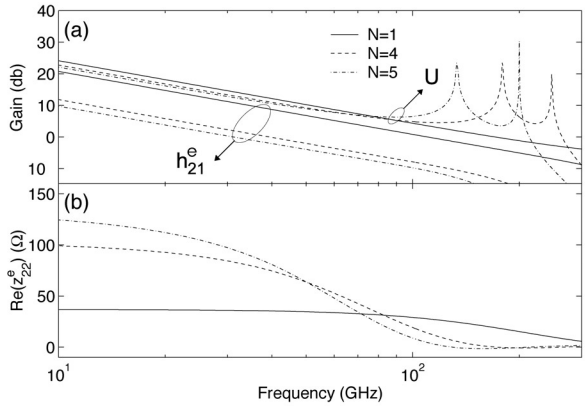

Fig. 27: (a) Unilateral power gain magnitude, current gain magnitude, and (b) output resistance for $X_{step} = 500Å$, $\Delta = 1.2\ \hbar\omega_{LO}$. As the number of steps increases (N = 1,4,5), U extends in frequency by means of resonance.

We have developed an elaborated process to fabricate very high-frequency HBTs using airbridges for electrode isolation. Figure 28 shows the schematic of the device and several SEM pictures taken from different angles. Electrical characterization of the devices will take place shortly.

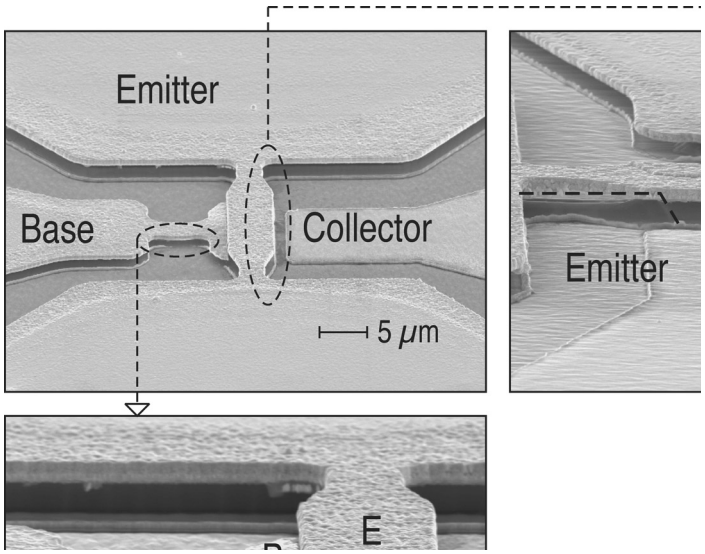

Fig. 28: Schematic and SEM pictures of a HBT device using airbridges for electrode isolation.

The MIT Microelectronics WebLab v. 5.0

Personnel

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Sponsorship

I-Campus (Microsoft)

The MIT Microelectronics WebLab (or WebLab for short) released its version 5.0 in the Spring of 2002. This latest release has been in use in educational assignments since September 2002 (See Figure 29).

WebLab allows the remote characterization of microelectronics devices using a Java applet running on a conventional web browser. Through WebLab, students from anywhere in the world and at any time of their choosing can operate an Agilent 4155B semiconductor parameter analyzer located at MIT and carry out current-voltage measurements of transistors and other semiconductor devices.

Release v. 5.0 features a new graphical interface and includes tools that simplify the management of the system in multiple courses with large numbers of students. The new graphical interface consists on a Java applet that uses the circuit language of electrical engineering to specify the experiment to be performed. This is much more intuitive than the text-based form that was utilized in previous versions of WebLab. The text-based approach, though inspired on the instrument interface, was found to be intimidating and to represent a significant barrier to first-time users. The new graphical interface hides away unnecessary details and eliminates clutter. This is also essential for the implementation of a collaboration system.

The latest release of WebLab also features a new remote management system that has been designed to allow the efficient use of the system in multiple subjects with large numbers of students. Through this system, the WebLab administrator can manage user accounts, user groups, device specifications, device access permissions, as well as examine a variety of system usage records. Additionally, the system features user self-registration and automatic e-mail notifications for users and administrators.

WebLab 5.0 was used in several courses in the Fall of 2002 and Spring of 2003 by nearly 700 students. About 280 of them were MIT students enrolled in two microelectronics subjects (120 in a junior level subject, both semesters, and 50 in a graduate subject). About 30 more graduate students used the system in an electronics materials course offered in Singapore (National Singapore University), and 350 more used in an undergraduate subject in microelectronics from Sweden (Chalmers University). About 10 additional students from industry used WebLab in various courses. In total, over 1300 students have used WebLab in lab assignments for credit since its first introduction in 1998.

The WebLab website can be found at http://weblab.mit.edu.

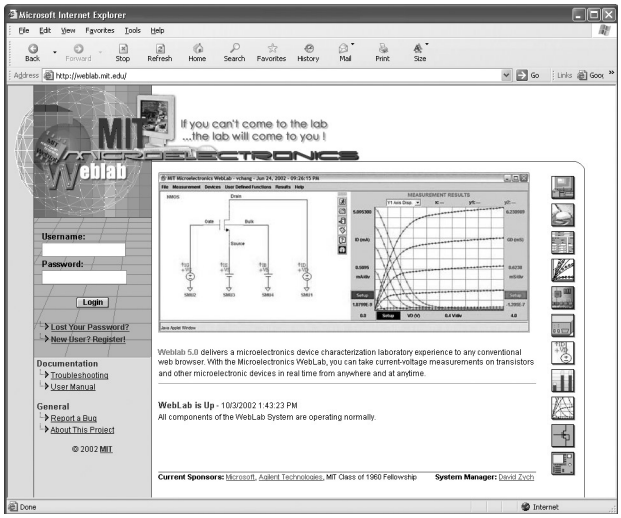

Fig. 29: Screen shot of WebLab 5.0 portal.