Microsystems Technology Laboratories Annual Report

December 2003

Massachusetts Institute of Technology
Cambridge, Massachusetts 02139-4307

Contents

continued

continued

Contents

Foreword

The Microsystems Technology Laboratories experienced an exciting phase of expansion this year. We saw substantial growth in the use of MTL infrastructure by campus researchers. In the past year, we have seen more than 350 students/staff using the cleanroom infrastructure, as well as a large number using the design infrastructure, and more than 100 students taking short courses supported by the labs. These investigators come from the research groups of 86 faculty and senior research staff at the Institute, representing nearly every department in the Schools of Science and Engineering. We maintain a technical staff of more than 20 engineers and technicians that sustain this infrastructure, as well as an administrative team that keeps the fiscal and personnel elements of the lab in good order.

I am pleased to mention some new additions for this year in the area of laboratory management. Prof. Judy Hoyt has joined the management team as a Faculty Associate Director. She will be focusing her attention on the vital cleanroom infrastructure, and providing valuable guidance as we navigate through complicated expansions and additions. Prof. Anantha Chandrakasan has also joined as a Faculty Associate Director to help in managing our industrial interactions and to provide valuable representation to the Circuits/Systems community. Judy and Anantha join Faculty Associate Director Prof. Duane Boning and Staff Associate Directors Dr. Vicky Diadiuk and Mr. Sam Crooks. We all look forward to their valuable input in the management of the labs.

We were also pleased to have Hewlett Packard join the Microsystems Industrial Group (MIG) this year. There is a great deal of mutual interest between the research groups in HP and the research portfolio in MTL, and we look forward to a sustained collaborative relationship.

The next several years pose many challenges and opportunities for our laboratories. We will be expanding the physical infrastructure in order to accommodate expanding programs in nanotechnology and systems biology. Coupled to this is a detailed assessment of the infrastructure and investments in upgrading our core services. In addition, we anticipate new and exciting research programs and people to be joining the MTL community.

As always, we are indebted to our hard-working staff. They maintain an exceptionally positive work environment that enables great things to happen.

Thank you.

Martin A. Schmidt
Director, Microsystems Technology Laboratories
School of Engineering
Professor, Electrical Engineering and Computer Science
October 2003

Acknowledgements

All of us at MIT are grateful to the following organizations for their generosity and participation in the Microsystems Industrial Group (MIG). Their membership makes possible the continuing operations of the Microsystems Technology Laboratories:

Advanced Micro Devices
Analog Devices
Applied Materials
Hewlett-Packard
IBM Corporation
Intel Corporation
Motorola Incorporated
National Semiconductor
Novellus Systems, Incorporated
Taiwan Semiconductor Manufacturing Corporation
Texas Instruments, Inc.

We would also like to acknowledge past support of the Microsystems Technology Laboratories by the following organizations:

Agere Systems
Compaq Computer Corporation
Delco Electronics Corporation
Eaton Ion Beam Systems Division
The Charles Stark Draper Laboratories
Ford Motor Company
GCA Corporation
General Electric Company
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Hughes Research Laboratories
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Rockwell
Raytheon Corporation
Sanders Associates, Inc.
Teradyne Incorporated
United Technologies Corporation

We also wish to acknowledge the support of those organizations who have generously contributed equipment for use at the Microsystems Technology Laboratories:

Agere Systems
Analog Devices
Applied Materials
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GCA Corporation
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Research Sponsors

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- Cambridge-MIT Initiative (MIT)
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  Air Force Office of Scientific Research (AFOSR)
  Army Research Office (ARO)
  Defense Advanced Research Projects Agency (DARPA)
  Defense University Research Initiative on Nanotechnology (DURINT)

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Acknowledgements

- Department of Defense *(continued)*
  - DARPA Bio-Info-Micro
  - Institute for Soldier Nanotechnology (ISN)
  - Joint Service Electronics Program (JSEP)
  - Office of Naval Research (ONR)
  - Multidisciplinary University Research Initiative (MURI)
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- MEC Fellowship
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- Microphotonics Center (IMIT)
- Microsoft MIT Alliance (I-Campus)
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  - Analog Devices
  - IBM
  - Infineon
  - Lucent Technologies
  - Maxim Integrated Products
  - National Semiconductor
  - Philips
  - Silicon Laboratories
  - Teradyne
  - Texas Instruments
- Mitsubishi Electric
- National Institute for Standards and Technology (NIST)
- National Institutes for Health
- National Science and Engineering Research Council of Canada Postgraduate Scholarship
- National Science Foundation
  - NSF Career Award
  - NSF Center for Bits and Atoms
  - NSF Center for Materials Science and Engineering (CMSE) (MIT)
  - NSF Fellowship(s)
  - NSF GOALI Program
  - NSF MRSEC
  - NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing
- National Semiconductor
  - National Semiconductor Fellowship
- National Aeronautics and Space Administration (NASA)
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- Novartis Foundation
- NTT
- Panasonic Boston Laboratory
- PDF Solutions
- Pirelli Lab S.p.A.
- Praesagus, Inc.
- QED, Incorporated
- Rockwell Scientific Corporation
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  - SRC Fellowship(s)
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- Universal Display Corp.
- U.S. Department of Transportation (DOT)
- Vitesse Semiconductor
- Walsin-Lihwa Corporation
- X-OPT, Incorporated

Research Interests of Faculty and Principal Research Scientist

	Research Areas	Office Telephone Net Address
A. I. Akinwande	Flat panel displays,Vacuum Microelectronics and its application to flat panel displays, RF power sources, and sensors. Wide bandgap semiconductors and applications to flat panel displays, UV emitters and RF power sources.	39-553A 258-7974 akinwand@mtl.mit.edu
D. A. Antoniadis	Advanced FET devices for high-speed and low-power CMOS integrated circuits including Silicon-on-Insulator, Si-Ge alloy heterostructures, and double-gated channels. Research involves experimental device fabrication, measurements, and modeling.	39-415b 253-4693 daa@mtl.mit.edu
M. Baldo	Interests include molecular electronics and fundamental physical processes in organic semiconductors, with a particular focus on protein-molecular complexes and spin determination during exciton formation. Device applications include transistors and diodes, and LEDs and photodetectors.	13-3053 452-5132 baldo@mit.edu
D. Boning	Semiconductor and MEMS manufacturing technology. Chip-scale and pattern-dependent modeling of chemical-mechanical polishing, electroplating, and plasma etch. Variation characterization and reduction in silicon, MEMS, and optoelectronic processes, devices, interconnects, and circuits. Run by run and feedback control for quality and environment in semiconductor fabrication.	39-567B 253-0931 boning@mtl.mit.edu
V. Bulovic	Physical properties of organic thin films, structures, and devices. Optoelectronic, electronic, and photonic organic devices of nanoscale thickness, including LEDs, lasers, solar cells, photodetectors, transistors, memory cells, and chemical sensors. Hybrid organic/inorganic materials and structures. Molecular electronics. Nanopatterning and nanostructured materials.	13-3138 253-7012 bulovic@mit.edu
A. P. Chandrakasan	Design of digital integrated circuits and systems. Emphasis on the energy efficient implementation of distributed microsensor and signal processing systems. Protocols and Algorithms for Wireless Systems. Circuits techniques for deep sub-micron technologies.	38-107 258-7619 anantha@mtl.mit.edu

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Research Interests of Faculty and Principal Research Scientist

	Research Areas	Office Telephone Net Address
J. A. del Alamo	Microelectronics technologies for gigahertz and gigabit-per-second communication systems: physics, modeling, technology and design. Technology and pedagogy of online laboratories for engineering education.	39-415a 253-4764 alamo@mit.edu
M. S. Dresselhaus	Electron transport properties and thermoelectricity of low dimensional systems (2D quantum well superlattices and 1D quantum wires). Electronic, vibrational and optical properties of carbon and related materials, including Raman spectroscopy from one isolated carbon nanotube.	13-3005 253-6864 millie@mgm.mit.edu
E.A. Fitzgerald	Low defect density relaxed SiGe buffer layers on Si; high mobility strained Si heterostructures; InGaP and GaAs integration on Ge and Si; fabrication of GeSi/Si detectors and InGaAs/GaAs emitters; visible AlInGaP LEDS and lasers integrated on Si; III-V solar cells integrated on Si; integration of thin film batteries with CMOS; basic studies concerning the generation, propagination, and interaction of defects in heterostructures; investigations of microscopic failure mechanisms in optoelectronic and electronic devices.	13-5133 258-7461 eafitz@mit.edu
C. G. Fonstad, Jr.	Compound semiconductor heterostructure materials, devices, and physics. Optoelectronics. Heteroepitaxy, bonding, and monolithic heterogeneous integration. Laser diodes, photodetectors, quantum well devices, and optoelectronic integrated circuits. Microscale thermo-photovoltaics.	13-3050 253-4634 fonstad@mit.edu
K. K. Gleason	Deposition and characterization of thin films for low dielectric constant, biopassivation, and dry resist applications. Hot filament and pulsed plasma enhanced Chemical Vapor Deposition (CVD).	66-352 253-5066 kkg@mit.edu
J. Han	BioMEMS, biomolecule analysis, microfluidics, and nanofluidics, integrated chemical and biological analysis systems.	36-841 253-2290 jyhan@mit.edu
J. L. Hoyt	Novel processes, materials, and device concepts for silicon technology. Device physics and epitaxial growth (chemical vapor deposition) of silicon-based heterostructures and nanostructures. Strained Si MOSFETs, heterojunction bipolar transistors, CMOS front-end processing, and three-dimensional device integration.	39-427A 452-2873 jlhoyt@mtl.mit.edu

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Research Interests of Faculty and Principal Research Scientist

	Research Areas	Office Telephone Net Address
Q. Hu	High-frequency and high-speed electronic devices, including terahertz quantum-cascade lasers, millimeter-wave heterstructures and bipolar transistors, and on-chip THz tranceivers.	36-465 253-1573 qhu@mit.edu
K. Jensen	Microfabrication and characterization of devices and systems for chemical synthesis and detection, hydrocarbon fuel conversion to electrical energy, bioprocessing, and bioanalytics. Multiscale simulation of transport and reaction processes. Chemical vapor deposition of polymer, metal, and semiconductor thin films. Synthesis and characterization of quantum dot composite materials.	66-566 253-4589 kfjensen@mit.edu
S. G. Kim	Nanomanufacturing, MEMS for optical devices, strain-tunable microphotonic devices, RF switches, piezoelectric micro power generation and energy harvesting, carbon nanotube assembly and nanopelleting.	1-310 452-2472 sangkim@mit.edu
L.C. Kimerling	Silicon integrated circuit materials and processes. Heterostructures; optoelectronic devices; and optical waveguides for Silicon Microphotonics. Photovoltaic cells and solar electricity. SiO_2; high k dielectrics; Si; SiGe; III-V compounds and alloys. Environmentally benign semiconductor manufacturing. Chemical kinetics and equilibria at surfaces.	13-4118 253-5383 lckim@mit.edu
L. A. Kolodziejski	Gas source molecular beam epitaxy of III-V compound semiconductors, optoelectronic devices: lasers, optical switches, saturable absorber Bragg mirrors, and fabrication of 1D and 2D photonic bandgap crystal structures.	13-3065 253-6868 leskolo@mit.edu
J. H. Lang	Analysis, design and control of electromechanical systems. Application to traditional electromagnetic actuators, micron scale actuators and sensors, and flexible structures.	10-176 253-4687 lang@mit.edu
H.-S. Lee	Analog and mixed-signal integrated circuit design with the emphasis on data converters, amplifiers, and communication circuits.	39-553B 253-5174 hslee@mtl.mit.edu
S. Manalis	Application of micro- and nanofabrication technologies towards the development of novel methods for probing biological systems. Current projects focus on electrical and mechanical detection schemes for analyzing DNA, proteins, and cells.	E15-422 253-5039 scottm@media.mit.edu

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Research Interests of Faculty and Principal Research Scientist

	Research Areas	Office Telephone Net Address
I. Masaki	VLSI architecture. Emphasis on interrelationship among applications, systems, algorithms, and chip architectures. Major application fields include intelligent transportation systems, video, and multimedia.	38-107 253-8532 masaki@mtl.mit.edu
T. P. Orlando	Superconductivity. Quantum computation with superconductors. Nonlinear dynamics of arrays of Josephson junctions.	13-3006 253-5888 orlando@mit.edu
D. Perreault	Circuit design, power electronics and energy conversion, and control. Applications to industrial, commercial, transportation, and biomedical systems.	10-039 258-6038 djperrea@mit.edu
M. Perrott	High speed circuit design involving analog, digital, and mixed-signal integrated circuits. Simulation techniques for phase-locked loops and other communication circuits. Applications to wireless, wireline, and optical networking systems.	38-344 452-2889 perrott@mtl.mit.edu
R. Reif	Integrated circuit fabrication technology. New process technologies for VLSI. Environmentally conscious manufacturing. Novel interconnect technologies.	38-401 253-7317 reif@mtl.mit.edu
C. Ross	Magnetic films and structures for data storage, nanostructures based on self-assembly processes.	13-4005 258-0223 caross@mit.edu
R. Sarpeshkar	Bioelectronics: Ultra Low Power analog VLSI for bionic systems, mixed-signal computing systems, and sensory systems.	38-294 258-6599 rahuls@mit.edu
M. L. Schattenburg	Advanced lithography, including X-ray, electron-beam, ion-beam, and optical. Nanotechnology and nanofabrication. Precision engineering and nano-accuracy dimensional metrology. Advanced interference lithography technology for super-accurate patterning of general grating and grid patterns. Micro and nanometer fabrication technology applied to advanced astronomical and laboratory instrumentation. Silicon micromachined structures applied to high-precision optical assembly. X-ray optics and instrumentation.	37-487 258-0223 marks@space.mit.edu http://snl.mit.edu

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Research Interests of Faculty and Principal Research Scientist

	Research Areas	Office Telephone Net Address
M. A. Schmidt	MicroElectroMechanical Systems (MEMS). Microfabrication technologies for integrated circuits, sensors, and actuators. Design of microsensor and microactuator systems.	39-521 253-7817 schmidt@mtl.mit.edu
H. I. Smith	Nanofabrication, nanostructures and metrology. Integrated-optical, photonic-bandgap, high-density-magnetic, and short-channel devices. E-beam, X-ray, deep UV, and interferometric lithography. Diffractive optics for photons and neutral atoms.	39-427B 253-6865 hismith@nano.mit.edu
C. G. Sodini	Design of technology intensive microsystems emphasizing integrated circuit design at the device level. Specific systems of interest include low power wireless cameras and displays, high data rate wireless LANs and low data rate wireless sensor systems.	39-527 253-4938 sodini@mtl.mit.edu
S. M. Spearing	Materials and Process Selection for MEMS; Structural design of MEMS. Mechanical testing of microfabricated materials. Microfabricated refractory material process development. Residual stress determination and reduction. Wafer bonding. Membrane structures. MEMS Packaging. Power-producing MEMS.	33-318 253-4467 spearing@mit.edu
C. V. Thompson	Processing and properties of thin films and nanostructures for applications in electronic and electromechanical micro- and nano- devices and systems. Control of stress and mechanical properties in thin films for MEMS. Interconnect reliability. Controlled growth of systems of nanostructures.	13-5069 253-7652 cthomp@mtl.mit.edu
D. E. Troxel	Applications of digital systems. Computer-aided fabrication of integrated circuits. Computer-assisted prototyping of advanced microsystems. Remote inspection of ICs and MEMS devices. Reliability of interconnect.	36-287 253-2570 troxel@mtl.mit.edu
H. L. Tuller	Micromachining. Sensor (gas, thermal, pressure) and actuator development. Photonic switching. Electrically-active interfaces. Electroceramics.	13-3126 253-6890 tuller@mit.edu

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Research Interests of Faculty and Principal Research Scientist

	Research Areas	Office Telephone Net Address
J. Voldman	Biological applications of microsystem technology. Engineering and use of microsystems for analysis and engineering of single cells. Physical and electrical cell manipulation. Design, modeling, microfabrication, and testing of microfluidic biological devices employing unconventional materials and fabrication processes. Electromechanics at the microscale.	36-824 617-253-2094 voldman@mit.edu
I. A. Waitz	Micro gas turbine engines, micro-combustion systems, MEMS igniters and temperature sensors, propulsion, fluid mechanics, thermodynamics, reacting flows, and aeroacoustics.	31-207 253-0218 iaw@mit.edu

Research Themes

The mission statement of the MTL is that:

- MTL is an Interdepartmental Laboratory that encompasses research and education with an intellectual core of :
  - Semiconductor Process and Device Technology
  - Integrated Circuits and Systems Design
- MTL fosters new initiatives in Microsystems at the Institute
- MTL provides Microsystems infrastructure to the Institute

As a lab we are organized around two defining features. The first is as an infrastructure provider for Micro- and Nano- system research. This infrastructure includes support of micro/nano fabrication, and Microsystems design. The second defining feature is our community of micro and nano researchers.

The MTL infrastructure support includes three shared experimental facilities, which collectively comprise more than 6000 sq.ft. of cleanrooms. The Integrated Circuits Laboratory (ICL) is a class 10 cleanroom which supports principally silicon-compatible electronics and photonics. The lab contains 6"-wafer equipment rated at a 0.5 micron CMOS technology level. The Technology Research Laboratory (TRL) is a class 100 cleanroom which supports much of the MEMS and compound semiconductor fabrication. Protocols exist for transfer of materials between ICL and TRL, which enables a range of research which integrates these technologies. The Exploratory Materials Laboratory (EML) operates as a 'low-barrier' facility for thin film processing and experimentation. Highly flexible equipment is maintained in this facility to explore development of novel materials and processes which fall outside the capabilities of the ICL and TRL. Rounding out the shared cleanrooms are a set of packaging and testing capabilities that are shared by all the labs. In addition to the fabrication facilities, MTL supports the design environment for IC research. This primarily involves supporting the software infrastructure utilized in IC design.

The research community of MTL is described in the abstracts contained in this volume. Specifically, there are research efforts in; Integrated Circuits and Systems, Microelectromechanical Systems (MEMS), Electronic Devices, Quantum Effect Devices, Submicron and Nanometer Structures, Manufacturing/Modeling/Simulation, Fabrication Technologies, Materials, and Optoelectronics. In addition, the labs support a collection of educational activities, notable of these being the 'hands-on' fabrication laboratory and the WebLab effort.

The Integrated Circuits and Systems research efforts address a wide range of applications with several common themes; wireless, low-power, mixed-signal and analog design, and circuit-issues in advanced technologies (scaled CMOS, photonics, organics) and applications (intelligent transportation). The MEMS program has several major thrusts; power MEMS, optical MEMS, RF MEMS, bioMEMS, microfluidics and chemical systems, and micromechanical devices (valves, actuators, switches). In addition, there are programs on materials/process characterization and metrology. Electronic Devices research in MTL is focused on advanced devices and materials including Si/SiGe, SOI, heterostructures, power MOS, compound semiconductors (InP, GaAs), and magnetics. The Quantum Effect Devices area includes programs in superconducting devices, quantum computing technologies, quantum dots, and organic optoelectronics. A defining element of Submicron and Nanometer Structures research is the emphasis on patterning methods at the nanometer scale. In addition to these efforts on lithography, there are projects on self-assembling, 3D folded structures, nanotubes and wires, and various nanostructured photonic elements. The Manufacturing/Modeling/Simulation research is primarily focused on developing a modeling framework for characterizing

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Research Themes

and predicting the performance of various micro/nano fabrication processes. In Fabrication Technology, we see efforts on new processes such as through wafer vias, etching processes, lithography methods, and deposition processes. The Materials area includes projects on 3D Integrated Circuits, materials growth (Ge, GaN, InGaP), characterization (deformation, stress), magnetic technologies, and bonding. Optoelectronics programs include a substantial effort in silicon/silica waveguide technology and devices, photonic crystals, integration of photonic and electronic devices, and various light emitters (diodes, lasers).

Taken all together, these represent an extraordinarily broad set of activities. If one were to identify a unifying theme associated with these projects, it would be the system-level interest in the technology. The MTL represents a community which brings experimentalist skilled in materials and technology at the micro and nano-levels together with circuits/systems researchers to realize visions for new systems which are enabled by the integration of these disciplines.

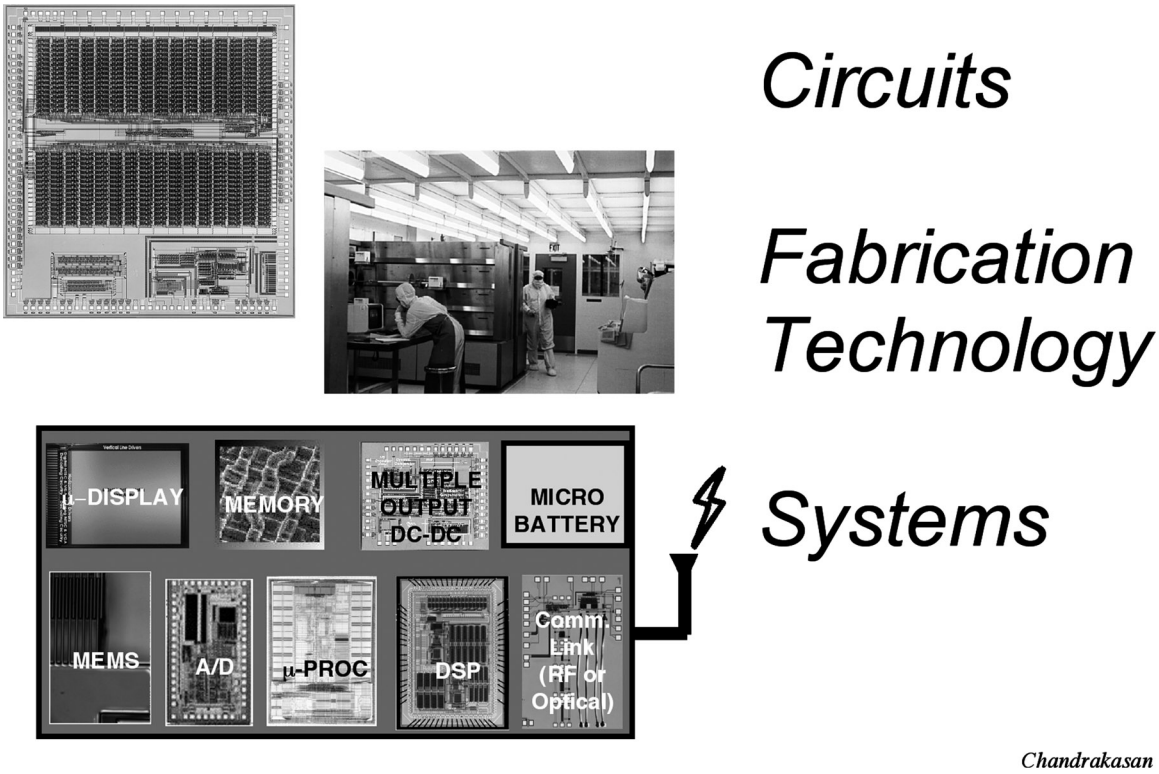


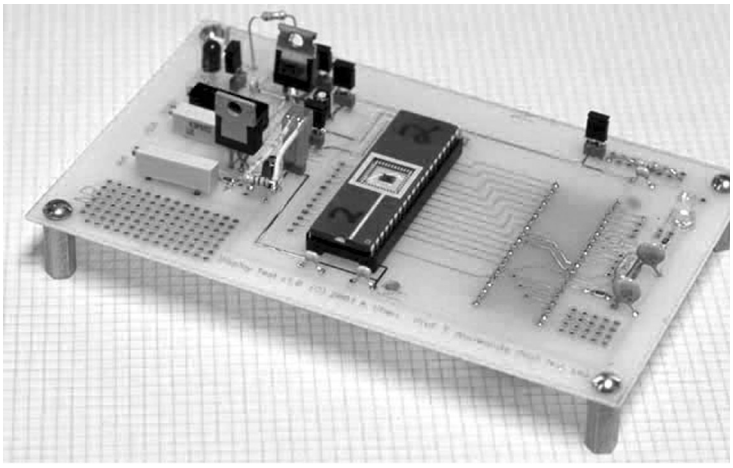
Figure: The MTL Research Themes

Opposite Page:

Circuit board including IC in 0.18 µm CMOS process.
Courtesy of A. Chen (A.I. Akinwande and H.-S. Lee)

Sponsor:
3M and MARCO Focused Research Center on Integrated Circuits and Systems (C2S2) (MARCO/DARPA)

Integrated Circuits and Systems



Integrated Circuits and Systems

- *μAMPS-2: A Fully-Integrated Energy-Agile Wireless Sensor Node*
- *Energy and Quality Scalable Wireless Communication*
- *Energy Efficient Multitarget-Multisensor Tracking on the uAMPS Platform*
- *Energy-Scalable 1024 Real-Valued FFT for Wireless Sensor Networks*
- *Novel Techniques Addressing Delay and Power Issues in Deep Sub-Micron Interconnect*
- *Design Methodology for Fine-Grained Leakage Control in MTCMOS*
- *PLL-Based Optical Clock Distribution*
- *Power-Aware Reconfigurable Hardware for Digital Baseband Processing*
- *Radio Design for a Power-Aware Microsensor Node*
- *Exploration of Sub-Threshold Circuit Design Topologies*
- *Ultra-Wideband Radio Antenna Design*
- *Ultra-Wideband Radio Transceivers*
- *Ultra-Wide Band (UWB) Short-Haul Data Communication*
- *Wireless Gigabit Local Area Network*
- *5.8 GHz Wideband Receiver for Wireless Gigabit LAN*
- *Analog Base-band Processor for Wireless Gigabit LAN*
- *Effect of Circuit Nonlinearity on System Performance Metrics, BER and Spectral Efficiency*
- *On-Chip Cross-Talk Analysis for an Array of Transceivers on a Single Chip*
- *Linear Power Amplifier Design for WiGLAN*
- *Smart Active-Matrix Display Drivers For Organic Light Emitting Devices*
- *A CMOS-Compatible Compact Display*
- *A Programmable, Wide Dynamic Range CMOS Imager with On-Chip Automatic Exposure Control*
- *Mixed-Signal Design in Deeply Scaled CMOS Technology*
- *A CMOS Bandgap Current and Voltage References*
- *Flicker Noise in Scaled CMOS Devices*
- *Device Level Optimization of Phase Noise in Integrated LC VCOs*
- *Radio Frequency Digital-to-Analog Converter*

continued

continued

Integrated Circuits and Systems

- ***Low Power RF Front-End for Wireless Microsensor Systems***
- ***Substrate Noise Coupling and Reduction Techniques in Mixed-Signal Systems***
- ***An Advanced Model Based Vision System for Intelligent Transportation Systems***
- ***Efficient Traffic Monitoring***
- ***Sensor Fusion for Automobile Applications***
- ***Superconducting Bandpass Delta-Sigma A/D Converter***
- ***Circuit and System Level Tools for Thermo-Aware Reliability Assessments of IC Designs***
- ***Intelligent Transportation Systems***
- ***The Low-Power Bionic Ear Project***
- ***The Visual Motion and Inertial Sensing Project***
- ***Spike-Based Hybrid Computers Project***

μAMPS-2: A Fully-Integrated Energy-Agile Wireless Sensor Node

Personnel

N. Ickes and C. Schurgers (A. P. Chandrakasan)

Sponsorship

DARPA

In recent years, the idea of wireless microsensor networks has garnered a great deal of attention and interest. A distributed wireless microsensor network consists of hundreds to several thousands of small sensor nodes scattered throughout an area of interest. Each node individually monitors the environment and collects data as directed by the user, but the network collaborates as a whole to deliver high-quality observations to a central base station. The large number of nodes in a microsensor network enables high-resolution, multi-dimensional observations and fault-tolerance that are superior to more traditional sensing systems. With these advantages in mind, microsensor networks hold great promise for applications such as warehouse inventory tracking, location-sensing, machine-mounted sensing, patient monitoring, and building climate control.

In the μAMPS-2 project, our aim is to build a highly integrated, yet versatile sensor system with an extreme focus on energy efficiency. This is achieved through custom ASIC design, while supporting the flexibility that is crucial in the dynamic operating environments that are typical for sensor networks. To this end, our hardware exhibits energy-agility: adapting the internal settings and circuit parameters on-the-fly to track the most energy optimal operating point under those varying conditions.

The μAMPS-2 architecture consists of a micropower DSP, surrounded by dedicated accelerator blocks for functions performed frequently by each sensor node. Accelerators for FFTs, FIR filtering, error correction coding/decoding, and data encryption are currently being designed. Each of these blocks is optimized for its specific task, while incorporating support for aggressive energy-agility. Furthermore, fine-grain shutdown modes are provided such that power is only consumed when strictly needed. Unused accelerators are dormant when not actively processing information. This architecture of highly optimized, on-demand hardware support for energy intensive tasks allows for ultra low-power data manipulation and lowers the processing burden on the DSP core.

This DSP core is at the heart of the μAMPS-2 node and employs a custom instruction set architecture optimized for microsensor applications. It has a 16-bit datapath, and will run at up to 10MHz, which is sufficient for typical microsensor applications. Clock speed can be dynamically reduced to tens of kilohertz or less for energy savings when less computational power is required. The on-chip data (~32kB) memory and instruction cache minimize the energy expended storing sensor measurements and fetching program instructions. Because many microsensor algorithms operate on blocks of sensor measurements, a sophisticated DMA (direct memory access) engine is employed to move data around the chip. The DMA engine can move blocks of measurements between accelerators and memory without intervention from the DSP.

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Energy and Quality Scalable Wireless Communication

Personnel

R. Min (A. P. Chandrakasan)

Sponsorship

DARPA, ARL Collaborative Technology Alliance, Hewlett-Packard under the MIT Alliance, and NDSEG Fellowship

Next-generation wireless devices will be characterized by shrinking size and increasing density, which together place an increasing emphasis on energy efficient operation. Moreover, emerging wireless applications such as microsensor networks will exhibit high operational diversity, reflected by time-varying environmental conditions, user requirements, and the nodes' own role in the network. Effective energy management strategies must therefore foster *energy scalability* through graceful energy vs. quality trade-offs in response to changing operational conditions.

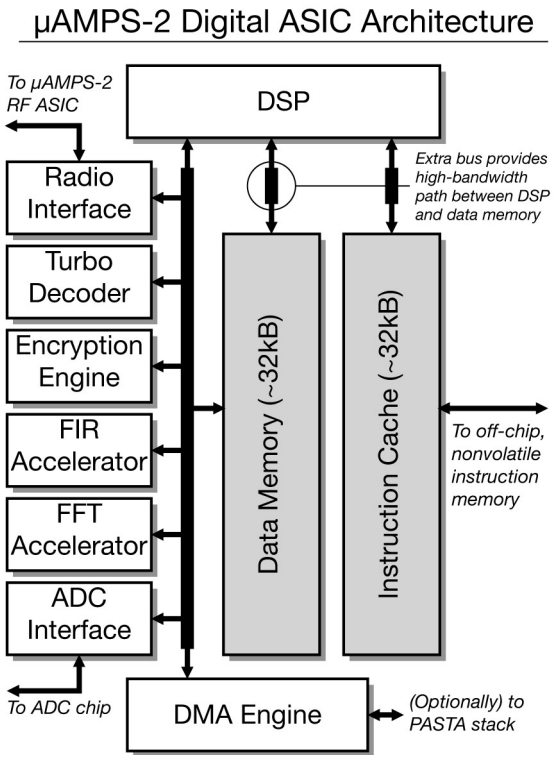

Fig. 1.

Graceful energy *vs.* quality scalability for wireless communication requires two prerequisites. First, the notion of communication "quality" must be defined. Hence, we define communication quality by four of its fundamental metrics: range, delay, reliability, and energy. We then introduce a basic API that allows an application to specify these metrics. Various combinations of delay, reliability, and energy can be chosen by direct specification. The communication range desired by an application can be expressed in a variety of ways, such as the distance to a specified node, a group of nodes, or the n nearest nodes. A second prerequisite is hardware that enables graceful trade-offs of energy and performance. The µAMPS-1 node provides flexible coding and output power settings.

Figure 2 then illustrates the energy required by the µAMPS-1 node for communication of variable reliability (bit error rate) and range. Note that, as the reliability or range requirements of communication increase, the energy required for communication increases monotonically. Each "step" in the graph corresponds to the minimum-energy selection of radiated power and coding policy that will meet the required quality constraints. The range and reliability of communication increase as more power is radiated from the transmitter or stronger error-correcting codes are used, resulting in longer transmit and receive times, and higher decoding energy.

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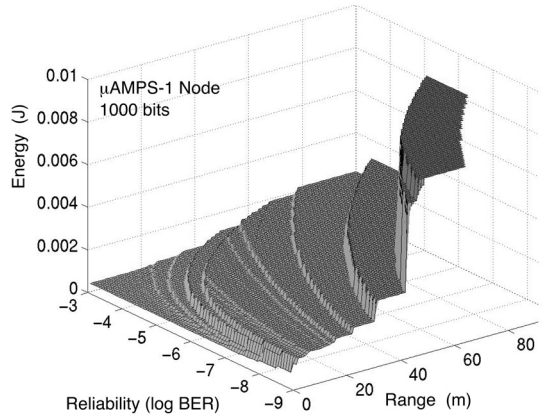

Fig 2: Energy-scalable communication on μAMPS-1 node.

Energy Efficient Multitarget-Multisensor Tracking on the uAMPS Platform

Personnel

K. Atkinson (A. P. Chandrakasan and C. Rohrs)

Sponsorship

ARL Collaborative Technology Alliance

For the uAMPS project, we have a network of acoustic sensing nodes producing a line-of-bearing to a sound source. The question then becomes how to integrate the data to produce the most accurate estimate of the target position. The line-of-bearing measurements are quite noisy in practice and simple triangulation would yield poor tracking performance. To achieve superior estimation accuracy we have implemented algorithms based on the Kalman filter, a fundamental algorithm of estimation theory.

The Kalman filter has two main advantages. First, it incorporates information regarding the statistical properties of both the target's motion and the measurements available, allowing for improved performance in the presence of noise. Second, it produces not only the estimate of the target's state, but also probabilistic information regarding the accuracy of the estimate (covariance matrix).

The covariance matrix and other probabilistic information computed by the Kalman filter serve a variety of purposes. For example, they can be used to validate measurements and reject those that are clearly spurious by computing the probability a particular measurement came from the target. (See Figure 3) Monitoring the covariance matrix can also indicate which sensors are providing useful information to localize the target, and allow for unneeded sensors to be shut down to save power.

Work is currently underway to extend the system to simultaneously track multiple targets. In this scenario the main challenge involves determining the measurement to target associations. The technique used is known as joint probabilistic data association, and computes the probability that each measurement validated for a target actually originated from that target. The state estimate is then updated with an appropriately weighted combination of all validated measurements.

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We currently have a real-time Kalman filter based tracking application running on the uAMPS nodes for a single target. (Figure 3 shows a screenshot.) Work in is progress to implement the multiple target tracking algorithms in addition to power-saving enhancements to shut down unnecessary sensors.

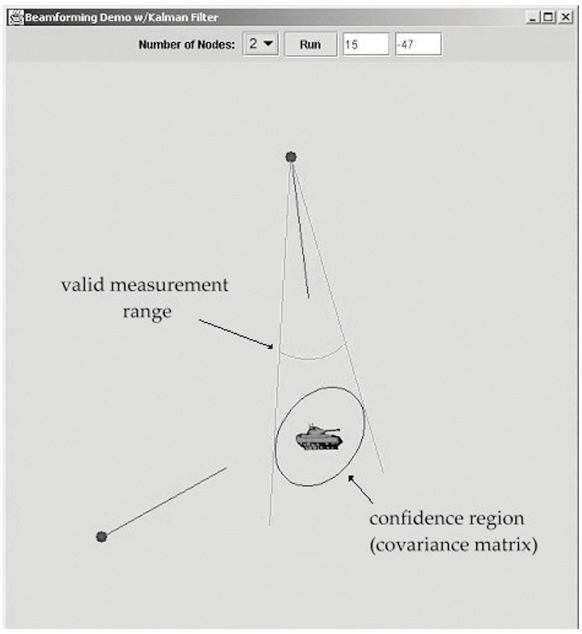

Fig. 3

Energy-Scalable 1024 Real-Valued FFT for Wireless Sensor Networks

Personnel

A. Wang (A.P. Chandrakasan)

Sponsorship

Intel Fellowship and DARPA

Energy efficient Digital Signal Processors (DSP's) is an important component of wireless sensor networks, where tens to thousands of battery-operated microsensors are deployed remotely and used to relay sensing data to the end-user. Given the constantly changing environments of sensor devices and the extreme constraints on battery lifetimes, system level energy-aware design considerations should be taken into account.

Energy-aware design is in contrast to low power design, which targets the worst case scenario and may not be globally optimal for systems with varying conditions. The energy-awareness of a system can be increased by adding additional hardware to cover functionality over many scenarios of interest and to tune the hardware such that over a range of scenarios, the system is energy-efficient. One algorithm that is widely used in sensor and wireless applications is the Fast Fourier Transform (FFT). In the area of sensor signal processing, the FFT is used in frequency domain beamforming, source tracking, harmonic line association and classification.

Energy-quality scalability for an system is needed if the environment of the device changes constantly. An energy-aware FFT will be able to adapt energy consumption as energy resources of the system diminish or as performance requirements change. Therefore, it is advantageous to design the FFT with energy scalability hooks such as variable memory size and variable bit precision, so that it can be used for a variety of scenarios. Our design focuses on a Real-Valued FFT (RVFFT) which can scale between 128-512-point FFT lengths and can operate at both 8 and 16-bit precision computation.

In this work two energy-aware architecture designs are developed. These architectures are evaluated in the context of a variable bit precision and variable

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FFT length RVFFT. The scalability of the RVFFT was implemented in a 0.18-micron process for energy-awareness measurements and hardware verification. Figure 4 shows a die photo of the scalable RVFFT implementation.

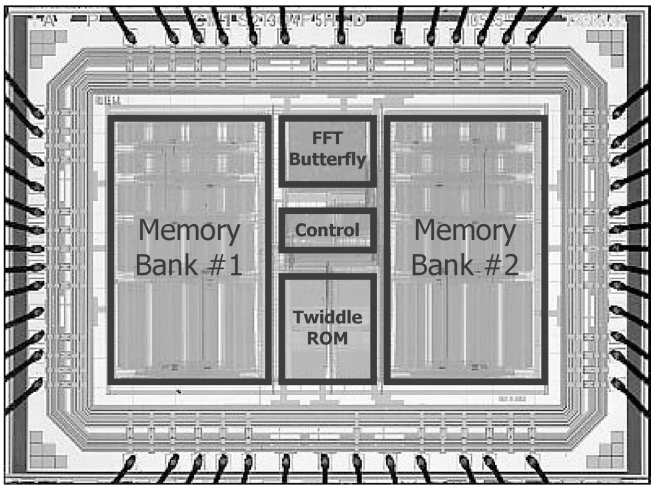

Fig. 4: Die photograph of the Energy-Scalable RVFFT.

Novel Techniques Addressing Delay and Power Issues in Deep Sub-Micron Interconnect

Personnel

T. Konstantakopoulos (A. P. Chandrakasan)

Sponsorship

MARCO Focused Research Center on Interconnect (MARCO/DARPA)

In deep-submicron technologies the primary component of delay is shifting from logic gates to the interconnect network. Buses can no longer be considered as a set of independent lines that don't interact. A more appropriate model would treat the bus as a distributed system where a transition on a line would affect adjacent lines as well. However, the transitions on a bus can be grouped into delay classes depending on the effective capacitance that the driver circuit needs to charge.

An effective approach to reduce delay in interconnect is by eliminating the transitions that are relatively time consuming. We are using coding schemes to accomplish that by increasing the number of lines in the bus, thus imposing some redundancy. In our implementation, which is shown in Figure 5, we are mapping a 4-line bus to a 6-line bus. A test chip to verify the proposed coding scheme has been fabricated and is being tested.

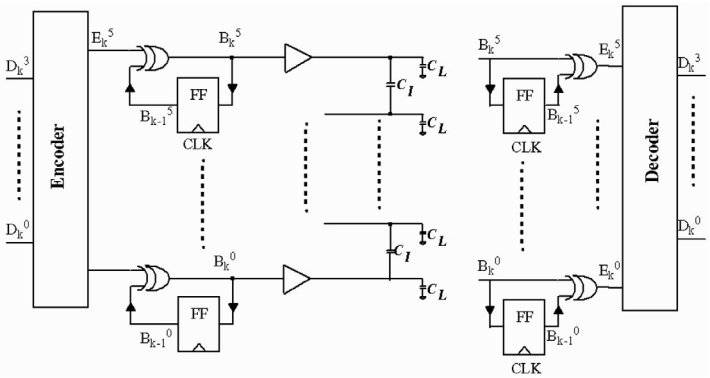

Fig. 5

Design Methodology for Fine-Grained Leakage Control in MTCMOS

Personnel
B. Calhoun (A. P. Chandrakasan)

Sponsorship
Texas Instruments and DARPA

Multi-threshold CMOS is a popular technique for reducing standby leakage power with low delay overhead. Most MTCMOS designs use large sleep devices to reduce standby leakage at the block level. The use of sleep devices at a local, gate level remains largely unexamined. One reason for choosing large sleep FETs is the design complexity associated with placing them locally. Segmenting the sleep transistor into many devices at the gate level creates a greater possibility for sneak leakage paths. Generally, sneak leakage paths are high leakage paths between power and ground that remain during sleep mode. Analysis of sneak leakage paths at the local level can provide insight that eliminates much of this complexity. Locally placed sleep devices offer several advantages over the large sleep FET approach, such as guaranteed circuit functionality at high speed, standard-cell MTCMOS design, and improved noise margins.

We developed a formal examination of sneak leakage paths and a design methodology that enables gate-level insertion of sleep devices for sequential and combinational circuits. A fabricated 0.13μm, dual VT testchip employs this methodology to implement a low-power FPGA architecture with gate-level sleep FETs and over 8X measured standby current reduction. The methodology also allows local sleep regions that reduce leakage in active CLBs by up to 2.2X (measured) for some CLB configurations.

An MTCMOS circuit uses a high VT sleep device between a low VT circuit and one rail, usually the ground rail. Whether the sleep device is one large device or many small ones, the basic structure of MTCMOS circuits suggests that sneak leakage paths must occur only where the sleep device(s) can be bypassed. Thus, the focal point for preventing sneak leakage paths is the interface between MTCMOS and CMOS circuits. The rules isolate cases where sneak leakage occurs at this interface. The testchip confirms that gate-level sleep devices can provide standby leakage savings. Placing the entire chip in sleep mode provides a measured reduction in leakage current by from 7.0X to 8.6X. We also propose fine-grained sleep regions and implement them on the testchip. The chip measurements match closely with simulation, and they show the benefit of the sleep region technique. The use of gate-level sleep devices allows inactive circuit regions to enter sleep at a fine grain. The other circuit components remain active and with unaffected performance. The total steady-state power (clock-gated) for an active CLB reduces by from 10% to 2.2X for different configurations. Figure 6 shows an annotated die photo of the chip.

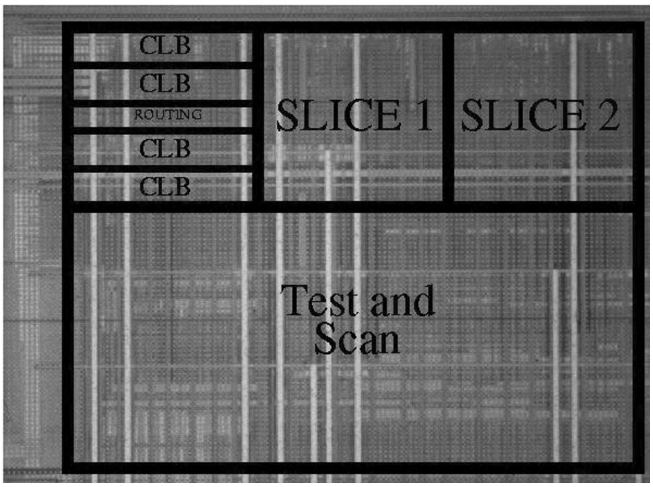

Fig. 6: Annotated Die Photo

PLL-Based Optical Clock Distribution

Personnel

A. Kern (A.P. Chandrakasan)

Sponsorship

MARCO Focused Research Center on Interconnect (MARCO/DARPA)

Because optical signals do not experience the time-variant propagation delays associated with the distribution of electrical signals, optical synchronization could potentially be used to generate extremely precise clocks. Many existing optical clock distribution systems, however, fail to fully utilize this potential because they are limited by the skew and jitter introduced in the transimpedance amplifier stages used for the optical to electrical signal conversion.

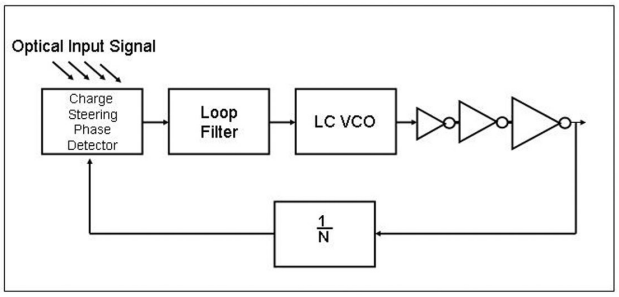

Fig. 7

Removing the explicit optical to electrical signal conversion step would result in a reduction of skew and jitter. This direct conversion step may be eliminated by generating the clock with an optically-locked PLL that contains a phase detector capable of directly comparing the phases of an optical and an electrical signal. (See Figure 7) The proposed phase detector uses the electrical feedback signal to steer the photocurrent generated by the optical signal.

The PLL is based on the traditional architecture and contains the phase detector, loop filter, VCO, and feedback divider. A LC VCO was chosen to minimize oscillator jitter and frequency range. Because a phase detector is used for comparison, the VCO range must be within a factor of two of the reference frequency or the loop could lock to a harmonic. Due to its superior jitter performance, a synchronous divider was used to generate the 1.6 GHz output frequency from an optical input frequency of 200 MHz.

A first-generation test chip will be fabricated in the TSMC 0.18 um process and tested. Future work will examine using an additional electrical feedback loop to aid frequency acquisition and investigate circuits for direct phase-frequency comparison of optical and electrical signals.

Power-Aware Reconfigurable Hardware for Digital Baseband Processing

Personnel
F. Honoré (A.P. Chandrakasan)

Sponsorship
MARCO Focused Research Center on Interconnect (MARCO/DARPA)

This project continues previous work on building energy-scalable solutions for wireless systems. A Field Programmable Gate Array (FPGA) architecture is the basis for exploring a fine-grain hardware approach to creating a platform for signal processing by introducing low-level power control. A novel Configurable Logic Block (CLB) with enhancements for distributed arithmetic computation and power control regions was validated through a testchip using a 0.13-um dual threshold voltage process.

The new CLB design yields much more efficient algorithm mapping over existing implementations by reducing logic block utilization by 50% or better. For more efficient power usage regions within the logic block have the ability to automatically power down when not in use. The results show that this fine-grain MTCMOS approach achieves significant power savings in the range of 1.2x to 2.7x by reducing active mode subthreshold leakage.

Interconnect overhead for FPGA's can be a significant fraction of the power budget for large designs. Programmable switch elements introduce large delays in long paths. Additionally, deep submicron buses have large parasitic interwire coupling capacitances that further increase delay of long wires. A new programmable switch architecture is being explored that will allow long paths to be pipelined to meet critical path timing or alternatively allow reduced voltage operation with minimal performance impact. Bus coding techniques are applied on groups of long routes to mitigate the impact of the interwire capacitance effect. Additionally, routing area overhead is reduced by more efficient placement of configuration storage elements and utilizing the available layers of metal.

By introducing these fine-grain hardware controls at several levels, this low power FPGA forms the basis for a platform that allows for effective in-system energy-delay tradeoffs for energy-constrained systems.

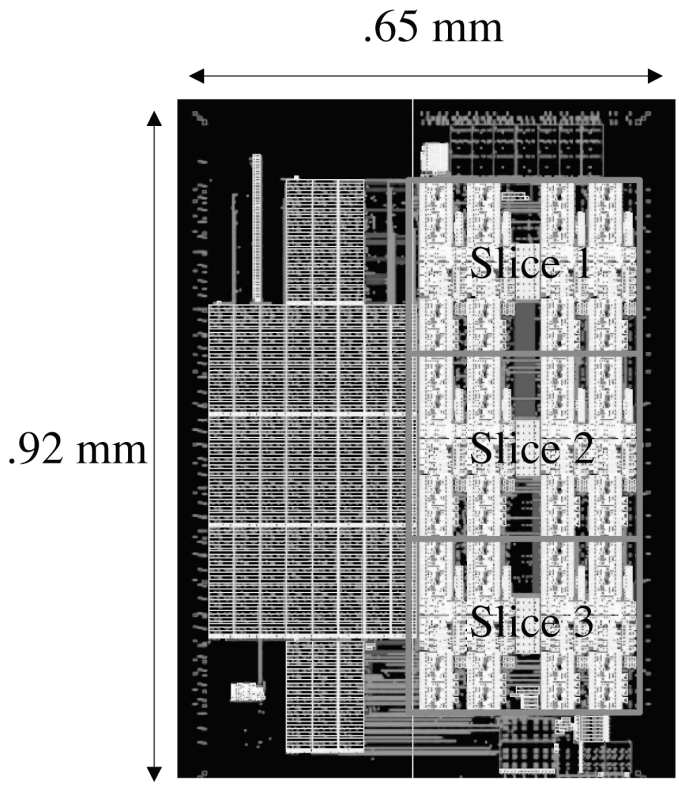

Fig. 8

Radio Design for a Power-Aware Microsensor Node

Personnel

D. Wentzloff (A. P. Chandrakasan)

Sponsorship

DARPA

The goal of the MIT μAMPS project is to develop a wireless network of small, low-power, general purpose sensor nodes that can collectively gather information about their surroundings and wirelessly relay it to a base station. The nodes are general purpose because they have a generic A/D interface that can connect to a variety of sensors, and the DSP and hardware accelerators can be selectively used or disabled depending on the complexity of the processing required by the application. The MIT μAMPS project is now in phase II: the development of a two-chip, power-aware node. One chip will include all of the digital hardware and sensor A/D converters. The second chip will include all of the RF hardware for the radio.

Since the first prototype radio for the μAMPS project was built, a need has arisen for long range wireless communication between nodes. To accommodate this, a new radio is being designed with the addition of a 1 Watt power amplifier that will improve the transmission distance by a factor of 10. Other improvements to the radio are lower idle and receive power consumption and the use of a radio chip with an integrated 8-bit microcontroller. The 8-bit microcontroller can be used as a protocol processor for the radio, and will greatly simplify the interface from the radio to the digital circuits.

Using this prototype radio as a benchmark, a chip will be fabricated with a complete, ultra low power radio having multiple knobs for varying its performance. This will allow the power consumption of the radio to be fine tuned based on the node's environment and proximity to other nodes. To accomplish this, RF components must be re-designed with the appropriate adjustments and feedback for regulating the performance. A test chip has been fabricated in collaboration with Nisha Checka that has seven Voltage-Controller Oscillators (VCO) operating at different frequencies, and digital circuits that intentionally inject noise into the substrate. By adjusting the power consumed by a VCO, the signal to noise ratio at the output can be controlled. This chip is currently in the testing phase. A picture of the die is shown in the figure. By adding functionality like this to a radio, the protocol processor will be able to vary parameters such as linearity and bandwidth in addition to transmit power. This has the potential of lowering the overall energy consumption per bit of the radio.

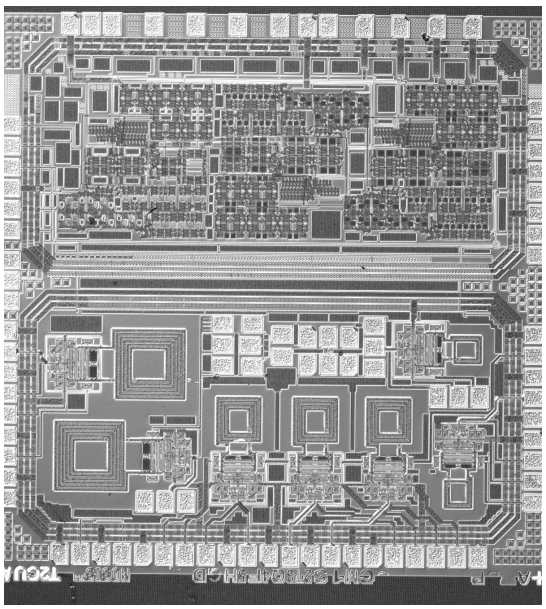

Fig. 9 Die photo of the VCO chip and digital circuits

Exploration of Sub-Threshold Circuit Design Topologies

Personnel
J. Cline (A. P. Chandrakasan)

Sponsorship
SRC Fellowship and DARPA

Sub-threshold logic design is a circuit technique that entails lowering the voltage supply below the threshold voltage of transistors to reduce the dynamic power dissipation. At such low voltage levels, sub-threshold currents are used to charge and discharge the logic.

My research aims to compare and contrast different logic design methodologies for the sub-threshold regime. The logic studied was evaluated in full-adder designs and implemented in a 16x16 bit Baugh-Wooley Multiplier.

An important observation obtained from the implementation above relies on the fact that sub-threshold current depends exponentially on the gate voltage. In strong inversion, this exponential relationship gives an 'on' current to 'off' current ratio of approximately a few thousand to one. In contrast, sub-threshold designs have voltages around a few hundred millivolts and thus, the ratio of the currents can be as small as 10:1. When implementing CMOS logic in the sub-threshold regime, designs must account for this small current ratio and the process variations must be tightly monitored. At the worst process corners, the already small ratio of currents can affect the speed and even the circuit functionality. Thus, the worst case process corners dictate the lowest functional voltages.

In conclusion, this research compared different logic families, such as transmission gate, static CMOS, and dynamic logic, implemented in the sub-threshold regime. The performance and energy tradeoffs were analyzed for an array of process variations and variable supply voltages, as low as 100mV.

Ultra-Wideband Radio Antenna Design

Personnel
J. Powell (A. P. Chandrakasan)

Sponsorship
Presidential Fellowship, DARPA and HP under the MIT Alliance

The recent allocation of the 3.1-10.6 GHz spectrum by the Federal Communications Commission for Ultra Wideband (UWB) radio applications has presented a myriad of exciting opportunities and challenges for design in the communications arena, including antenna design. Ultra Wideband Radio requires power spectral densities of –43.1dBm/MHz and bandwidths greater than 50% of the center frequency. Due to the power constraints, many UWB designs occupy the entire bandwidth. Successful transmission and reception of an Ultra Wideband pulse that occupies the 3.1-10.6 GHz spectrum require an antenna that has linear phase and VSWR ≤ 2 throughout the entire band. Linear phase ensures constant group delay which is imperative for transmitting and receiving a pulse with minimal distortion. VSWR ≤ 2 is required for proper impedance matching throughout the band, ensuring at least 90% total power radiation. This corresponds to a return loss of greater than 10 dB throughout the band. Compatibility with an integrated circuit also requires an unobtrusive, electrically small design.

One method for achieving broadband characteristics uses Babinet's Equivalence Principle of duality and complementarity. The principle states that the product of the input impedances of two planar complementary antennas is such that $Z_1 Z_2 = \eta^2/4$. This is illustrated in the spiral slot antenna design in Figure 10, which incorporates two complementary spirals in one antenna element. This design shows that the metal spiral is the exact complement of the free-space spiral, which then requires that $Z_1 = Z_2 = \eta/2$. This impedance can be adjusted based on the choice of dielectric constant value.

Preliminary simulations of this design have shown promising results with regard to VSWR bandwidth and linear phase, at a size of 4.5 cm x 4.5 cm. Multiple implementations will be designed on various PC boards to determine an optimum dielectric constant value and dielectric thickness based on bandwidth and beamwidth

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measurements. Antenna radiation patterns, gains and efficiencies will be measured in an anechoic chamber. Pulse transmission and reception will be tested on a UWB discrete system to qualitatively determine the effects of pulse transmission and reception in the time domain. Lastly, this antenna will be tested with a UWB IC transceiver.

In summary, this research involves the design, implementation and characterization of an Ultra Wideband antenna for integration with a UWB IC transceiver.

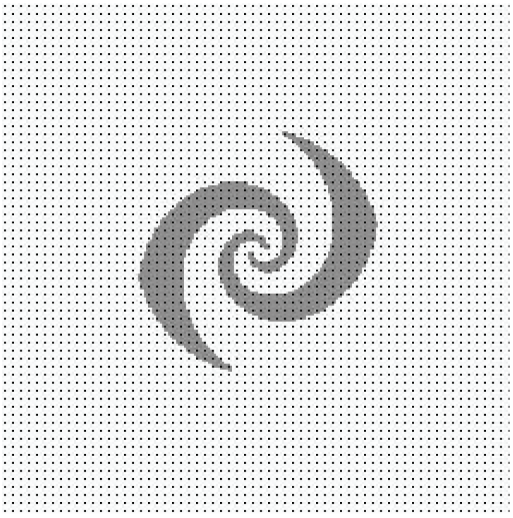


Fig. 10

Ultra-Wideband Radio Transceivers

Personnel

R. Blazquez, F. S. Lee, P. Newaskar, J. Powell, D. D. Wentzloff (A. P. Chandrakasan)

Sponsorship

HP-MIT Alliance, Presidential Fellowship, DARPA, Air Force Research Laboratory

The recent approval of Ultra-Wideband (UWB) wireless technology by the Federal Communications Commission has presented a myriad of exciting opportunities for circuit design, system design and antenna design. Depending on the application, UWB signals utilize bandwidths from DC to 960 MHz or 3.1 GHz to 10.6 GHz. Contrary to traditional narrowband, single-tone radio signals, a UWB signal is typically composed of a pulse train of sub-nanosecond pulses modulated either in polarity or position as shown in Figure 11. The narrowness of the pulse in the time domain corresponds to the wideness of the band in the frequency domain. Since the total power is spread over such a wide swath of frequencies, its power spectral density is extremely low. This minimizes the interference caused to existing services that already use the same spectrum. On account of the large bandwidth used, UWB links are capable of transmitting data over tens and hundreds of megabits per second.

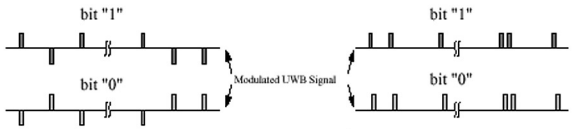


Fig. 11 : Transmitting Information in a UWB System

To date, we have implemented and tested a base-band (DC to 960MHz) front end UWB chip shown in Figure 12 (our future research will target communication in the 3.1-10.6 GHz band). Currently we are designing a full base-band transceiver using BPSK modulation, with a symbol rate of 20 megabits per second.

Our research approach for UWB radio transceivers is divided into these five sections: transmitter, antenna, analog front-end receiver, analog-to-digital conversion/ mixed-signal processing, and digital backend.

continued

continued

TRANSMITTER

The transmitter for our first architecture consists of a three to one switch. Every 20 nanoseconds, the transmitter output switchs from the idle state of 0.9 volts, to either the power rail, 1.8 volts or ground rail, 0 volts, to provide positive or negative pulses. The output from the transmitter is ac-coupled to the transmit antenna. The power supply is scaled to scale the transmit power output.

A block diagram of a general UWB transceiver is shown in Figure 13.

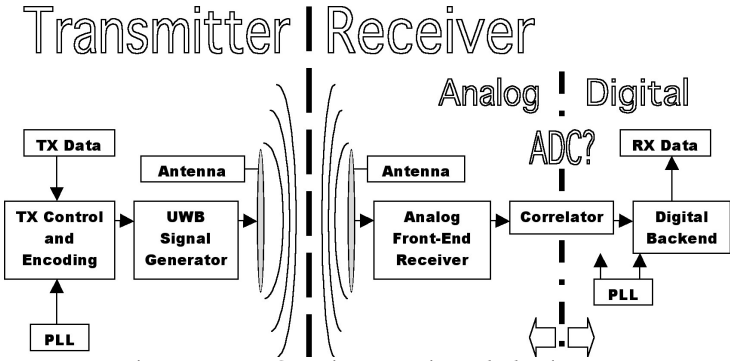


Fig. 13 : UWB Generic Transceiver Block Diagram

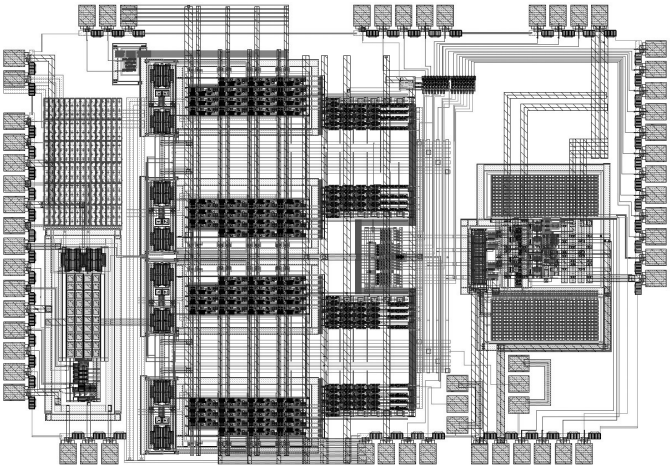


Fig. 12 : Layout of Analog front-end for base-band UWB

ANTENNA

UWB requires power spectral densities of –43.1dBm/MHz and bandwidths greater than 50% of the center frequency. Due to the power constraints, many UWB designs occupy the entire bandwidth. Successful transmission and reception of an Ultra Wideband pulse that occupies the entire FCC allocated spectrum require an antenna that has linear phase and VSWR ≤ 2 throughout the entire band. Linear phase ensures constant group delay, which is imperative for transmitting and receiving a pulse with minimal distortion. VSWR ≤ 2 is required for proper impedance matching throughout the band, ensuring at least 90% total power radiation. This corresponds to a return loss of greater than 10 dB throughout the band. Compatibility with an integrated circuit also requires an unobtrusive, electrically small design. Preliminary simulations of a spiral slot antenna have shown promising results with regard to VSWR bandwidth and linear phase, at a mere size of 4.5 cm x 4.5 cm. Multiple implementations will be designed on various PC boards to determine an optimum dielectric constant value and dielectric thickness based on bandwidth and beam-width measurements.

ANALOG FRONT-END RECEIVER

An analog front-end has been designed for the base-band, zero to 960MHz UWB band. The LNA of the front end was chosen to be single-ended, and utilizes known noise-canceling techniques to achieve a broadband low noise figure. The noise figure of the entire front-end is under 3.8dB between the frequencies of 100MHz to 1GHz. Between 10MHz and 100MHz, the noise figure is degraded by 1/f noise, and is as high as 8dB. The gain of the entire front end is 60dB, differentially. A single-ended to differential circuit converts the single-ended

continued

LNA signal to a differential signal, and feeds into a cascade of differential stages to obtain the overall 60dB gain.

ANALOG-TO-DIGITAL CONVERSION
Digitizing a large-bandwidth RF signal near the antenna introduces its own set of challenges and has traditionally been considered infeasible. A high-speed, high-resolution analog-digital converter (ADC) is difficult to design, and is extremely power-hungry. However, due to the unique spectral characteristics of UWB signals and their noise environment, it can be shown that reliable detection of a UWB signal is achievable with very few bits of resolution in the ADC. A theoretical analysis of the problem has been carried out that validates the above hypothesis. It has been determined that 4 bits of resolution are sufficient for reliable detection of a UWB signal. Subsequently, design issues for a high-speed, low-resolution ADC in a fine line-width process have been explored, based on the design and implementation of a 4-bit, 4 giga-samples time-interleaved FLASH converter in 0.18mm CMOS.

DIGITAL BACKEND RECEIVER
For the first implementation of a base-band UWB receiver, a mostly digital implementation was chosen. Detection and all necessary signal processing is performed in the digital domain. As the ADC is providing 4 giga-samples per second, each of them with 4 bits, this is the total data rate that it is necessary to process in the digital back end.

The wireless channel will imply several echoes plus the usual attenuation and interferences that degrade the reception. The premise of the design is to provide fair protection against these problems.

An important part of the receiver, at least during the beginning of the communication is the synchronization. Apart from being necessary for the detection of the signals, it allows to drastically reduce the power consumption. In order to do this an architecture based in parallel correlators are proposed and implemented.

Ultra-Wide Band (UWB) Short-Haul Data Communication

Personnel

A. Chow (A.I. Akinwande and H.-S. Lee)

Sponsorship

MARCO Focused Research Center on Circuits and Systems (C2S2) (MARCO/DARPA)

High-level computation can be integrated on-chip to perform image processing, or data compression/decompression, or intelligent power management. High-resolution displays require large input data bandwidth; for example, computer monitors typically require over 2GHz bandwidth and interface circuits dissipate high power. As an example, The Silicon Image Sil 161B digital video interface receiver dissipates 800 mW. Interface circuits using compression and/or circuit techniques such as low-swing signaling can reduce the interface power dramatically, lowering the overall system power.

We are investigating a RF wireless link between the display and the host. For high resolution displays, even with on-chip data compression, the I/O data rate will still be very high. For this reason, the traditional narrow-band wireless link is not a suitable technology. We propose ultra-wideband data communication technology for host-to-display data communication. This technology can potentially be extended to chip-to-chip and back plane data communication as well. The ultra-wideband communication, which has been in limited use for medium-to-long range (~mile), low-data rate communication, employs a train of impulses rather than a single frequency RF carrier. The impulse train has a very wide frequency spectrum, typically DC- GHz range. Since the energy is spread in such a wide frequency range, there is negligible interference with traditional narrowband RF systems. Unlike narrowband transceivers, highly frequency selective circuits are unnecessary to facilitate the integration of the entire transceiver. Also, the effect of the multipath can be mitigated, and even exploited by measuring the arrival time and the phase of the multipath signals. For this reason, the untra-wideband technology is more suitable for short-range, fixed environment communication than the application that has been in use. The host-to-display, chip-to-chip, and backplane communication can benefit from the ultra-wideband communication because they are typically short-range, fixed environment communication. The short-range nature of the host-to-display, chip-to-chip, and backplane communication could provide a reasonable signal-to-noise ratio, which combined with ultra-wideband, would provide potentially very high data rate required in such data communication. Also, the host-to-display wireless link has an added possibility of broadcasting to multiple displays.

Our focus is an UWB receiver in which most signal processing is performed in the digital domain. This requires an A/D converter with extremely high sampling rate (> 10 GHz) and moderate (6 bit) resolution. There are several options to achieve such high sampling rates, one of which is time-interleaved analog to digital converters. The speed increase is achieved by placing several converters in parallel. This method requires that the individual converters, which make up the parallel combination, be matched. Mismatches in non-idealities, such as gain error, timing error, and voltage offset, greatly degrade the performance of such systems. Calibration is often used to reduce these mismatches.

This research will focus on using digital signal processing techniques to perform background calibration on the individual converters. Many converters use several input references (V_{max}, V_{gnd}, and a ramp function) to measure the gain error, offset error, and timing error. We are investigating an alternative calibration waveform to measure all of these errors that can be derived in one pass. For example, a single frequency sine wave calibration tone when digitized by individual channels and Fourier transformed will produce all necessary measurements. These non-idealities can be directly taken from the amplitude, offset, and phase of the digitized sin wave. Furthermore, by using spread spectrum modulation techniques, the calibration can be performed in the background.

Wireless Gigabit Local Area Network

Personnel

A. Chandrakasan, H.-S. Lee, and C.G. Sodini

Sponsorship

Center for Integrated Circuits and Systems (CICS)

The exploding number of electronic devices or "appliances" requiring high bandwidth communication will continue to drive the need for higher speed (Gigabit-per-second, Gb/s) networking. We assume that the Next Generation Internet (NGI) will carry high-speed data to and from the home or office. However, a Local Area Network (LAN) within these structures is necessary to continue high-speed data transmission to and from end-use devices, such as cameras, displays, printers, high resolution video, mobile communicators, and novel devices. The enabling technology for this rich set of applications is a *wireless Gb/s LAN*, (WiGLAN), connected to the NGI.

The WiGLAN offers several research challenges. First, there is a wide range of data rates, quality of service, and need for real time transmission to and from the appliances. For example, voice transmission over the network will not require high data rates, but may require low power dissipation for portability. Interactive video transmission requires real time transmission and very high data rates especially as high resolution video and 3D graphics become available. System resources will need to be adaptive in order to support this wide range of appliances. Second, since many of the appliances will require portability, low power design techniques at the circuit, chip architecture, and overall system level will be required. Third, this research requires synergy between a variety of disciplines including, communication system design at the physical layer, low power circuit and system design, digital signal processing algorithm and IC design, mixed signal IC design, and RFIC design. It also lends itself to a number of demonstration projects using some of the technology which results from this research. Besides the educational component of the PhD researchers directly involved, this program will generate a number of IC's and algorithms which can be demonstrated by Masters student design projects.

A block diagram of the Wireless Gigabit Local Area Network, WiGLAN, is shown in Figure 14. We envision a network server being the gateway between the NGI and the local area network. Each appliance is attached to the network through a WiGLAN adapter which is capable of providing a wireless connection to the network. This adapter should be physically small, implying a high degree of integration of the electronic functions required to interface digital data from the appliance to and from the network. The quality of service, QoS, which is a function of data rate and bit error rate, should be scaleable with power dissipation to permit battery operation of many appliances.

The network requirements of high bandwidth efficiency and real time transfer led to our choice of a multi-carrier modulation, such as Orthogonal Frequency Division Multiplexing, (OFDM) using M-Quadrature Amplitude Modulation, (MQAM) signal constellations. We plan to digitize the entire signal bandwidth (150 MHz) available at the 5.8 GHz ISM band and adapt the bit rate (change M) within sub-bands according to the available Signal-to-Noise Ratio (SNR) and interference in the sub-band. A programmable digital signal processor will perform this adaptive modulation.

The adaptive bit rate processor located in the network server will estimate the channel capacity by measuring the SNR and interference within sub-bands across the entire 150 MHz signal band. The channel estimation algorithm is a subject of this research. Depending on the SNR and interference, data modulation will range from simple Phase Shift Keying (PSK) up to 256 level QAM with intermediate levels of QAM, (i.e. 4-QAM, 16-QAM, etc.) allowing for transmission of approximately 1b/Hz for PSK up to 8b/Hz for 256-QAM.

In order to provide the capacity enhancements required to support the target data rates, the system to be developed will make extensive use of multiple-element

antenna arrays for both transmission and reception. A key component of the proposed research will therefore be the development of computationally and power efficient space-time coding and space-time processing algorithms that exploit the substantial diversity benefit inherent in the use of such antenna arrays. At the implementation level, multiple-element antenna arrays require a separate receive and transmit channel for each antenna element. To efficiently meet this requirement, we propose to build a system of parallel radios divided into three distinct Integrated circuits, namely RF, Mixed signal, and DSP.

The WiGLAN network adapter consists of three functions: digital signal processing for multi-carrier adaptive bit rate QAM, a baseband analog processor performing data conversion and filtering, and an RF transceiver function which interfaces the modulated baseband data to a 5.8 GHz carrier. We will design and characterize integrated circuits to perform these functions.

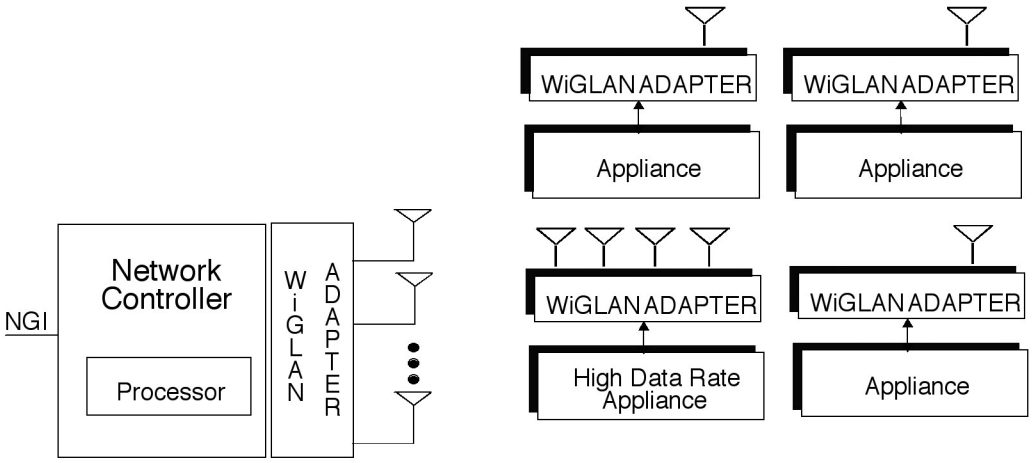


Fig. 14: Wireless Gigabit Local Area Network

5.8 GHz Wideband Receiver for Wireless Gigabit LAN

Personnel
L. Khuon (C. G. Sodini)

Sponsorship
Center for Integrated Circuits and Systems (CICS) and SRC

To take advantage of space-time diversity algorithms, multiple receiver front ends are needed on a single chip. Direct conversion does not require an image reject filter and simplifies the Radio Frequency (RF) filtering requirements. The nature of multiple receivers on chip, however, implies that the homodyne's local oscillator radiation would significantly interfere with nearby receivers since its frequency is in-band to the desired RF signal. In addition, a direct conversion receiver performs In-phase and Quadrature (I/Q) demodulation in the analog domain. This results in an I/Q phase imbalance, directly impacting the bit-error-rate performance. With a heterodyne architecture, the received signal could be digitized at a low IF and the functions of I/Q demodulation along with channel selection could be performed in the digital domain.

The receiver for the WiGLAN performs amplification, filtering, and downconversion of the 150 MHz signal centered at 5.8 GHz. The receiver downconverts the Radio Frequency (RF) signal to a low Intermediate Frequency (IF) that is fed to the analog baseband processor where it is equalized and digitized. The design approach for the receiver is based upon block level analyses that consider the gain, noise, and linearity tradeoffs necessary for the WiGLAN's adaptive modulation scheme.

The focus of this research is the design of on-chip filters within the framework of the Wireless Gigabit LAN (WiGLAN) receiver design. To reduce the effect of image frequencies for the heterodyne receiver, dual conversion architecture is selected to allow for optimized frequency planning. As such, filters are needed for the band selection and image rejection at the RF, band selection at the first IF, and anti-aliasing at the low IF. The primary challenges are to obtain the necessary band filtering and image rejection with an integrated approach without severely degrading the system's noise and linearity performances.

An initial integrated image reject filter was fabricated on IBM BiCMOS 7HP process technology (See Figure 15). The filter incorporates an on-chip inductor that has its quality factor enhanced through the use of a negative resistance circuit. The filter's center frequency is tunable externally with a DC voltage. In addition, by controlling the DC current of the negative resistance circuit, the rejection response is also adjustable. This simple notch filter circuit only performs a rejection at the image frequency. To perform rejection of a band of frequencies, higher order filters are necessary, and this initial circuit may serve as the building blocks for more complex responses for both the image band rejection and the signal band selection at the RF and IF stages. Besides the impact on the receiver's noise and linearity performances, the design of integrated filters must also consider issues of stability and possible automatic frequency response adjustments to account for device tolerances.

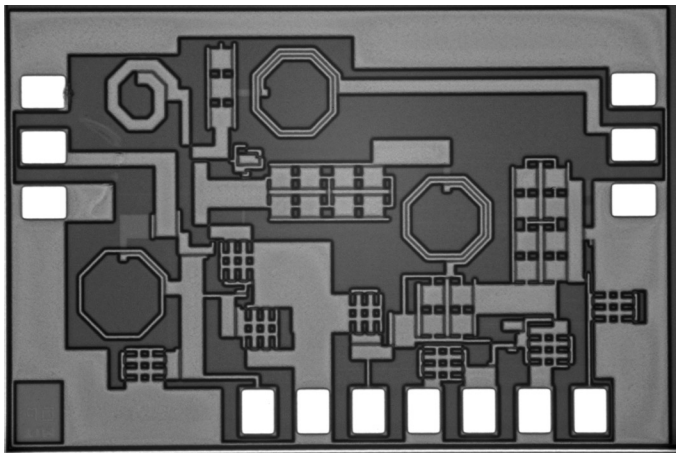


Fig. 15: Die photo of an LNA with notch filter for image rejection on IBM BiCMOS 7HP process.

Analog Base-band Processor for Wireless Gigabit LAN

Personnel
M. Spaeth (H.-S. Lee)

Sponsorship
SRC and Center for Integrated Circuits and Systems (CICS)

The base-band analog processor performs necessary signal processing on the 150 MHz base-band signal in the Transmit (Tx) and Receive (Rx) signal paths of a wide-band wireless local area network. There are tremendous technical challenges in the development of this base-band analog processor due to the high data rates and complex modulation schemes employed in a wireless network. The analog circuits in both the transmit and receive sections of the processor must handle 150MHz of signal bandwidth with signal-to-noise ratio in excess of 75dB (12 bits). In the receive section, these circuits include a low-noise wide-band anmplifier, a programmable gain-amplifier, an anti-alias filter, a channel equalization filter (if required), and finally an A/D converter.

This work focuses on the implementation of the extremely high speed, high resolution, and wide-bandwidth A/D converter in the Rx section of the base-band analog processor. In order to digitize the 150 MHz-wide signal band, the A/D converter must have an effective sampling rate above the Nyquist frequency of 300 MHz . To ease the anti-alias and digital filtering requirements, a sampling frequency above twice Nyquist will be used. The preliminary estimate of the A/D converter resolution needed to handle the wide dynamic range of the received signal is 12 bits. Additionally, any harmonic and intermodulation distortion in the signal path produces spurious signals in other sub-bands, so the A/D converter must exhibit very high spurious-free dynamic range (SFDR) in addition to wide bandwidth. At present, such high performance is beyond the capability of monolithic silicon integrated circuits.

To achieve high performance operation, some degree of parallelism is often employed. In a parallel time-interleaved converter, any mismatch in the gain, offset, or timing of the constituent channels results in undesirable harmonics in the output spectrum. Therefore, the time interleaving schemes commonly used today employ a small degree of parallelism, so that the harmonics lie either out of the signal band of interest or below the quantization noise floor. Our approach is to use large-scale parallelism (128 active channels) in a time-interleaved pipeline A/D converter. Back-end digital calibration is applied to account for static gain, offset, and timing mismatch errors between channels, so that the resulting calibrated output has sufficiently low spurious harmonics.

Measurement and calibration techniques for gain and offset errors are performed using standard calibration techniques. By digitizing a fast ramp using one converter as a fixed timing reference for the remaining converters, the relative timing skew between channels can be discerned. The calculated timing offsets are then used to re-time the output data stream using polynomial interpolation in the DSP in the back-end. Thus, all of the calibration is performed using simple algebraic operations with minimal latency. To allow all of the calibration operations to be performed in the background, a small fraction of the available channels are systematically pulled out for calibration, while a novel token-passing control scheme selects which of the 'active' converters will sample the incoming signal.

Figure 16 shows a top-level block diagram of the proposed A/D converter. 129 identical pipeline A/D channels are organized into 16 banks of 8 converters, with one additional converter used only as a skew timing reference. In this scheme 2 banks are pulled out at a time for calibration, so the remaining 112 converters operate at about 5.5 MHz to achieve the desired 600MHz aggregate sampling rate. 14 bit pipelines are used to generate 12 bit digitally error-corrected outputs. The converter bank that is actively digitizing the input signal receives the output of the front-end anti-aliasing filter. The converter banks that are under calibration may digitize DC values for gain

continued

and offset measurements or the fast ramp for timing skew measurements. The converter has two sets out outputs so that digitized signal samples and calibration data may be output simultaneously. The back-end DSP averages the calibration data, and generates the algebraic coefficients needed to correct the gain, offset, and timing mismatch errors.

While the infrastructure generate calibration data is on-chip, the sample output from the IC is raw and uncalibrated, with the calibration occurring offchip. This split architecture allows for other novel schemes to be employed, taking advantage of the massive amount of data being output to resolve higher resolution, but lower data rate samples. In addition to straight forward calibration, non-uniform sampling methodologies and oversampling techniques are also being explored, so that the core IC design can be more intelligently applied to a broader range of applications.

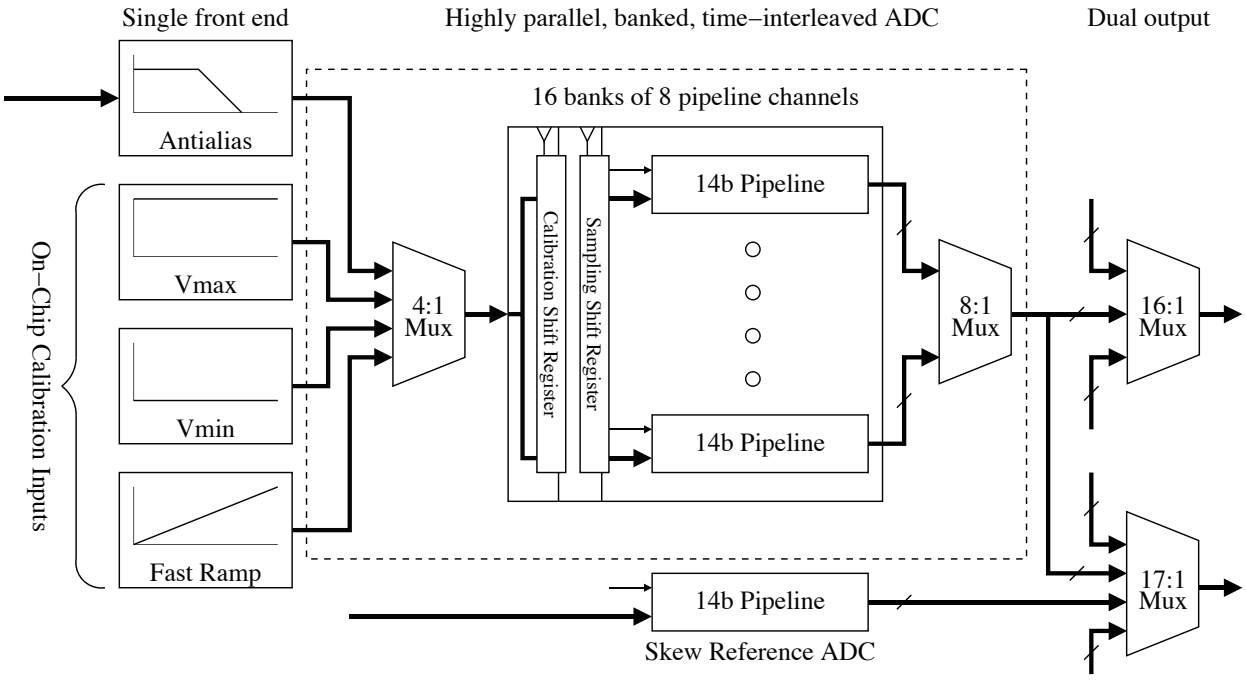


Fig. 16

Effect of Circuit Nonlinearity on System Performance Metrics, BER and Spectral Efficiency

Personnel

F. Edalat (C.G. Sodini)

Sponsorship

Center for Integrated Circuits and Systems (CICS) and The National Defense Science and Engineering Graduate Fellowship

As the demand for RF spectrum increases, high-speed data transmission over radio channel is likely to benefit from high bandwidth efficiency obtained from transmission of multi-carrier signals (OFDM or TDM) with Multilevel Quadrature Amplitude Modulation (M-QAM). In addition, from the circuit point of view, power amplifiers are more desirable to operate at high power levels than at low power levels for improved power efficiency. Higher efficiency means that a larger percentage of the dc (e.g. battery) power is delivered to the load. However, at high power levels, power amplifiers become nonlinear. Since the envelope of a QAM-modulated signal is not constant, it requires a high level of linearity of the transceiver components to achieve an acceptable performance.

Traditionally, to operate in the linear region, a large back off from the 1-dB compression point of the power amplifiers was suitable. This leads to low power efficiency and high power consumption, which cannot be tolerated in portable wireless systems. A higher power efficiency of a power amplifier can be obtained at the expense of more nonlinear distortion. In other words, as the input power enters the nonlinear region of power amplifier, power efficiency increases while the performance degrades. In addition, nonlinearity introduces a degradation of spectral efficiency. As a consequence, for a given nonlinear power amplifier, we would like to find the maximum input power - in the nonlinear region of the amplifier - that achieves BER below the maximum target BER and spectral efficiency above the minimum allowable spectral efficiency. Such information is extremely valuable to circuit and system designers, facilitating the collaboration between the two, and hence leading to more efficient practical design solutions in a shorter amount of time. However, obtaining such information requires knowledge of how circuit nonlinearity parameters affect system performance metrics, BER and spectral efficiency, which is the focus of this research.

To investigate the effect of circuit nonlinearity on the system performance, a communication system with a nonlinear power amplifier model is simulated. The transmitter of the communication system consists of an M-QAM random source, creating a sequence of symbols chosen randomly from the signal constellation. The symbol sequence is converted to a continuous-time waveform by a square-root-raised-cosine filter, and then added to an Additional White Gaussian Noise (AWGN) characterizing the circuit noise introduced by other transmitter components, such as the VCO and mixer. The resulting signal is the input to the nonlinear power amplifier model, and its output goes to the AWGN channel. At the receiver, the received signal is passed through another square-root-raised-cosine filter, which together with the filter at the transmitter constitutes a Nyquist Filter that is required to achieve zero inter-symbol interference. The filter output is sampled at the optimum sampling point, and subsequently detected by a Minimum-Distance optimum detector. The detected symbols are then compared with the transmitted symbols, and the number of symbols in error is calculated. Throughout the simulation, the signal is maintained at the baseband, and the effect of up-converting it to passband for the purpose of our study is taken into account by characterizing only the nonlinearity effect of power amplifier in the band of interest around the carrier frequency. The result of such simulation is directly affected by the accuracy of the model used to characterize the nonlinearity of the power amplifier. Our model is obtained by examining the transfer characteristic data of an experimental class-A power amplifier fabricated in IBM SiGe 7AP BiCMOS process. Once the best nonlinearity model is found, insightful results can be produced by this simulation, including the performance degradation level, BER, as a function of input back-off from saturation, or the optimum modulation level to use in order to operate at a required power level with a maximum tolerable BER.

On-Chip Cross-Talk Analysis for an Array of Transceivers on a Single Chip

Personnel

J. Liang (C.G. Sodini)

Sponsorship

MARCO Focused Research Center on Circuits, Systems, and Software (C2S2) (MARCO/DARPA)
and Center for Integrated Circuits and Suystems (CICS)

The Wireless Gigabit Local Area Network (WiGLAN) project is using multiple antennas to increase capacity through Space-Time Coding (STC). Such a system can benefit from integrating multiple RF front ends on a single chip. Each front-end analog circuit consists of a mixer, filtering, and power amplifier at the transmitter side and an LNA, mixer and filtering at the receiver side. In addition, local oscillators at specific frequencies must be synthesized and applied to the mixers. Along the chain of each front end, there are multiple nodes that signal cross-talk can occur.

Such cross-talk between these parallel radios can severely degrade the system performance, imposing major challenges for integration. How much overall-system-performance degradation does the cross-talk cause? How much can careful circuit-design contribute to cross-talk suppression? How to determine the adequate level for cross-talk suppression? This study will attempt to answer these questions.

The focus of the research is to quantify the effect of cross-talk upon the overall system performance. In particular, a study of the specific nodes which are vulnerable to cross-talk along the radio front ends and the required isolation level for various modulation schemes will be carried out. Two types of signal cross-talk can occur when the WiGLAN system operates. They are the On-Chip Signal Cross-Talk and the Spatial Channel Signal Cross-Talk. The cross-talk level of the first type is related to the particular circuit and system design techniques used. The level of the second type is determined by the characteristics of the space channel or the environment where the system operates. We usually have little control over the characteristics of the space channel.

One may ask, since there is already cross-talk in the space channel, why should we be concerned about the on-chip signal cross-talk? The reason lies in that the on-chip signal cross-talk stays almost constant or varies very little with respect to time while the spatial channel signal cross-talk varies randomly in time. The effectiveness of STC depends on the randomness of the overall channel, which includes both the on-chip channel and the space channel. The deterministic nature of the on-chip channel limits the randomness of the overall channel. Therefore, the on-chip signal cross-talk can undermine the overall system performance once it exceeds a certain level. In order to model the WiGLAN correctly and ensure flexibility in quantifying the cross-talk effects, we will make both the modulation coding scheme and the performance characteristics of each circuit block adjustable. Thus, we will be able to quantify the cross-talk level of systems of different digital modulation schemes and different individual circuit performance.

Linear Power Amplifier Design for WiGLAN

Personnel

A. Pham (C.G. Sodini)

Sponsorship:

MARCO Focused Research Center for Circuits, Systems and Software (C2S2) (MARCO/DARPA)
and Center for Integrated Circuits and Systems (CICS)

The goal of this research is to build a power amplifier suitable for the WiGLAN (Wireless Gigabit per second LAN) project. In order to get such a high throughput, multiple orthogonal n-QAM modulation channels are used which require power amplifiers with extremely high linearity. However, conventional power amplifiers usually have to trade efficiency for linearity. There are two main sets of solutions to overcome this limitation. First, linearization techniques can be used to boost linearity of highly efficient amplifiers. Examples include envelope-error-restoration, Cartesian-loop feedback, ... Second, adaptive biasing techniques can be used to improve efficiency of linear power amplifiers. The power amplifier proposed in this project uses an adaptive current biasing technique as described below.

Due to their high bias conditions, conventional class A and AB power amplifiers are very inefficient, especially at backed-off power levels. For a conventional fixed-bias amplifier, the dc supply power is constant across the output range at $P_{dc} = V_q I_q$. The efficiency is highest at the maximum output power where both the current and voltage achieve their maximum swings. At lower output levels, the current and voltage amplitudes are reduced. However, the dc supply voltage and current remain unchanged. Therefore, the efficiency decreases rapidly as the output power is reduced as shown in Figure 17.

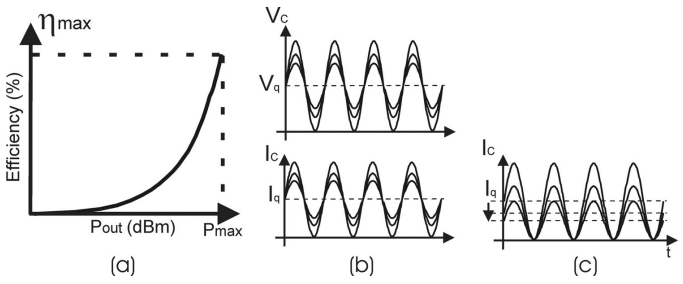


Fig. 17: (a) Typical Efficiency Curve (b) Fixed-Bias Waveforms (c) Adaptive Current Biasing

To improve efficiency at low output levels, the bias current is adjusted dynamically based on the input signal level. When the output power is reduced, the efficiency can be improved if the bias current (I_q) can be adjusted so that the current swing is to the edge of clipping for every input power level as shown in Figure 17c. Essentially, the bias circuit is a voltage controlled current source, which consists of an input level detector, a rectifier, and an averaging circuit as shown in Figure 18.

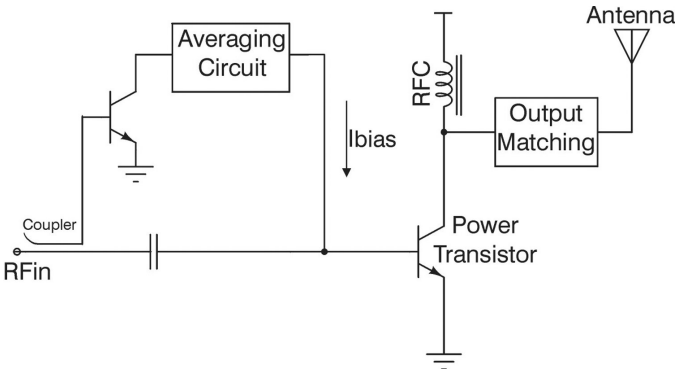


Fig 18: Adaptive Current Biasing Block Diagram

The amplifier is designed for the 5.8 GHz UNII-band and fabricated using the IBM SiGe 7HP BiCMOS process. Using the proposed adaptive current biasing technique, the amplifier exhibits significant improvement in efficiency at low output power while maintaining good linearity. The efficiency at low power levels increases as much as two times compared to the fixed-bias version. At maximum linear output power of 19.2 dBm, the power amplifier shows 30% Power-Added-Efficiency (PAE), and 16.45 dB gain with -35.46 dBc Adjacent Channel Leakage Power Ratio (ACPR) operating at a supply voltage of 2.5V.

Smart Active-Matrix Display Drivers For Organic Light Emitting Devices

Personnel

M. Powell, J. Yu (V. Bulovic and C. G. Sodini)

Sponsorship

MARCO Focused Research Center for Circuits, Systems and Software (C2S2) (MARCO/DARPA) and
Center for Integrated Circuits and Systems (CICS)

In this project we are developing pixilated active matrix "smart drivers" for displays consisting of organic light emitting devices (OLEDs). Organic LEDs are perhaps the most promising novel technology for development of efficient, pixilated, and brightly emissive, flat-panel displays. They naturally emit over large areas, and offer the advantage of growth on lightweight and rugged substrates such as metal foils and plastic, with no requirement for lattice-matching.

Organic LED devices, however, exhibit non-liner light output responses that complicate their implementation in an application requiring a fine control of the output light intensity. Specifically, the I-V characteristics of OLEDs depend on the cathode/anode type, device layer thickness, and operating temperature. The power efficiency of pixels in a display will drift over time due to operational degradation. The individual pixels in a display can then exhibit different aging, in accordance with their use. The brightness non-uniformities due to the differential aging will reduce the useful display lifetime.

Our smart active matrix circuitry compensates for the OLED non-uniformities by monitoring light output and adjusting the driving conditions according to the OLED performance. The adjusted output provides a defect-free picture. In the final design a Si *p-n* detector integrated behind each pixel will give feedback to the driver circuits that will adjust the proper current level to derive a constant brightness output. Figure 20 shows a typical integrated structure in which our patented transparent OLED is used. In this design both OLED electrodes are capable of transmitting the emitted light which is mostly observed on the top, but is also partially absorbed in the detector. The integrated circuit layout of the mini-display is shown in Figure 21. Notice that six transistors control each pixel (Figure 20). Also, each column shares one feedback circuitry. The integrator type of compensation is used for each feedback circuitry to ensure that the light output is matched to the reference input. The values of discrete components were so chosen to stabilize the feedback loop.

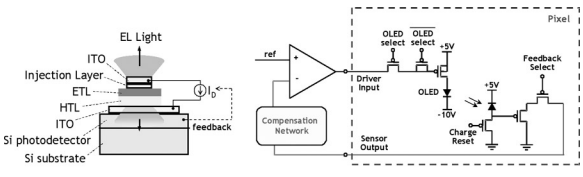


Fig. 19 (left) An OLED pixel integrated with a "smart" si active matrix driver. The si photodetector monitors the intensity of the OLED pixel during the on state and provides feedback to the driving circuit to keep the light output intensity constant as the device efficiency changes with operation. (Right) pixel design in integrated circuit implementation

The present state of the art of OLED display technology uses a constant current to drive an OLED pixel. In this driving scheme even the most efficient of OLEDs will drop their luminescent output to 90% of the 100 Cd/m^2 initial brightens in ~ 5000 hours. As a human eye can distinguish brightness change of less than 10%, the 90% operating point indicates the longest useful lifetime of a pixel in a display.

With the circuit developed in this project we compensate for the loss of brightness of an aging OLED pixel by increasing the operating (driving) voltage as

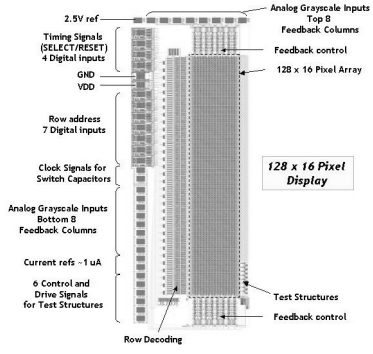


Fig. 20: 28 x 16 pixel integrated circuit layout.

continued

a function of time. The lifetime of such compensated pixel is now primarily limited by the maximum voltage that the driving circuit can deliver. From the data of Figure 22 we project that for the maximum driving circuit voltage of 10V, the constant pixel brightness can be sustained for 30,000 hours by doubling the initial drive current, and for the maximum driving voltage of 12V, the constant pixel brightness can be sustained for 50,000 hours by tripling the initial drive current. Such long projected lifetimes would enable the use of OLEDs in commercially viable displays.

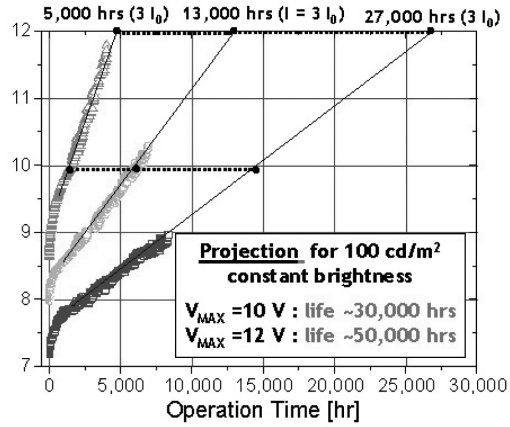


Fig. 21: Driving circuit voltage increase the proposed display driving scheme that compensates for the aging of an OLED.

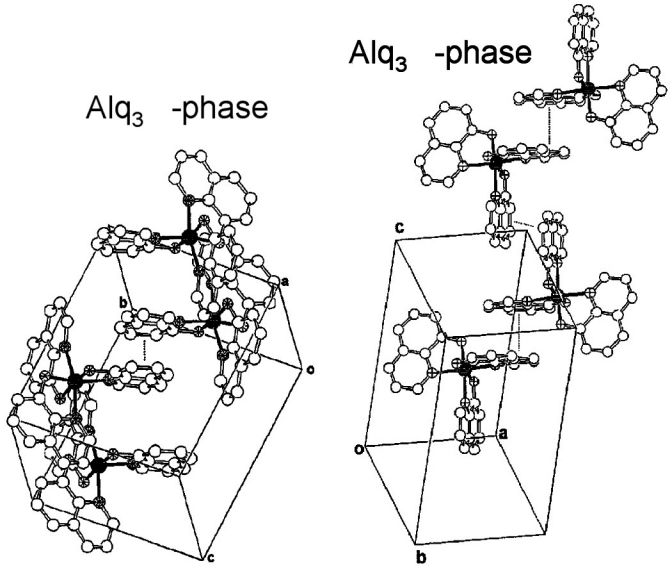


Fig. 22. α nd β crystal forms of Alq3. (from Brinkmann, et al.*, J. Am. Chem. Soc., 122, 5147 (2000).*

A CMOS-Compatible Compact Display

Personnel

A. Chen (A.I. Akinwande and H.-S. Lee)

Sponsorship

3M and MARCO Focused Research Center on Integrated Circuits and Systems (C2S2) (MARCO/DARPA)

The proliferation of portable electronic systems has created demand for high-resolution displays which are compact and highly energy-efficient. We have designed and built a proof-of-concept for a display that meets these design constraints. Our display uses a standard digital CMOS integrated circuit to produce a low-brightness image, and an image intensifier to increase brightness to a visible level. Exploiting high level of integration achieved by the CMOS IC, low power techniques such as pixel memory and data compression can be implemented to lower the system power consumption. We are exploring the use of high-accuracy calibration techniques for the display driver circuits. We are designing the driver circuit for compatibility with other emissive display technologies such as organic LEDs so that a single driver circuit can be employed in multiple display technologies. A display using our design should produce a daylight-visible image using approximately half a watt of power.

Silicon devices can convert electrical energy into light, although their efficiency is very low. We use silicon light-emitting diodes to produce a very faint image which is optically coupled into an image intensifier. The image intensifier is a compact vacuum device that uses cathodoluminescence to increase the brightness of an image. It is commonly found in night vision scopes and scientific equipment. The intensifier in principle can be built very compactly by using multiple channel plates with MEMS technology. Cathodoluminescence, using a phosphor to convert electrons to photons, is an established technology used in cathode-ray tubes. Cathodoluminescent devices have high conversion efficiency (40 lumens/watt), high reliability, and can achieve very high output brightness (projection televisions).

We produced a laboratory demonstration of the system. An integrated circuit with light-emitting arrays was fabricated in a commercial 0.18μm CMOS logic process. Each array measured 16x32 pixels and included a word-line decoder. Each pixel contained a 1-bit digital memory along with light emitter and driver circuits. Sample images were recorded, as shown below.

We are exploring circuit designs to support the integration of light emitters onto CMOS integrated circuits. Memory can be added to the display to eliminate the need for refreshing, thus reducing switching power. In addition, row parallel current level addressing is being

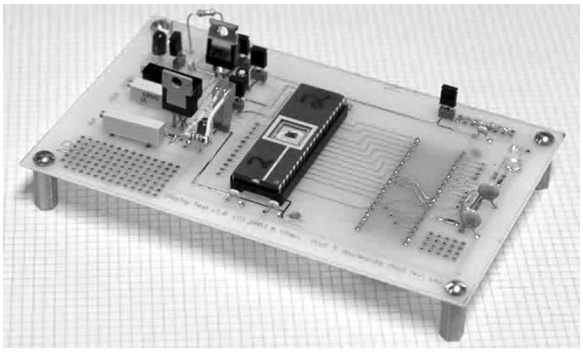


Fig. 23: Circuit board including IC in 0.18μm CMOS process.

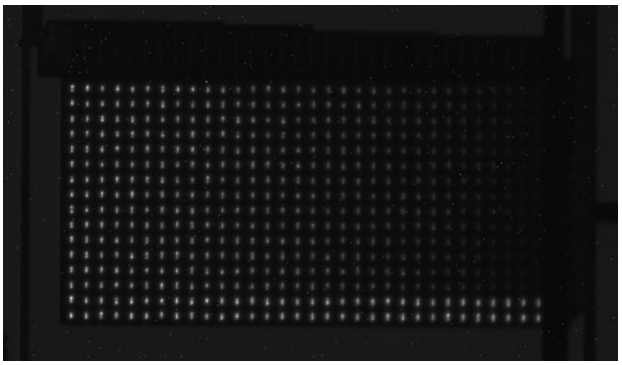
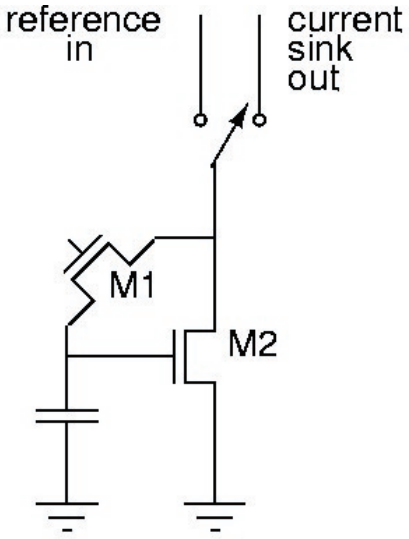


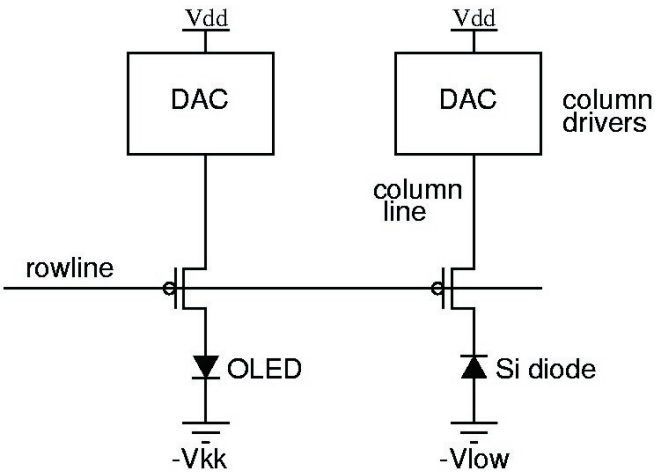
Fig. 24: 32-level grayscale image from test system captured with CCD camera.

continued

investigated. Calibration techniques are used to overcome manufacturing process variation and allow precise brightness control of each pixel. In addition, we believe our circuit designs will be capable of supporting multiple emissive display technologies. Our current target is a silicon backplane which can drive (1) silicon light emitters with image intensifier, and (2) an organic LED.



Current Copier circuit used for row driver calibration



Potential use of identical driver circuitry for multiple display technologies

Fig. 25

A Programmable, Wide Dynamic Range CMOS Imager with On-Chip Automatic Exposure Control

Personnel

P. M. Acosta Serafini (C. G. Sodini and I. Masaki)

Sponsorship

Intelligent Transportation Research Center (ITRC)

Machine vision applications which use visual information typically need an image sensor able to capture natural scenes which may have a dynamic range as high as four orders of magnitude. Reported wide dynamic range imagers may suffer from some or all of these problems: large silicon area, high cost, low spatial resolution, small dynamic range increase factor, poor pixel sensitivity, small intensity resolution, etc. The primary focus of the proposed research is to develop a single-chip imager for machine vision applications which addresses these problems, but is still able to provide an ultra wide intensity dynamic range by implementing a pixel-by-pixel automatic exposure control. The secondary focus of the research is make the imager programmable, so that its performance (light intensity dynamic range, spatial resolution, light intensity resolution, frame rate, etc.) can be tailored to suit a particular machine vision application.

The imager sensing array has pixels which can be independently read and reset. The proposed brightness adaptive algorithm then predictively scales the voltage in photodiodes that would saturate under normal circumstances based on information gathered in several readout checks. The total integration time is subdivided into several integration times (called integration slots), which are progressively shorter. If in any of the checks it is determined that the pixel will saturate at the end of the current integration slot, then the pixel is reset and is allowed to once more integrate light, but for a shorter period of time. Each pixel has a small associated memory location needed to store an exponent which identifies the actual integration slot used. This information is used to appropriately scale the digitized pixel output.

A proof-of-concept integrated circuit has been fabricated in 0.18um 5M CMOS process shown below in Figure 26. It includes a 1/3" VGA (640x480) array (7.5μm square pixels), 64 cyclic analog-to-digital converters for digital pixel output, an integration controller which implements the described algorithm, 4-bit per-pixel SRAM memory for exponent storage and supporting digital logic.

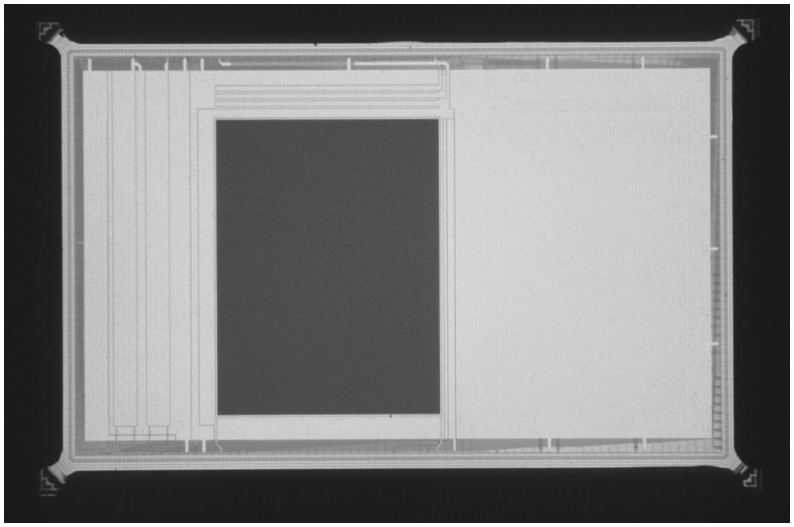


Fig. 26: Die photo of programmable wide dynamic range CMOS image.

Mixed-Signal Design in Deeply Scaled CMOS Technology

Personnel

J. Fiorenza (H.-S. Lee and C. G. Sodini)

Sponsorship

Center for Integrated Circuits and Systems (CICS) and MARCO Focused Research Center for Circuits, Systems and Software (C2S2) (MARCO/DARPA)

There are tremendous challenges in implementing mixed-signal systems on a single substrate in deeply scaled CMOS technologies primarily due to the negative impact of the technology on analog circuits. Nearly every aspect of scaling except speed goes against analog circuits. Lower power supply voltage severely restricts the signal range, requiring substantially lower circuit noise in order to keep the signal-to-noise ratio. Small geometry transistors exhibit far less voltage gain and greater threshold voltage mismatches than their predecessors. Attempts to overcome device gain limitations with conventional techniques such as cascode and regulated cascode aggravate already slim signal swing. The use of long-channel devices for higher gain inevitably compromises the circuit speed.

In order to overcome the challenges, we are exploring innovative circuit techniques that avoid shortcomings of deeply scaled technologies, and actually exploit them in mixed-signal systems. As the first step we have been investigating circuit techniques that overcome the device gain limitations without penalizing the signal swing or circuit speed. An innovative approach that we have developed employs two signal paths: the main path and the prediction path. The prediction path processes the signal ½ clock phase earlier than the main path at a reduced accuracy. The information obtained from the prediction phase is used in the main path in order to compensate for the finite device gain, incomplete settling, and other non-idealities. The two-path approach can be applied to many different classes of analog circuits including data converters, filters, instrumentation amplifiers, and many others. Compared with previous techniques of effective gain enhancement, the proposed technique incurs little penalty in power consumption – an important measure often ignored in the literature. As the initial proof-of-concept, we designed a MOS sample-and-hold amplifier in a standard 0.18 μ digital CMOS process. The simulation predicts the accuracy corresponding to 100dB amplifier gain with no cascading. The chip has been fabricated and shown to be functional, and is currently undergoing performance evaluation.

A CMOS Bandgap Current and Voltage References

Personnel
M.C. Guyton (H.-S. Lee)

Sponsorship
Center for Integrated Circuits and Systems (CICS)

Most analog circuits require reference voltages and currents that do not vary with power supply voltages and temperature. Bandgap voltage references with an output voltage around 1.2 volts have been popular for this purpose. However, producing current sources referenced to bandgap voltage requires an operational amplifier increasing the complexity and power consumption.

The focus of this research is to develop simple and low power bandgap current references. We have developed a novel bandgap core circuit that produces a bandgap referenced output current directly without an operational amplifier. This simple circuit can even be operated as a 2-terminal bandgap current source. The same core circuit can also be used to generate arbitrary non-integer multiples of bandgap voltage.

A prototype 2-terminal band-gap current source has been designed and fabricated employing only 4 MOS transistors and 2 parasitic PNP transistors in a standard 0.35μ CMOS technology.

This chip shows full functionality. At a nominal 2V supply voltage and 80 μA output current, the entire circuit dissipates 160 μW, requiring no excess power consumption other than that of the current source itself. The measured output resistance is 350 kΩ. Since the design was performed without prior temperature characterization of components such as the bipolar transistors and resistors, the trimming range was found to be inadequate for achieving minimum temperature coefficient. Over 5°C – 50 °C temperature range, the temperature coefficient is 142 ppm/V.

Flicker Noise in Scaled CMOS Devices

Personnel
T. Sepke (H.-S. Lee and C. G. Sodini)

Sponsorship
MARCO Focused Research Center for Circuits, Systems and Software (C2S2) (MARCO/DARPA), Center for Integrated Circuits and Systems (CICS), Maxim Fellowship

Research of flicker noise in MOSFETs encompasses a large body of work spanning several decades. The number fluctuation model explains the source of flicker noise as the trapping of channel electrons in the gate oxide. Traps deeper in the oxide have longer time constants associated with them than traps closer to the channel, resulting in a non-white Power Spectral Density (PSD). A uniform distribution of traps in the oxide produces a PSD that is inversely proportional to frequency. The traps can also be distributed in energy in the oxide resulting in a gate voltage dependence. In addition to channel carrier number fluctuations, the trapped charges create an electric field, which results in mobility fluctuations that are correlated with the trapping events. A complete number fluctuation and correlated mobility fluctuation model was originally presented by Jayaraman and Sodini (IEEE Elec. Dev. 1989), and a simulation adapted form by Hung, Ko, Hu, and Cheng (IEEE Elec. Dev. 1990).

Assuming a simple scaling of devices (L/s, W/s, sC_{ox}), the number fluctuation model predicts no change in the flicker noise voltage at the gate with device scaling. One figure of merit that is of interest to circuit designers is the flicker noise corner frequency which is defined as the frequency where the flicker noise PSD is equal to the thermal noise PSD. Again using the simple scaling defined above, the number fluctuation model, and the square-law drain current model, it can be shown that the corner frequency increases proportional to the scaling factor s.

A simulation study has been performed comparing the noise of 0.25μm and 0.18μm transistors. The models predicted flicker noise corner frequencies as high as 100MHz. They also predict a dramatic decrease in the amount of flicker noise when transitioning from strong inversion to subthreshold. In order to investigate the flicker noise, a measurement system for on wafer devices has been designed and is currently being

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implemented. Several devices of different sizes and under different bias conditions will be measured and analyzed. Of special interest are the weak to moderate inversion regimes, and bias points desirable for analog circuit designs.

Upon exploring the behavior of scaled devices, any generalizations or insights will be applied to an analog or RF circuit design application. The circuit design will be made with the goal of mitigating effects of increased flicker noise in future technologies.

Device Level Optimization of Phase Noise in Integrated LC VCOs

Personnel

A. Jerng (C.G. Sodini)

Sponsorship

Center for Integrated Circuits and Systems (CICS)

Integrated LC Voltage-Controlled Oscillators (VCOs) are essential components in wireless systems. The Wireless Gigabit Local Area Network (WiGLAN) project aims to achieve a data rate of 1 Gb/s using 150 MHz of bandwidth in frequency bands allocated in the 5-6 GHz range. An adaptive M-ary modulation scheme, up to 256-QAM, is chosen to provide the required data rates, imposing stringent accuracy requirements on the Local Oscillator (LO) signal. VCOs with low phase noise and high operating frequencies are required. In addition, there is a desire to maintain compatibility with integration trends such as lower supply voltages. This research focuses on the design of a 5 GHz LC VCO based on 0.18 μm CMOS devices using a 1.8 V supply.

Phase noise analysis is complicated by the non-linear and time-varying nature of an oscillator. Recent research has identified bias circuit noise as an important contributor to phase noise. Upconverted flicker noise from MOS devices degrades close-in phase noise. Understanding the mechanisms through which circuit noise converts into phase noise is essential to the optimization of phase noise performance. Our design approach has been to develop models for the different phase noise conversion processes and to understand the relationship between device parameters such as g_m and f_t and the phase noise mechanisms. The resulting design intuition will allow us to treat and optimize the various phase noise sources independently, and understand the device-level tradeoffs involved in high frequency CMOS VCO design.

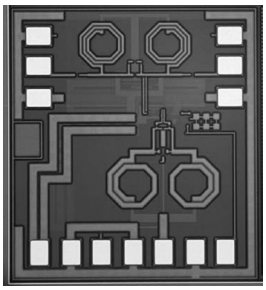

Fig. 27

We have designed and fabricated an experimental set of seven VCOs using IBM's BiCMOS 7HP process technology (See Figure 27). Key device parameters were varied across the experimental set through choices of device type and device sizing, while keeping circuit parameters such

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continued

as supply current, voltage swing, and LC tank elements fixed in order to allow insightful comparisons of phase noise. The experimental data allows us to quantify the relative contributions of bias noise, MOS thermal noise, and MOS flicker noise to phase noise and to understand the impact of the device parameters on their contributions.

We have found that bias noise and flicker noise contributions to phase noise can be minimized through proper MOS device sizing. In addition, we have observed that 0.18 μm PMOS devices exhibit better measured phase noise than 0.18 μm NMOS devices due to lower drain thermal noise (See Figure 28). Our work has resulted in an optimized all-PMOS VCO topology demonstrating low voltage low phase noise performance at 5.3 GHz.

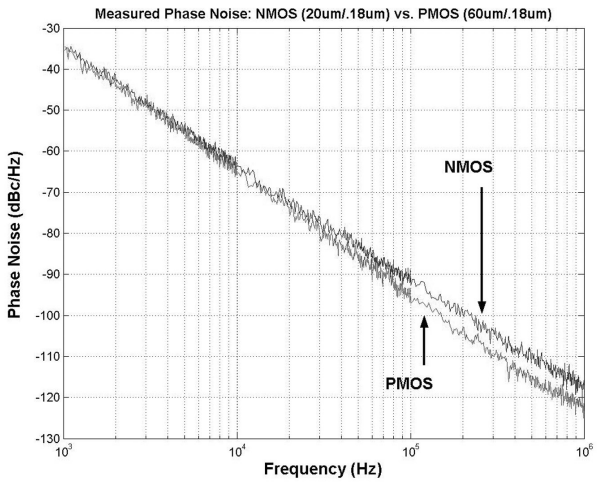

Fig. 28

Radio Frequency Digital-to-Analog Converter

Personnel

S. Luschas (H.-S. Lee)

Sponsorship

National Semiconductor Fellowship and Center for Integrated Circuits and Systems (CICS)

Dynamic performance of high speed, high resolution, DACs is limited by distortion at the data switching instants. Inter-Symbol Interference (ISI), imperfect timing synchronization, and clock jitter are all culprits. A DAC output current controlled by an oscillating waveform is proposed to mitigate the effects of the switching distortion. The oscillating waveform should be a multiple (k*fs) of the sampling frequency (fs), where k >1. The waveforms can be aligned so that the data switching occurs at the peak and/or the valley of the oscillating current output. This makes the DAC insensitive to switch dynamics and jitter. The architecture has the additional benefit of mixing the DAC impulse response energy to a higher frequency. Instead of the conventional sinx/x DAC impulse response roll-off, there is a large high frequency lobe near the control oscillating waveform frequency (k*fs). An image of a Low Intermediate Frequency (IF) input signal can therefore be output directly at a high IF or Radio Frequency (RF) for transmit communications applications.

A narrowband sigma-delta DAC with eight unit elements was chosen to implement the RF DAC concept. A sigma-delta architecture allows the current source transistors to be smaller since mismatch shaping is employed. Smaller current source transistors have a lower drain capacitance, allowing large high frequency output impedance to be achieved without an extra cascode transistor. Elimination of the cascode reduces transistor headroom requirements and allows the DAC to be built with a 1.8V supply. The RF DAC is fabricated in a 0.18 μ digital CMOS process. Measured single-tone SFDR is 75dB and SNR is 52dB, while two-tone IMD3 is 70.8dBc over a 17.5MHz bandwidth centered at 942.5 MHz.

Low Power RF Front-End for Wireless Microsensor Systems

Personnel
A. Y. Wang (C. G. Sodini)

Sponsorship
ABB and NSF Fellowship

The design of wireless microsensor systems has gained increasing importance for a variety of commercial and military applications. With the objective of providing short-range connectivity with significant fault tolerance, these systems find usage in such diverse areas as environmental monitoring, industrial process automation, and field surveillance.

The main design objective is maximizing the battery life of the sensor nodes while ensuring reliable operation. For many applications, the sensors need to "live" for 1-5 years without battery replacement. To achieve this goal, the microsensor system has to be designed in a highly integrated fashion and optimized across all levels of system abstraction. This also means that all the characteristics particular to the microsensor system must be exploited. One such characteristic is that the RF output power is small due to the short transmission distance, which makes the transceiver electronics the dominant source of energy dissipation.

In this research the impact of circuit non-idealities including noise, nonlinearity, and modulation errors upon system performance are analyzed, and these effects are incorporated into the design of key front-end components. In addition, the effect of increasing the RF transmit power, which is small, to compensate for the SNR loss due to circuit non-idealities is investigated. This can potentially lower the performance specification of the RF front-end and reduce the over-all power consumption.

Substrate Noise Coupling and Reduction Techniques in Mixed-Signal Systems

Personnel
M. S. Peng (H.-S. Lee)

Sponsorship
Center for Integrated Circuits & Systems (CICS), MARCO Focused Research Center for Circuits, Systems and Software (C2S2) (MARCO/DARPA)

The demands of lower power, higher speed, and lower cost have driven the integration of all circuits in a system, analog and digital, onto a single chip. In this integration, one of the primary problems is substrate noise coupling. Digital circuits create noise, which couples into the sensitive analog circuits through the shared substrate. Improperly accounted for, this substrate noise can degrade analog performance drastically.

Up to now, most efforts in addressing this problem have been to ensure that analog circuits are robust enough to withstand the digital substrate noise. These techniques include physical separation, differential architectures, and simulation. Little effort has been placed on reducing the substrate noise itself.

With this in mind, the focus of this research is to investigate the characteristics of the substrate noise seen in analog circuits as well as ways to cancel the substrate noise. We have implemented a test chip that includes different digital circuits as substrate noise generators and a delta-sigma A/D converter that samples the substrate noise as well as an external signal.

Substrate noise is characterized by observing the output of the delta-sigma converter built on the test chip to measure the substrate noise. By operating one digital circuit, an array of large inverters which mimics digital I/O drivers so that it produces a periodic noise waveform on the substrate, the delta-sigma modulator can be used as an accurate on-chip sampling scope to map the substrate noise as a function of time. The delta-sigma converter is ideal as the sampling scope because of the inherent averaging effect and 1-bit output that simplifies the interface. The sampling edge of the delta-sigma A/D converter is moved relative to the digital clock edge so that the substrate noise waveform can be reconstructed from the delta-sigma converter output. Figure 29 shows an example of the substrate noise generated by low-to-high and high-to-low inverter transitions and measured using this technique.

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In order to reduce the effect of the substrate noise, a feedback loop that shapes the substrate noise in bands of interest has been implemented and tested. This type of noise shaping is well suited for band-limited analog applications. While the concept is demonstrated in a low-pass system, the same principle can be used in band-pass systems.

The substrate noise shaping loop is based on a delta-sigma modulator loop with the substrate noise treated as quantization noise. The feedback D/A is replaced by an array of transient-injecting inverters. This has the advantages of simplicity, low power, complementarity to existing substrate noise reduction techniques, and no restrictions on analog or digital circuit design. Figure 30 shows the substrate noise reduction seen in a delta-sigma modulator. The substrate noise is seen to be reduced by 20 dB when the substrate noise shaping loop is engaged. Signal to noise plus distortion ratio (SNDR) of a sampled-data analog circuit, in this case another delta-sigma converter, is increased by 10dB. Substrate noise was generated by large inverters which imitate the substrate noise generated by large I/O drivers. We believe further improvement is possible by carefully managing aliasing of the substrate noise in the noise shaping loop as well as in the sampled-data analog circuits.

The test chip with the substrate noise characterization system and the substrate noise shaping system runs at 2.5V and has been fabricated in conventional 0.25μm CMOS technology.

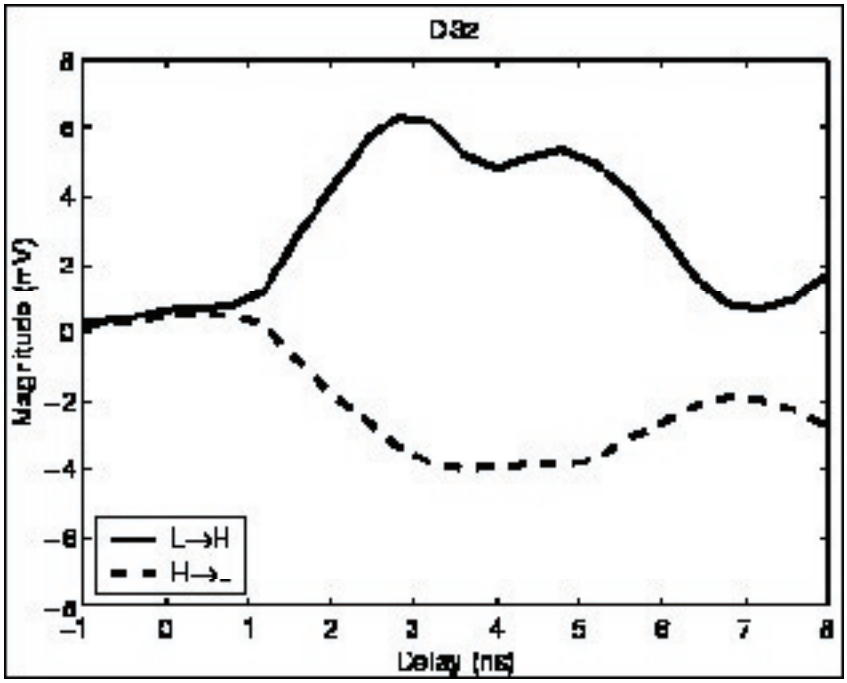

Fig. 29: Measured substrate noise with an on-chip sampling scope.

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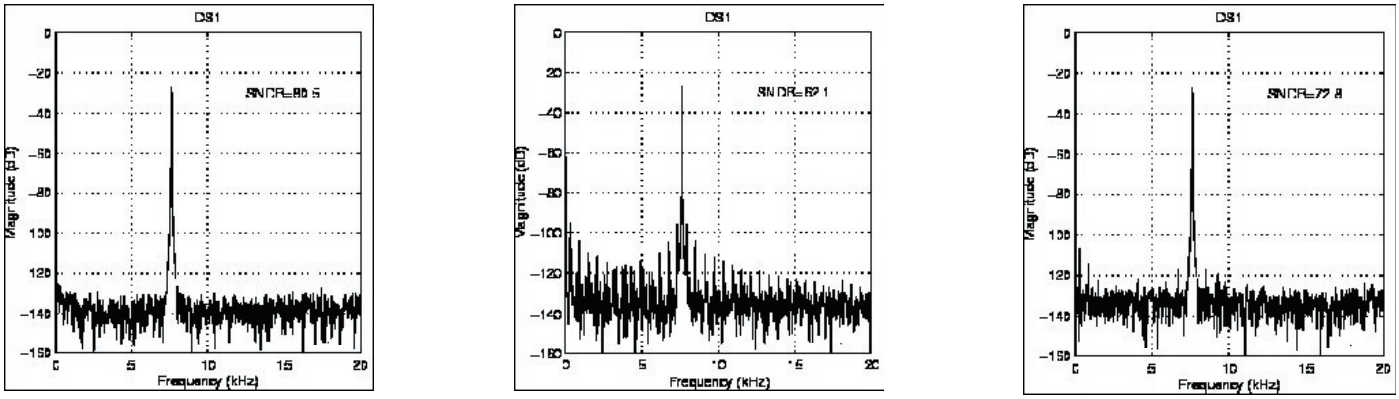

(a) **(b)** **(c)**

Fig. 30: Delta-sigma converter outputs with a 7.6kHz input signal. (a) Substrate noise generator off, substrate noise shaping loop off. (b) Substrate noise generator on, substrate noise shaping loop off. (c) Substrate noise generator on, substrate noise shaping loop on.

An Advanced Model Based Vision System for Intelligent Transportation Systems

Personnel

M. Kais (C. Laugier, M. Parent, I. Masaki and B.K.P. Horn)

Sponsorship

Intelligent Transportation Research Center (ITRC), Lounsbery Foundation, and INRIA

In order to offer better safety and increase the capacity of the roads, new concepts of mobility are being developed. These advanced transportation systems are based on autonomous driving and platooning. Platooning applications consist of creating a platoon of electronically coupled vehicles with a very small headway. In a platoon, the first vehicle is manually or automatically driven and the others follow. Another application is driverless fully autonomous electric vehicles called cybercars (See Figure 31) for transportation in urban environment.

Fig. 31: A cybercar

These applications require sensors for the guidance and obstacle detection tasks. The goal of the vision system is to build an accurate representation of the environment in front of the vehicle to be used by the planning layer. Stereo vision offers a low cost and easy way to get some range information about the environment. Traditional vision systems are fine for the highway environments, because they are well defined (size, marker). However, urban environments present a challenging task due to the complexity of the scenes. For instance, in a single frame, the road and lane boundaries can take on several primitives, such as a curb, a white lane marker, or a line of cars parked on the side of the road.

Fig. 32: Results from the lane marker detector

Our approach consists in fusing information from the cameras with some a priori knowledge stored in a database. This a priori knowledge consist of a global model i.e. an environment model (how the roads are linked), a geometric model of the road and lane boundaries (shape) and a model of the road and lane boundaries feature (lane marker, curb, planes). This global model is acquired during a learning phase and linked to an existing geographic database using a Geographic Information System. Once the learning phase is completed, the estimate of the position of the vehicle and the a priori knowledge are used to enable some specialized detectors in specific Regions Of Interest (See Figure 32) in order to extract from the images relevant information that is used for the 3D reconstruction.

Efficient Traffic Monitoring

Personnel
N.S. Love (I. Masaki and B. K. P. Horn)

Sponsorship
Intelligent Transportation Research Center (ITRC)

Traffic control centers use several methods to monitor traffic conditions. Currently, the most popular methods involve the use of cameras (image sensors) at high-density traffic locations. The cameras are controlled at the traffic control centers. The traffic control center has on the order of 10 monitors and hundreds of cameras; each monitor cycles through a set of cameras while operators watch for any traffic incidents. This system is currently implemented using dedicated analog lines which have a low bandwidth. Bandwidth limitations inhibit the efficient transmission of network data. Consequently, the load due to a continuous transmission of images severely impacts the network's performance.

Our system reduces transmission load by distributing the processing of images to the image sensor and the control of transmission to mobile agents. Each image sensor processes each image and determines the contents of the image, and mobile agents decide if the image, traffic information, or nothing is sent to the traffic control center. The goal of this work is to reduce the transmission load of image sensor networks by distributing processing tasks to image sensors and reducing image transmission using mobile agents.

In the case of traffic monitoring, traffic images are processed at the control center to determine the average speed of vehicles or the number of vehicles that pass through a checkpoint during some time interval (traffic flow). Distributing the processing to the image sensors involves using an image sensor network to perform object recognition and image compression on the images at the image sensor before the image reaches the control center.

Providing select images to the user is achieved thru mobile agents. The control center dispatches mobile agents which search for images according to a user preset priority criteria. At an image sensor, each image is acquired and processed; the contents of the image are determined (number of vehicles, average speed of vehicles, whether there has been an accident or a sharp change in traffic conditions) and a priority is set to the image. The mobile agent from the control center checks when the image is updated and the level of priority of the image. The mobile agent decides if an image is sent back to the control center or information from the image based on the preset priority criteria. Figure 33 shows the components of the network and their interaction. By sending the mobile agent to intelligently decide the transmission of the image or traffic information, the transmission load is reduced.

Each sensor has a processor which acquires images and performs a three-dimensional contour based image compression algorithm on each image. The 3D image compression algorithm is a lossy compression method that retains three components: contour, color, and distance information. Each component can be used together or separately to aid in object recognition without fully decompressing the image.

Edge tracing determines the contours in the image. A modified differential chain coding method is used to further compress the contours. Differential chain coding codes the position of the first edge in the contour and the differential direction of the remaining edges in the contour. Differential chain coding does not follow contours that branch. We modified the differential chain coding to include branching for a more complete representation of the contour and to increase compression of the contour. The modification is a depth-first traversal of the contour with the addition of a marker to signify a split and a marker to signify a return to a split location. The additions of these two markers increase compression by eliminating the need to code start locations at the split. Start locations are costly to encode depending on the size of the image, the larger the image the more bits are needed to encode the start locations. Encoding each marker is 4 additional

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bits. The savings of encoding the markers verses the start locations is seen in images that are larger than 64x64.

Finding the color on each side of the contour retains color information. To improve the quality of the decompressed image, the mean color of blocks between contours can also be included in the compressed image.

The distance information is obtained using a stereo vision algorithm. The cameras are aligned on a horizontal bar, and images are captured simultaneously from both cameras. Assuming the relative orientation (rotation and translation) between the cameras is known, the distance from one camera to an object can be determined by finding corresponding points in both images. Figure 34 shows the camera general setup of a stereo vision system.

Object recognition is performed on the compressed images to determine traffic flow and incident detection. The image sensor assigns a priority level to each image based on its contents (i.e. traffic congestion has medium priority, accidents have high priority, etc…).

The vehicles are detected by grouping features of each contour. The features used are depth, motion, and position. The vehicles are modeled with a multivariate Gaussian distribution using the Expectation-Maximization algorithm (EM), which is a maximum likelihood estimate, to approximate the scene as a mixture of Gaussian distributions. EM is a statistical clustering method which gives the mean, standard deviation, and weight of each cluster. Each cluster represents an object in the image. An object is detected by determining which cluster each contour belongs to and placing a bounding box around the contours in the same cluster. A contour is linked to a cluster with the minimum Mahalanobis distance. The Mahalanobis distance is a distance with each dimension scaled by the variance.

Once the vehicles are detected, the vehicles are tracked to determine the average speed, number of vehicles, traffic flow information, and incident detection. Once the image sensor gathers traffic information, mobile agents can determine whether the information is transmitted over the network.

Using the image sensor and mobile agents to complete processing tasks and to retrieve select images reduces the network's transmission load. For example, a police station dispatches a mobile agent to the cameras. The police station requests images with the criteria for high priority level accidents. The mobile agent will only retrieve those images with accidents. Transmission of traffic accident images versus all available images improves the network efficiency. The research develops a demonstration where mobile agents are sent with a given criteria to several camera locations where images are retrieved based on preset criteria.

Reduction of the transmission load will enable more users to obtain information without loss of performance. Distributed processing helps to minimize the transmission load by using the image sensors to complete normal processing tasks as opposed to processing at the control center. Mobile agents are equipped with the appropriate criteria to sift through the traffic information and to provide current traffic images and information to the user. The agents complement the image sensor network by providing select images based on criteria set by the user; using both mobile agents and image sensors, the network performance will be improved.

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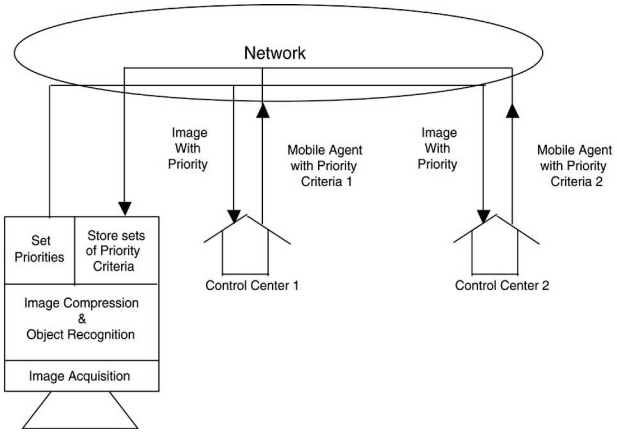


Fig. 33: Network Components

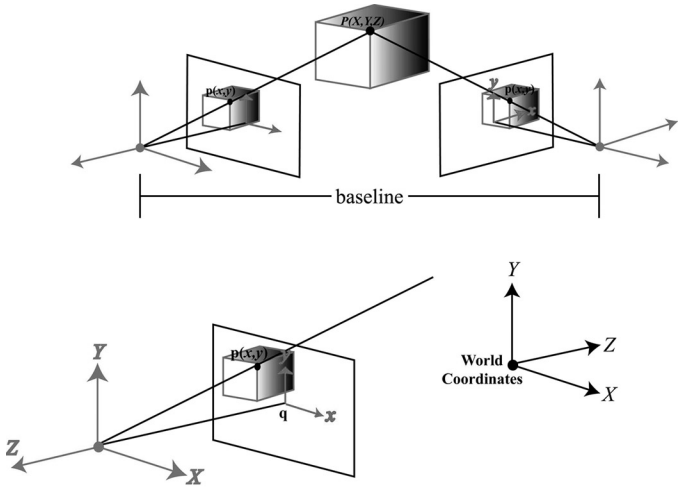


Fig. 34: Stereo Vision Setup

Sensor Fusion for Automobile Applications

Personnel
Y. Fang (I. Masaki and B.K.P. Horn)

Sponsorship
Intelligent Transportation Research Center (ITRC) at MIT's MTL

To increase the safety and efficiency for transportation systems, many automobile applications need to detect detail obstacle information. Highway environment interpretation is important in Intelligent Transportation Systems (ITS). It is expected to provide 3D segmentation information for the current road situation, i.e., the X, Y position of objects in images, and the distance Z information. The needs of dynamic scene processing in real time bring high requirements on sensors in intelligent transportation systems. In complicated driving environment, typically a single sensor is not enough to meet all these high requirements because of limitations in reliability, weather, and ambient lighting. Radar provides high distance resolution, while it is limited in horizontal resolution. Binocular vision system can provide better horizontal resolution, while the miscorrespondence problem makes it hard to detect accurate and robust Z distance information. Furthermore, video cameras could not behave well in bad weather. Instead of developing specialized image radar to meet the high ITS requirements, sensor fusion system is composed of several low cost, low performance sensors, i.e., radar and stereo cameras, which can take advantage of the benefit of both sensors.

Typical 2D segmentation algorithms for vision systems are challenged by noisy static background and the variation of object positions and object size, which leads to false segmentation or segmentation errors. Typical tracking algorithms cannot help to remove the errors of initial static segmentation since there are significant changes between successive video frames. In order to provide accurate 3D segmentation information, we should not simply associate distance information for radar and 2D segmentation information from video camera. It is expected that the performance of each sensor in the fusion system would be better than being used alone.

Our fusion system introduces the distance information into the 2D segmentation process to improve its target segmentation performance. The relationship between the object distance and the stereo disparity of the object can be used to separate original edge map of stereo images into several distance-based edge layers in which we further detect whether there is any object and where the object is by segmenting clustered image pixels with similar ranges. To guarantee robustness, a special morphological closing operation is introduced to delineate vertical edges of candidate objects. We first dilate the edge to elongate the edge length so that the boundaries of target objects will be longer than that of noisy edges. Then an erosion operation deletes short edges. Typically the longest vertical edges are located at the object's boundary. The new distance-range-based segmentation method can detect targets with high accuracy and robustness, especially for the vehicles in highway driving scenarios.

For urban-driving situations, heavy background noise such as trees, etc., usually cause miscorrespondence, leading to edge-separation errors. The false boundary edge lines in the background area can be even longer than the boundary edge lines. Thus it is hard to eliminate false bounding boxes in background areas without eliminating foreground objects. The noisy background adds difficulties in segmenting objects of different sizes. To enhance the segmentation performance, background removal procedure is proposed. Without losing generality, objects beyond some distance range are treated as background. The pixels with small disparity represent the characteristics of the background.

Sometimes in assigning edge pixels to different edge layers, there exists ambiguity. Without further information it is hard to decide among multiple choices. Some algorithms simply pick one randomly, which might not be true in many situations. Typically, to avoid losing potential foreground pixels, edge pixels are assigned to all distance layers and edge-length filters can suppress ambiguity noise. However, when background noise is serious, algorithm picks only edge pixels without multiple choices. Eliminating pixels from the background in this way will

continued

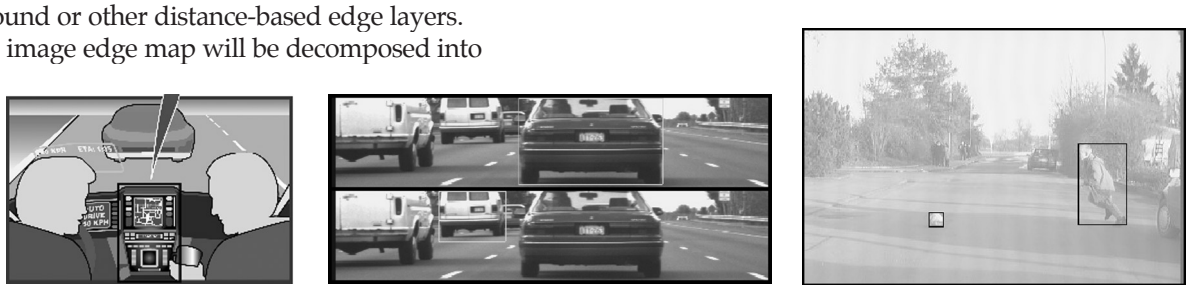
continued

lose significant pixels of target objects, making segmented region smaller than its real size. Thus, motion-based segmentation region expansion is needed to compensate for performance degradation. The original segmentation result can be used as initial object segmentation seeds from which larger segmentation boundary boxes will expand. The enlarging process is controlled by the similarity of segmentation seed boxes and surrounding edge pixels. With such region growing operations, the accurate target sizes are captured.

The proposed depth/motion-based segmentation procedure successfully removes the impact of background noise and captures objects of different sizes.

We presented a new sensor-fusion-based 3D segmentation algorithm to detect target distance and 2D location (See Figure 35). The system consists of following components: "distance-based edge layer separation," "background edge pixel removal," "target position detection," and "motion-based object expansion." The system firstly detects the rough depth range of all targets of interest. Then, we propose a new object segmentation method based on both motion and distance information. The segmentation algorithm is composed of two phases. "Distance-based edge-layer separation" and "background detection" are the first phase, which capture significant edge pixels of objects in interested distance layers while rejecting the noise from either background or other distance-based edge layers. Thus, original image edge map will be decomposed into several distance-based edge maps and heavy background noise can be removed. The advantage of this phase is that detecting targets sequentially in different edge maps is easier than segmenting all targets simultaneously in one busy edge map. The second phase is a new depth/motion-based segmentation/expansion that can accurately capture objects of different sizes. With motion information for decomposed edge layers ("motion-based region expansion"), it further differentiates the target objects from noises in other distance layers, thus helping to detect objects of different sizes or to identify moving objects.

The algorithm successfully increases the accuracy and reliability of object segmentation and motion detection under the impact of heavy background noise. The algorithm can offer precise segmentation in detecting multiple objects of different sizes and non-rigid targets, such as pedestrians. The performance is satisfying and robust while computational load is low. This algorithm not only improves the performance of static image segmentation, but also sets up a good basis for further information tracking in video sequences. It shows that fusing stereo-vision and motion-vision algorithm helps to achieve high accuracy and reliability under the impact of heavy background noise.



(a) (b) (c)

Fig. 35: (a) Highway environment interpretation. (b) Segmentation Result for Highway Environment. (c) Segmentation Result for Urban Driving Environment.

Superconducting Bandpass Delta-Sigma A/D Converter

Personnel

J. F. Bulzacchelli (H.-S. Lee and M. B. Ketchen — IBM)

Sponsorship

Center for Integrated Circuits and Systems (CICS)

The direct digitization of RF signals in the GHz range is a challenging application for any circuit technology. Traditionally, flash A/D converters have been used to digitize signal frequencies above 1 GHz, but their resolution and linearity are inadequate for most radio systems which must handle signals with a large dynamic range. Semiconductor bandpass delta-sigma modulators are used to digitize IF signals with high resolution, but their performance at microwave frequencies is limited by the speed of semiconductor comparators and the low Q of integrated inductors.

In this program, we present the design and testing of a superconducting bandpass delta-sigma modulator for direct A/D conversion of GHz RF signals. The schematic of the circuit is shown in Figure 36. The input signal is capacitively coupled to one end of a superconducting microstrip transmission line which serves as a high quality resonator (loaded Q > 5000). The current flowing out of the other end of the microstrip line is quantized by a clocked comparator comprising two Josephson junctions. If the current is above threshold, the lower junction switches and produces a quantized voltage pulse known as a Single Flux Quantum (SFQ) pulse. If the current is below threshold, the upper junction switches instead. The pattern of voltage pulses generated across the lower Josephson junction represents the digital output code of the delta-sigma modulator. These voltage pulses also inject current back into the microstrip line, providing the necessary "feedback" signal to the resonator. At the quarter-wave resonance of the microstrip line (about 2 GHz in our design), the resonator shunts the lower junction with a very low impedance; the "feedback" current to the resonator is maximized, and the quantization noise is minimized. Because of the high speed of Josephson junctions and the simplicity of the modulator circuit, the maximum sampling rate exceeds 40 GHz.

While such a high sampling rate improves the performance of the delta-sigma modulator, the challenges of high speed testing in a cryogenic environment are formidable. Even in the best cryogenic sample holders, the long cables used to connect the superconducting chip to room-temperature electronics have significant losses at frequencies above 10 GHz. Experimentally, we found two solutions for clocking the circuit at high frequencies. In the first approach (detailed in previous reports), we employ an optoelectronic clocking technique in which picosecond optical pulses at a 20.6 GHz repetition rate are delivered (via optical fiber) to an on-chip photodetector, the current pulses from which drive a Josephson clock amplifier. In the second approach, the modulator is triggered by an on-chip clock source. An increase in bias current turns the Josephson clock amplifier into an oscillator tunable between 20 and 45 GHz. We found that surprisingly good frequency stability could be achieved with the on-chip clock source with careful adjustment of dc bias currents.

Since the modulator output data rate exceeds the capacity of the interface to room-temperature test equipment, on-chip processing of the data is used to reduce the bandwidth requirements for readout. As explained in the 1998 MTL report, two segments of the modulator's bit stream are captured with a pair of 128-bit shift registers. The number of clock cycles skipped between acquiring the two segments is set by an on-chip programmable counter (from 0 to over 8000). Cross-correlation of the two captured segments is used to provide estimates of the autocorrelation function R[n] of the modulator output, from n=0 up to a large value, such as n=8000. Fourier transformation of R[n] then yields a power spectrum with frequency resolution comparable to an 8K FFT of the original bit stream.

Figure 37 shows the block diagram of the modulator test chip. As mentioned above, the bandpass modulator can be clocked either externally by a 20.6 GHz optical source or internally by an on-chip Josephson oscillator. A 1:4 demultiplexer converts the single-bit output of the modulator to 4-bit words at one-fourth the sampling rate. This allows most of the test chip, including the programmable counter and the

continued

shift register memory banks, to operate at a reduced clock rate with larger timing margins. Because of the 1:4 demultiplexing, 128-bit memory banks A and B are organized as 4 parallel rows of 32-bit long shift registers. As just discussed, the number of clock cycles skipped between loading the A and B memory banks is set by a programmable counter which is programmed by external control currents. Once the shift registers have been loaded, a readout controller unloads the stored bits and transfers them to "high-voltage" drivers which amplify the output signals up to about 2 mV, which is large enough to be detected by room-temperature electronics. The test chip employs over 4000 Josephson junctions and represents one of the most complex circuits ever designed in this technology.

The test chip was fabricated at HYPRES, Inc. While the chip has been used with the 20.6 GHz optical clock, higher oversampling ratios and SNRs are attained with the on-chip clock source operating near 40 GHz. In the initial experiments, the programmable counter on the test chip was programmed so that the shift registers captured 256 consecutive bits from the modulator, so that 256-point FFTs could be calculated. The output spectra of the modulator at a sampling rate of 42.6 GHz is plotted in Figure 38. The width (about 500 MHz) of the input tone at 1.7 GHz reflects the low frequency resolution of the 256-point FFTs. The Full-Scale (FS) input sensitivity is -17.4 dBm (30 mV rms). Quantization noise is suppressed at 2.23 GHz and at higher frequencies corresponding to higher-order microstrip modes. The SNR (49 dB over a 20.8 MHz bandwidth) is limited by the frequency resolution of the measurements, but still exceeds the SNRs of semiconductor modulators with comparable center frequencies. Other measurements, based on the correlation technique discussed above, show that the in-band noise over a 19.6 MHz bandwidth is -57 dBFS. The center frequency and sampling rate of the experimental modulator are the highest reported to date for a bandpass delta-sigma modulator in any technology.

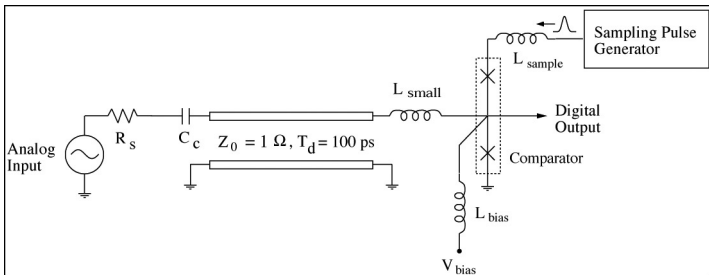


Fig. 36

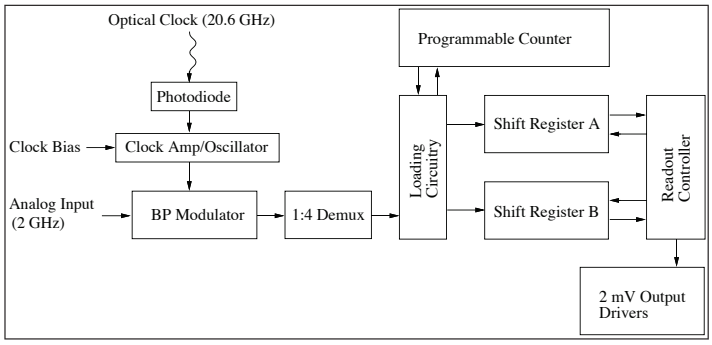


Fig. 37

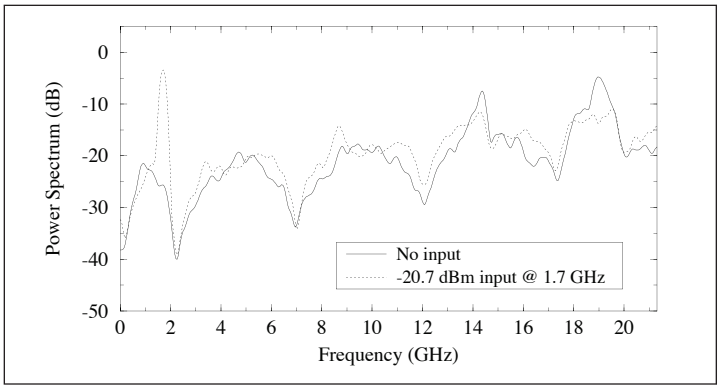


Fig. 38

Circuit and System Level Tools for Thermo-Aware Reliability Assessments of IC Designs

Personnel

S. M. Alam (D. E. Troxel, K.E. Goodson, and C.V. Thompson)

Sponsorship

MARCO Focused Research Center on Interconnect (MARCO/DARPA)

Integrated circuits are often designed using simple and conservative 'design rules' to ensure that the resulting circuits will meet reliability goals. This simplicity and conservatism leads to reduced performance for a given circuit and metallization technology. To address this problem, we had developed a TCAD tool, ERNI, which allows process-sensitive and layout-specific reliability estimates for fully laid out or partially laid out integrated circuits (Y. Chery and S. Hau-Riege) (See Figure 39).

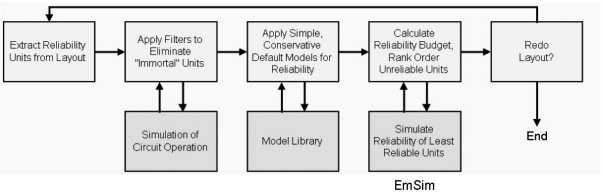


Fig. 39: A flowchart for a full hierarchical circuit-level reliability assessment, the basis for the prototype tool ERNI.

Circuit-level reliability analyses require reliability assessment of a large number of sometimes complexly connected interconnect trees. We have shown through modeling and experiments that the resistance saturation observed in straight via-to-via lines, which can lead to immunity from electromigration-induced failure, also occurs in more complex interconnect trees. We have also shown that trees will be 'immortal' if their effective current-density line-length product, $(jL)_{eff}$, is below a critical value. The jL product that defines immortality can be determined from experimental characterization or simulation of the reliability of straight via-to-via lines. Simple tests for tree immortality can be used in a hierarchical way to eliminate trees from further more computationally intensive reliability assessments. After filtering of immortal trees, the reliability of mortal trees must be assessed. This can be done through reliability simulations with individual trees, but this computationally intensive method should be reserved for the most problematic trees, those with the least reliability, and which are least convenient to 'fix' through layout modifications. We have suggested computationally simple and conservative 'default' models for assessment of tree reliabilities based on the Korhonen analysis and have tested models and simulations through experiments on simple interconnect trees.

Recent development in semiconductor processing technology has enabled the fabrication of a single integrated circuit with multiple device-interconnect layers or wafers stacked on each other. This approach is commonly referred to as the Three-Dimensional or 3D integration of ICs. Although there has been some research on the impact of 3D integration on chip size, interconnect delay, and overall system performance, the reliability issues in the 3D interconnect arrays are fairly unknown. We have extended the reliability concepts in ERNI and developed a framework for reliability analysis in 3D circuits with a novel Reliability Computer Aided Design (RCAD) tool, ERNI-3D. Using ERNI-3D, circuit designers can get interactive feedback on the reliability of their circuits associated with electromigration, 3D bonding, and joule heating.

As the 3D integration technology is not yet widespread, and no CAD tool supports IC layouts for such a technology, we first developed a comprehensive 3D circuit layout methodology, the circuit on each wafer or device interconnect layer can be laid out separately with inter-wafer via information embedded in the layout. The inter-wafer via information is generalized into three categories sufficient for defining all types of interconnection between wafers in a 3D stack (See Figure 40). A strategy for layout-file management that incorporates the orientation of each wafer in the bonding process is also proposed. We have implemented the layout methodology in 3D-MAGIC, an extension of MAGIC originally developed at UC Berkeley and widely used in academia. The test circuits designed with 3D-MAGIC are a 3D 8-bit adder and an 8-bit encryption processor mapped into a 3D FPGA.

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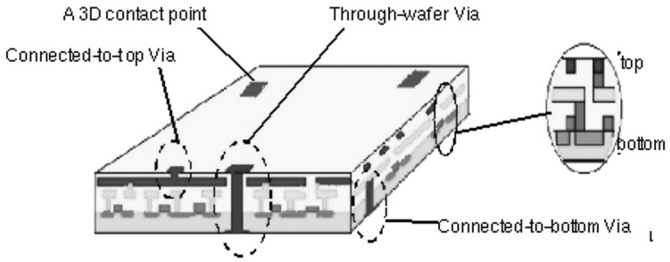


Fig. 40: Different types of via/contact for 3D ICs.

The reliability CAD tool, ERNI-3D, parses 3D circuit layouts and extracts both conventional and 3D interconnect trees. It employs the Hierarchical Reliability Analysis approach, and filters out a group of immortal trees using their current-density length products. After the filtering process, the stringent reliability models are applied to the remaining interconnect trees to compute their median and mean time to failures. Finally, all the different time to failures are combined using a joint probability distribution to report a single reliability figure for the whole chip. This initial version of ERNI-3D treats 3D circuits with two wafers or device-interconnect layers in the stack. However, the data-structures and algorithms in the tool are generic enough to make it compatible with 3D circuits with more than two device-interconnect layers and to allow the incorporation of more sophisticated reliability models in the future.

As high temperature rise poses as a major challenge in stacked 3D ICs, we are currently working on circuit and system layout for thermal management and its impact on reliability. ERNI-3D provides an infrastructure for such development. A novel feature of this activity is the capability to guide optimal placement of microfluidic *thermal connects* (see Figure 41) at the layout-level. As a demonstration vehicle, we are focusing on structures of the type shown in the figure, in which device layers are bonded face-to-face (high density interconnects) and micromachined wafers are bonded back-to-back (low density through-wafer vias) to create channels for fluidic thermal connects. One of the key concepts is that while 3D stacked systems produce a heat generation problem, they also provide four more surfaces to use for heat extraction (or two pairs of surfaces for flow-through heat extraction).

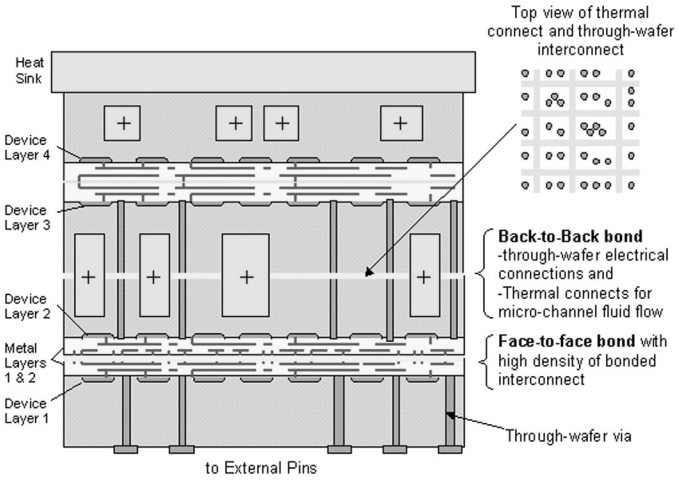


Fig. 41: Thermal management in a 3D IC. Here the 3D IC is a 4-wafer bonded stack.

Intelligent Transportation Systems

Personnel

J. F. Coughlin, B. K. P. Horn, J. K. Kucher, T. B. Sheridan, C. G. Sodini, and J. M. Sussman

Sponsorship

Intelligent Transportation Research Center at MIT's MTL

Transportation is important not only economically but also socially. The inter-state highway project built a sound infrastructure for our society. US citizens are spending, on average, about $1,000 per year on cars, trucks, and roads. What infrastructure do we need for tomorrow? The goal of this project is to develop a technical foundation for tomorrow's transportation systems. Currently we have a number of infrastructures which are independent from each other; examples include infrastructures for transportation, communication, finance, health care, emergency care, and others. In the next generation, these independent infrastructures will be integrated more closely with advanced information technologies. For example, highway tolls can be charged to drivers' bank accounts automatically with electronic toll gates connected to banks' computers. If a car accident occurs, as another example, the accident can be detected by an air-bag sensor and reported automatically through wireless network to ambulance stations. The ambulance and hospital will have a teleconference on the way from the scene to the hospital for rapid medical intervention.

For transportation, safety is very important. We are working on technologies which compensate for the diverse characteristic changes caused by aging, in collaboration with MIT's age laboratory. A typical 50-year-old driver, for example, needs twice as much light to see as a typical 30-year-old driver, and we are developing a pedestrian detection system based on infrared images to make night driving safer.

The Intelligent Transportation Systems project consists of various research topics ranging from small-scale systems to large-scale systems as well as fundamental to application oriented subprojects. An example of small-scale subprojects is an adaptive dynamic range image acquisition chip. Medium-scale systems include a personal-computer-based real-time three-dimensional machine vision system, sensor fusion systems, and an image recognition system for compressed three-dimensional images without decompression. Examples of large-scale systems are an image sensor network and the safety analysis of a fully-automated transportation system.

The research is being carried out at the Intelligent Transportation Research Center in MIT's Microsystems Technology Laboratories. The center is being sponsored by several member companies.

The Low-Power Bionic Ear Project (ICS)

Personnel
M. Baker, C. Salthouse, J.J. Sit, and S. Zhak (R. Sarpeshkar)

Sponsorship
Advanced Bionics Corporation

The aim of the project is to construct a cochlear-implant processor for the deaf that has the potential to reduce the current power consumption of such processors by more than an order of magnitude via low power analog VLSI processing. In addition, a cochlear implant processor that is based on the architecture of a silicon cochlea, i.e., on an analog electronic model of the inner ear, is being explored for its potential to revolutionize patient's speech recognition in noise (Rahul Sarpeshkar, Lorenzo Turicchia, George Efthivoulidis, and Luc Van Immerseel, "The Silicon Cochlea: From Biology to Bionics", accepted paper, Proceedings of The Biophysics of the Cochlea: Molecules to Models Conference, Titisee, Black Forest, Germany, July 27-August 1, 2002.)

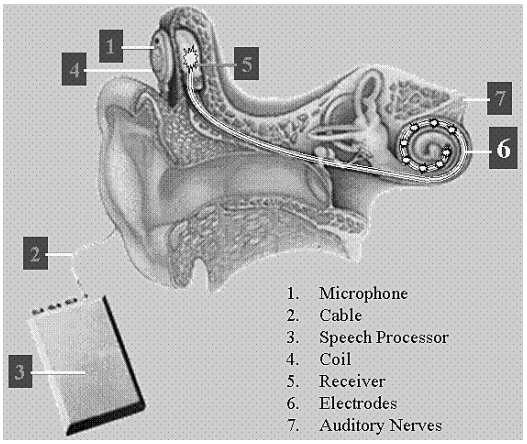


Fig. 42

Figure 42 shows the overall system architecture of a current bionic ear system (cochlear implant system). Sound that is transduced from a microphone is eventually converted into electrode stimulation in surgically implanted electrodes. The aim of this project is to reduce the power consumption to levels that will enable fully implanted systems to become a reality.

Several building block circuits for such a processor including a 100uW analog front end, a programmable bandpass filter, and a logarithmic map circuit were designed. Figure 43 shows a chip photograph of a DAC programmable fourth-order programmable bandpass filter that operates on 6uW of power consumption with over 60dB of dynamic range on a 2.8V supply (Christopher Salthouse and Rahul Sarpeshkar, "A Micropower Bandpass Filter for Use in Cochlear Implants", accepted paper, IEEE International Symposium on Circuits and Systems, Arizona, May 2002.)

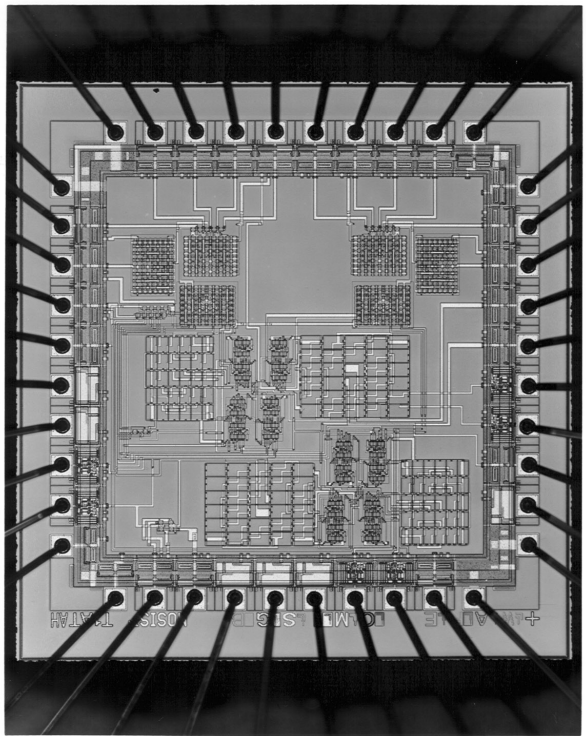


Fig. 43

The Visual Motion and Inertial Motion Sensing Project

Personnel
M.Tavakoli-Dastjerdi (R. Sarpeshkar)

Sponsorship
Caltech Subcontract of DARPA Funding

This project maps the distributed feedback loops of biological photoreceptors to silicon to create low-power high-performance silicon photoreceptors. Such photoreceptors are useful as front ends in VLSI motion sensors; important in robotic and active-vision applications. An ultra-low-noise MEMS vibration sensor, which provides inertial information to a vibrating visual sensor being built by collaborators at Caltech, has also been built.

Figure 44 shows the VLSI layout of a visual motion sensor that yields the speed and direction of a globally moving visual image along the "Y" direction. The array contains both photodiodes and analog VLSI processing circuitry that is inspired by similar circuitry in the housefly. Figure 45 shows the experimental setup for testing a capacitive MEMS vibration sensor with associated ultra low noise offset-compensating electronics on an electronics die which is wirebonded to the MEMS die. The sensor achieved an electronic noise floor equivalent to 30ug/rt(Hz) over a 1Hz-100Hz bandwidth, a specification that appears to be 3 times better than any equivalent commercial or research system in spite of its separate-die solution for mechanical and electrical systems. The system was able to detect a change of 1 part per 5 million in capacitance. The offset-compensating electronics has been briefly described in "A Low-Noise Nonlinear Feedback Technique for Compensating Offset in Analog Multipliers", Maziar Tavakoli-Dastjerdi and Rahul Sarpeshkar, accepted paper, IEEE International Symposium on Circuits and Systems, Arizona, May 2002.

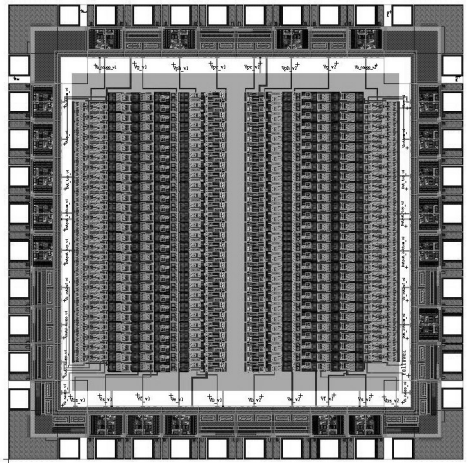


Fig. 44

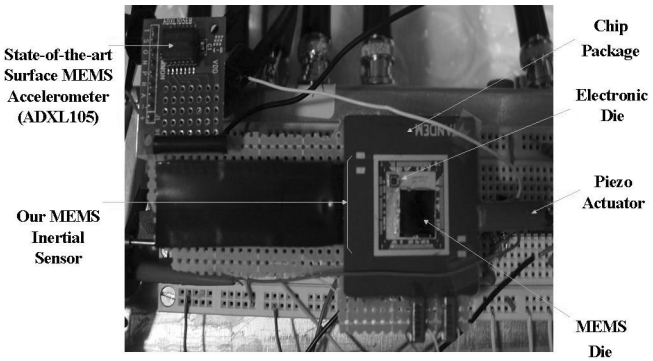


Fig. 45

Spike-Based Hybrid Computers Project

Personnel
M. O'Halloran, A. Mevay, H. Yang, R. Sarpeshkar

Sponsorship
Office of Naval Research

This project attempts to combine the best of analog and digital computation to compute more efficiently than would be possible in either paradigm of computation. (Rahul Sarpeshkar and Micah O'Halloran, "Scalable Hybrid Computation with Spikes", in press, Neural Computation, 2002). This project is inspired by the duality of analog spike-time and digital spike-count codes of the brain's neurons. It is being applied to create low-power time-based analog-to-digital converters, analog memories, and novel event-based control architectures. Several design issues that are important in mixed-signal systems including good power supply rejection are being explored.

Figure 46 shows the layout of a low power analog-to-digital converter that uses time as a signal variable rather than the traditional variables of voltage or current to perform quantization. A technique for achieving good power supply rejection without sacrificing the gain bandwidth product of an amplifier has been reported (Micah O'Halloran and Rahul Sarpeshkar, "A Low Open-Loop Gain High-PSRR Micropower CMOS Amplifier for Mixed-Signal Applications", paper, IEEE International Symposium on Circuits and Systems, Arizona, May 2002).

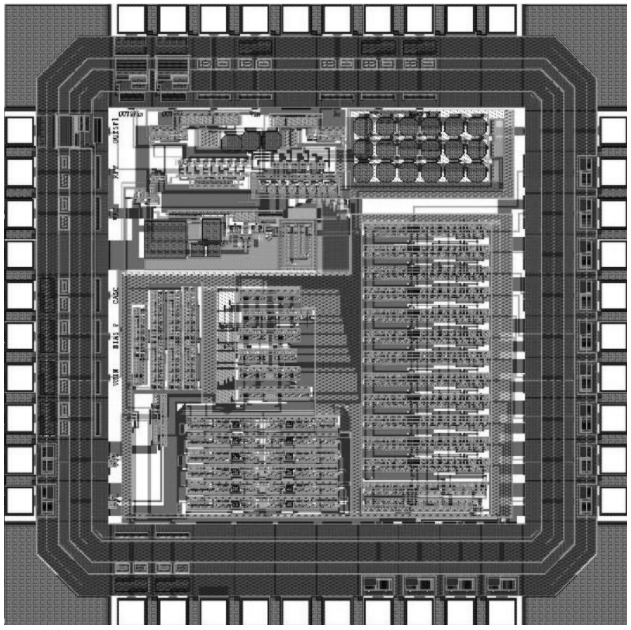


Fig. 46

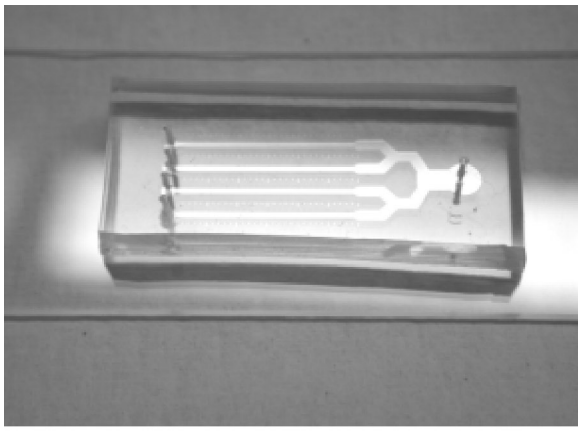
Opposite page:

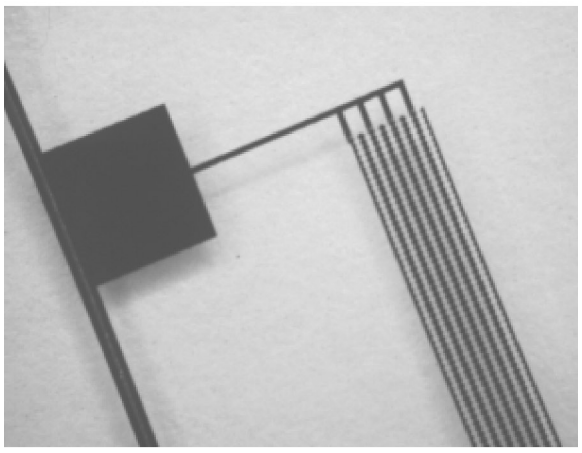
(Top) Microfluidic cell-adhesion assay device that is fabricated using rapid prototyping techniques; (Middle) Cell electroporation lysis device that contains arrays of electrodes; (Bottom) Organelle sorting device that uses miniaturized isoelectric focusing field flow fractionation technique.

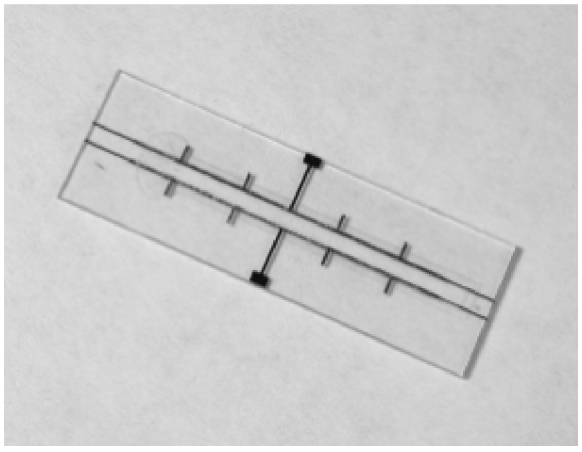
Courtesy of H. Lu, S. Gaudet, L. Koo, P. Sorger, D. Lauffenburger, and L. Griffith (K. Jensen and M. Schmidt)

Sponsor:
DARPA Bio-Info-Micro

Microelectromechanical Devices







Microelectromechanical Devices

- *Microspectrometer Using Electrostatic or Piezoelectric Tunable Gratings*
- *Micromachined Structures for Microphotonics*
- *Electronic Detection of DNA by its Intrinsic Molecular Charge*
- *Development of Microfluidic Device for Study of Chemotaxis*
- *Integration of Heterogeneous Microfluidic Separation*
- *Platforms for Rapid Screening and Analysis of Biological and Chemical Processes*
- *Microfabricated Fluidic Devices for Cell Adhesion Assay, Cell Lysis, and Subcellular Component Separations*
- *Vapor Microbubbles for Cell Actuation*
- *Microfluidic Logic*
- *A Differential Microcantilever Stress Sensor for Biomolecular Detection*
- *Self Activated Microcantilever-based Gas Sensor*
- *Gas-Liquid Flow, Separation and Mass Transfer in MicroChemical Systems*
- *Microreactors for Catalyst Testing*
- *Scalable Multiphase Microchemical Systems for Direct Fluorination*
- *MicroChemical Systems for Separations*
- *Three Dimensional Integration of Microfluidic Devices*
- *Low Leakage Micro Switch Valves for Gas Chromatography*
- *Fuel Processing in Microfabricated Chemical System*
- *Microchemical Systems for Fuel Processing and Conversion to Electrical Power*
- *Piezoelectric Micro Power Generator (PMPG): A Novel MEMS Based Electrical Power Source*
- *Development of Hydrocarbon-Fueled Silicon Combustors for Micro Gas Turbine Engines*
- *Thermophotovoltaic Micro-Generators*
- *Micro-Fuel Cell*
- *Lateral RF MEMS Switch with PZT Actuation*
- *MEMS Tunable Capacitor and LC Tank*
- *DRIE-Fabricated Curved-Electrode Zipping Actuators with Low Pull-In Voltage*
- *MEMS Amplification of Piezoelectric Strain for In-Plane Actuation*
- *Water-Immersible Micromachined $Pb(ZrTi)O_3$ Thin Film Actuator*

continued

continued

Microelectromechanical Devices

- ***Wafer Bond Alignment and Strength Characterization***
- ***Microelectromechanical (MEMS) Thin Film Stress Sensors***
- ***3D Nanomanufacturing via Folding of 2D Membranes***
- ***Nano-Scale Machining with Femtosecond Laser Pulses***

Microspectrometer Using Electrostatic or Piezoelectric Tunable Gratings

Personnel
W.-C. Shih, C. Hidrovo, C. W. Wong, and Y.-B. Jeon (S.-G. Kim and G. Barbastathis)

Sponsorship
n/a

This project seeks to build a "true" miniature optical spectrometer utilizing analog tunable gratings. Miniaturization is desirable for portable devices and applications which parallel processing benefits. However, in optics there are two fundamental problems when systems are small: the decrease of numerical aperture and optical path length. The combination of these two problems degrades the resolution of such a system. Existing technologies have tried to maintain performance through maximizing numerical aperture and optical path length under constraints miniaturization superimposes. However, we believe this is not the way if true miniaturization is desired. Instead we confront the aperture and path length deficiency issues and try to resolve them with the aid of computational imaging and optical diversity.

Computational imaging is widely used in the context of image processing for deblurring or restoration purposes. Since every image is formed through convolving a system function with the object, restoration is essentially the inverse process. The system function can be generated by motion blur, diffraction, or aberration, etc. If one can model the convolution process properly and use appropriate numerical algorithms, the result of the inverse problem may be better than the original image. For our case, the object is a spectral intensity distribution and the convolver is the Point Spread Function (PSF) of the system. Optical diversity is essentially a method which allows us to change the system transfer function at minimal cost, in our case, actuation of the tunable grating. Various transfer functions not only increase the robustness of inversion by over-constraining the system, but also give us adaptive spectral resolution capability.

The electrostatic grating is shown in Figure 1. An SOI wafer with 25 μm thick device layer is etched with DRIE until the buried oxide is exposed. The buried oxide is removed successively with wet etching. The period of the grating is 12 μm, and the grating can be actuated by two comb-drives on both sides. The piezoelectric grating is shown in Figure 2. The grating structure is made of platinum and silicon nitride. The actuators are made of two platinum electrodes sandwiching the thin film PZT.

We set up a grating monochromator with the tunable grating. Due to the cross-leakage and unavoidable noise in the measurement, the system is ill-conditioned. There are many methods to resolve this such as Wiener filtering and maximal-likelihood. We used Tikhonov regularization with positivity constraint to extract the real spectrum out of the "blurred" spectrum due to miniaturization. The real spectrum and the recovered spectrum are shown in Figure 3. Optical diversity utilizes the fact that the grating is tunable, and we can change the system transfer function upon actuation. Figure 4 shows an Improved recovered spectrum using Computational Imaging with Optical Diversity (ICIOD).

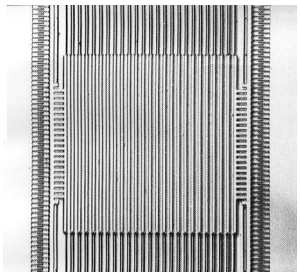


Fig. 1: Electrostatic grating.

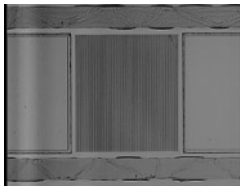


Fig. 2: Piezoelectric grating.

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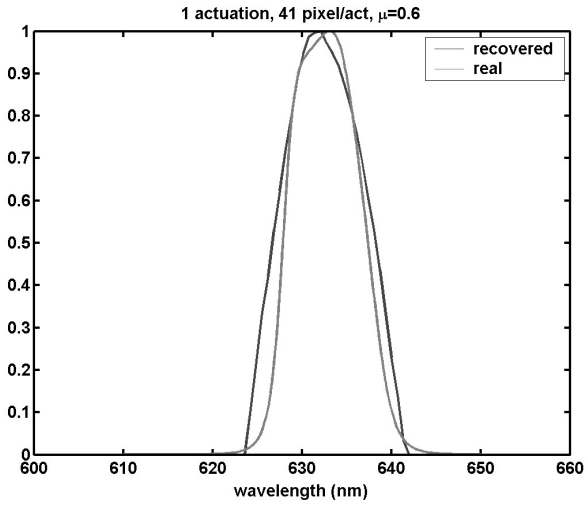

Fig. 3: Spectrum recovered using deconvolution VS real spectrum of an interference filter.

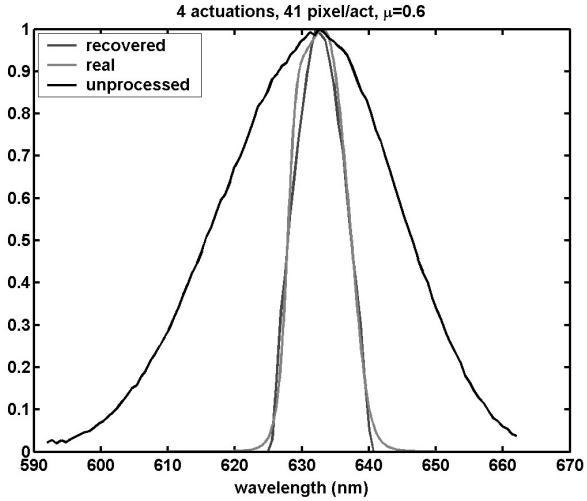

Fig. 4: Spectrum recovered using ICIOD VS real spectrum of an interference filter.

Micromachined Structures for Microphotonics

Personnel
D. Seneviratne and Y. Avrahami (H.L. Tuller), with M. Watts, H. Haus, and G. Nielson (G. Barbastathis)

Sponsorship
Multidisciplinary program supported by Pirelli and administered by the Microphotonics Center

Binary-switchable and dynamically-tunable micromachined structures are being designed and fabricated to operate in conjunction with optical resonators and photonic band gap structures to achieve optical switching, multiplexing/de-multiplexing, and wavelength add-drops in Si integrated photonic systems. The work is being performed in conjunction with a multidisciplinary group that is working on the integration of microphotonic devices onto silicon wafers. Novel, multi-functional, optical material systems that can be readily integrated with Si platforms are also being investigated.

Electronic Detection of DNA by its Intrinsic Molecular Charge

Personnel
E. Cooper and J. Fritz (S. Manalis)

Sponsorship
DARPA Bio-Info-Micro and AFOSR

A wide range of techniques for detecting nucleic acids is based on their hybridization to DNA probes on a solid surface. In the methods used most routinely, the physical nature of the readout requires the attachment of reporter molecules such as fluorescent, chemiluminescent, redox or radioactive labels. Although label-dependent methods achieve the highest sensitivities, eliminating the labeling steps has the advantage of simplifying the readout and increasing the speed and ease of nucleic acid assays. This is especially desirable for characterizing infectious agents, scoring sequence polymorphisms and genotypes, and measuring mRNA levels during expression profiling. The development of label-independent methods that can monitor hybridization in real-time and that are simple and scalable is still in its infancy.

We have demonstrated the selective and real-time detection of label-free DNA using an electronic readout (*Fritz et al. PNAS 2002*). Microfabricated silicon field-effect sensors were used to directly monitor the increase in surface charge when DNA hybridizes on the sensor surface (See Figure 5). The electrostatic immobilization of probe DNA on a positively charged poly-L-lysine layer enables rapid hybridization at low ionic strength where field-effect sensing is most sensitive. Nanomolar DNA concentrations can be detected within minutes, and a single base mismatch within 12mer oligonucleotides can be distinguished by using a differential detection technique with two sensors in parallel (See Figure 6). The sensors were fabricated at the MTL and show promise for future electronic DNA arrays and rapid characterization of nucleic acid samples. This approach demonstrates the most direct and simplest translation of genetic information to microelectronics.

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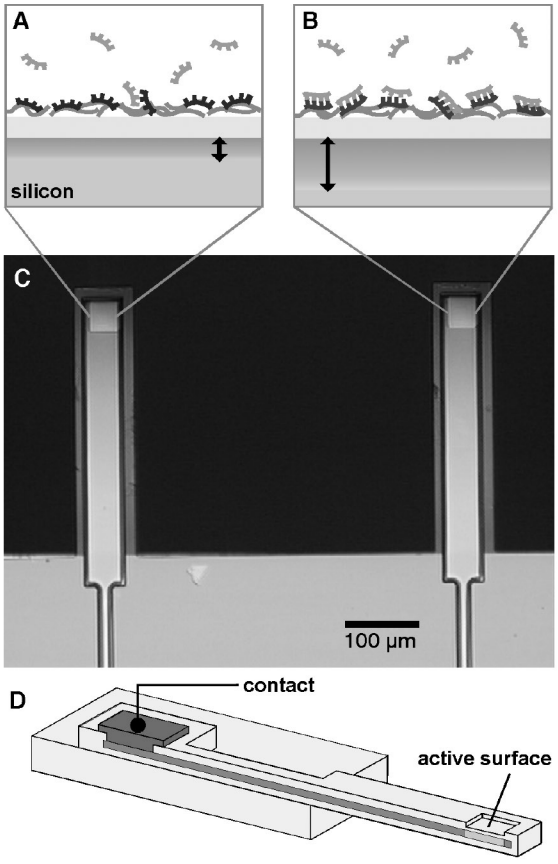

Fig. 5: (a) and (b) Electrolyte - insulator - silicon interface of a n-type field-effect sensor. DNA exhibits one intrinsic negative charge per base at its sugar-phosphate backbone. Probe DNA is electrostatically bound to a layer of PLL on the surface. (a) Binding of negatively charged target DNA to its complementary probe DNA at the sensor surface extends the depletion region (black arrow) in the silicon portion of the sensor compared to (b) where no binding occurs to non-complementary probe DNA (blue). (c) Optical image of a device consisting of field-effect sensors at the terminus of two cantilevers. The cantilevers are 500 µm long, 75 µm wide and 3 µm thick. (d) Cross section of a cantilever field-effect sensor. The sensing area at the terminus of the cantilever is electrically connected to a metal contact on the substrate by a layer of highly doped silicon inside the cantilever.

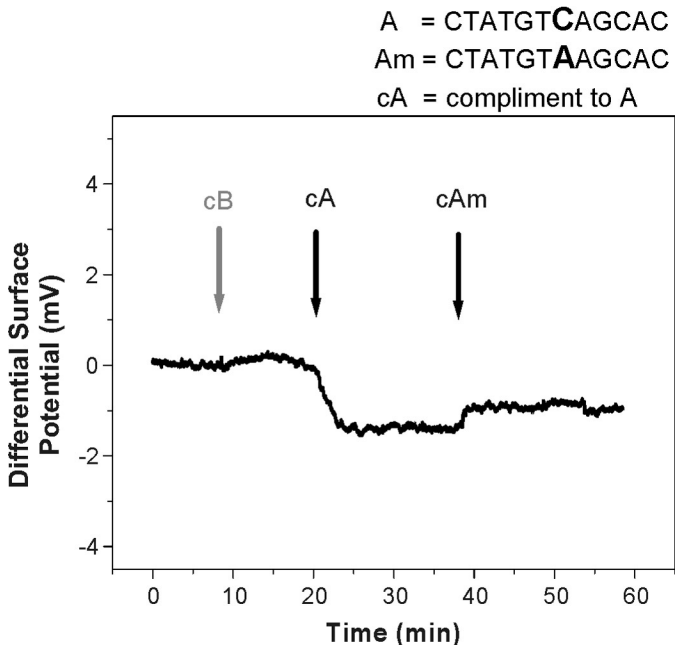

Fig. 6: Differential surface potential from two sensors which were functionalized with probe oligonucleotides A and Am which differ only in a single base. Control solutions with non-complementary target oligonucleotide cB show no differential signal, while injection of 80 nM of complementary sequences cA and cAm both show a distinctive hybridization signal.

Development of Microfluidic Device for Study of Chemotaxis

Personnel
M. Shur (C. F. Dewey)

Sponsorship
DARPA

Cells exhibit a highly complex and integrated response to chemical gradients that requires quantitative explanation. Several theoretical models of a cell's ability to sense a gradient have been formulated. However, the inability to produce a linear gradient of chemoattractant and maintain it at steady state has prevented researchers from obtaining reproducible, quantitative results and validating the models.

Currently, the Dunn chamber assay is widely used for studying chemotaxis. In order to study slow-moving cells such as fibroblasts, a gradient must be maintained at steady state for four or more hours, which is impossible to do in the static Dunn chamber.

The multilayer application of soft lithography allows for peristaltic pumping and valving modules to be built into the device (See Figure 7). The overall goal is to manufacture a device on a chip with integrated modules for pumping fluids and cells, mixing various concentrations of reagents, placing cells in designated areas, and controlling chamber temperature to provide a viable environment for the cells. Ultimately, the chemotaxis chamber will be a universal "lab on a chip" that can be used to study different types of cells on various substrates and to probe potential chemoattractants at a range of concentrations.

The geometry of the current design allows for several experiments to be run simultaneously. The diverging flows of chemoattractant and buffer allow for several discrete gradients to be established.

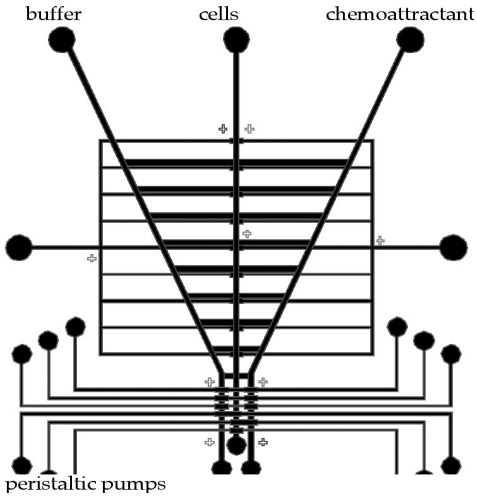

Fig. 7: Two layer mask for the chemotaxis chamber containing valves and peristaltic pumps.

Integration of Heterogeneous Microfluidic Separation

Personnel
Y. C. Wang and M. H. Choi (J. Han)

Sponsorship
DARPA

One of the most important separation methods in the field of proteomics is 2-D protein electrophoresis separation. It is the only method to separate over 1,800 proteins in a single run with satisfying reproducibility now. The first dimension separation is IsoElectric Focusing (IEF) which can focus proteins into different groups by their pI values. Then, Sodium Dodecyl sulfate polyacrylamide gel electrophoresis (SDS-PAGE) is performed to separate these protein groups by their molecular weight.

Our goal here is to build an on-chip multidimensional separation system for separation of biomolecules, especially proteins. We have developed IEF and SDS-PAGE techniques on a microfluidic chip format. Miniaturization of these techniques allows us to perform these processes in very short microchannels (several millimeters or less) within a minute, which is an order of magnitude improvement in speed. The methods and chip architecture for these separations have been selected specifically for the eventual goal of their integration to two-dimensional 2D protein separation. IEF of proteins was achieved with commercially available ampholyte in a microchannel (1cm or shorter), fabricated on either poly(dimethylsiloxane) (PDMS) or glass substrates. Several naturally fluorescent and labeled proteins were analyzed with this technique (See Figure 8). We also demonstrated SDS-PAGE in a chip by photopolymerizing and photopatterning polyacrylamide gel in a microchannel. A protein marker sample (20.1 ~ 205 kDa) was analyzed, and the peak movement was monitored by video microscopy (See Figure 9).

Miniaturizing the length of separation channel in IEF and SDS-PAGE techniques leads to a number of improvements over their conventional counterparts. 1) Separation of protein peaks could be achieved very quickly, typically within 30s. 2) The electric potential to be applied across the channel was greatly decreased, which is another engineering constraint in future integrated systems. 3) Instead of mobilizing or eluting focused peaks, a microscope optic could be used for imaging of the channel in real time for a faster analysis. These advantages can be exploited for constructing future microfluidic 2-D protein separation systems, which is highly desirable for proteomics research.

Our next goal in this project is to develop technologies to combine these heterogeneous separation systems, and to solve any issues arising from such integration. The success of this project could lead to a generic solution for other integrated microfluidic systems for (bio)molecule analysis, where several fluidic components should be interfaced without compromising the function of each components.

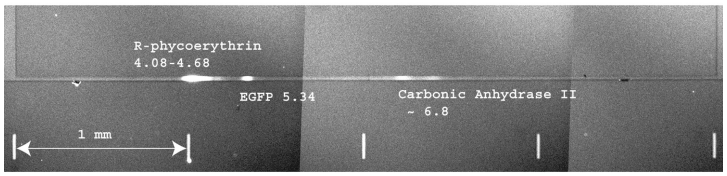

Fig. 8: Isoelectric focusing in 4mm channel. Electric field was 35.7 V/cm. Carbonic anhydras.e II was labeled by cysteine-specific labeling (rhodamine-maleimide), while R-phycoerythrin and EGFP are naturally fluorescent. The focusing was achieved within 30 s after applying the electric field. Wider channel regions at both ends are filled with catholyte and anolyte, respectively, and pH gradient was established within 4mm channel.

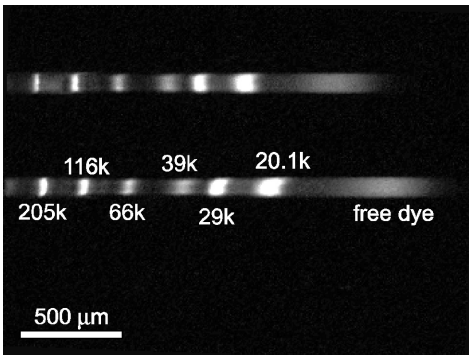

Fig. 9: SDS-PAGE separation of six proteins in 12% gel (acrylamide : bis-acrylamide = 37.5: 1), also containing 0.1% SDS and 0.2% photoinitiator. The gel buffer was 0.375M Tris-Cl (pH=8.6). The rightmost peak in the channel is due to the Bromophenol blue dye added to the sample. The width of dye band is much larger than other protein bands, suggesting no stacking effect for small dye molecules.

Platforms for Rapid Screening and Analysis of Biological and Chemical Processes

Personnel

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(K. F. Jensen, P.E. Laibinis, R.J. Ram, M.A. Schmidt, and A.J. Sinskey)

Sponsorship

DuPont MIT Alliance

This is a multidisciplinary research program aimed at developing new platforms for bioprocess discovery and development, specifically banks of miniaturized, automated bioreactors, each with integrated bioanalytical devices, and all operating in parallel (see Figure 10). Such systems will address the continuing demand in bioprocess science and engineering for fast and accurate analytical information that can be used to rapidly evaluate the interactions between biological systems and bioprocess operations. Moreover, the microbioreactors will provide the platforms for efficiently incorporating modern tools of biology (genetics, enzymology, bioinformatics) to improve bioprocess screening and development. Applying microfabrication technology to bioprocess development should result in rapid screening of strains and metabolic pathways as well as speed up of transfer of cell cultures in production. In order to realize the microfermentors, we are addressing the following critical issues: (i) design and fabrication strategies for microfermentors; (ii) integration of novel optical sensors; (iii) sensitivity of the analytical devices; (iv) biocompatibility of the materials; (v) appropriate biological systems for evaluating performance of the microfermentors; and (vi) benchmarking of microfermentation against traditional bioprocessing methodologies.

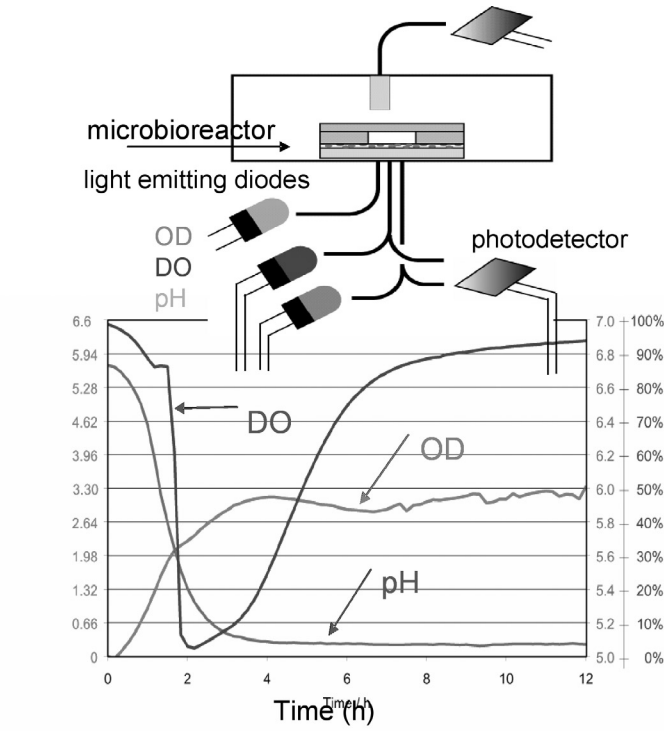

Fig. 10: (Top) Schematic of microbioreactor with optical, on-line monitoring of optical density (cell concentration), Dissolved Oxygen (DO), and pH. (Bottom) Example of data obtained with on-line sensors.

Microfabricated Fluidic Devices for Cell Adhesion Assay, Cell Lysis, and Subcellular Component Separations

Personnel

H. Lu, S. Gaudet, L. Koo, P. Sorger, D.Lauffenburger, and L. Griffith
(K. F. Jensen and M. A. Schmidt)

Sponsorship

DARPA Bio-Info-Micro

This project is part of the DARPA Bio-Info-Micro program at MIT aimed at understanding signal transduction pathways in cell decision processes, in particular apoptosis (programmed cell death) and cell-biomaterial interactions. We focus on the development of advanced micro-scale analytical devices for efficient analysis of small populations of cells, their subcellular components, and intracellular proteins of interests.

Cell adhesion is important in many fundamental biological phenomena and medical applications. We miniaturized a shear flow chamber to perform cell adhesion assays that probe the cell-substratum interactions. The advantages include much larger dynamic range of shear forces, ease of analysis, and small sample requirement (in terms of both cells and biomaterials). These devices were fabricated using rapid prototyping techniques and were demonstrated for both short-term and long-term cell culture, biochemical stimulation, and adhesion analysis.

In proteomics and signal transduction studies, the demand to identify the location and amount of proteins poses challenges to subcellular separation and sample preparations. Current technologies involve laborious and time-consuming procedures that require large sample volumes (>10^6 cells). For protein profiling, the organelle separation needs to be fast, parallel, and automated to match the great number of experiments needed. We developed microfluidic systems that handle small number of cells (~10^3), lyse them, and separate out the organelles of interest (See Figure 11). Cell lysis by electroporation is accomplished in a device containing multiple metal saw-tooth electrodes and flow channel. Alternating electric field and appropriate voltages are used to minimize water electrolysis and to maximize cross cell membrane potential while minimizing impact on the organelles. Once cells are lysed, organelles of interest, such as mitochondria and nuclei, are separated from the resulting lysate by isoelectric focusing in a microfabricated device containing parallel electrodes and fractionation collection channels. The performance of the device has been modeled to provide understanding of isoelectric focusing on the micron scale with particles that are amphoteric (such as organelles). Current research extends this method to more separations on the molecular level and the devices are used to address fundamental biological questions underlying signal transduction pathways.

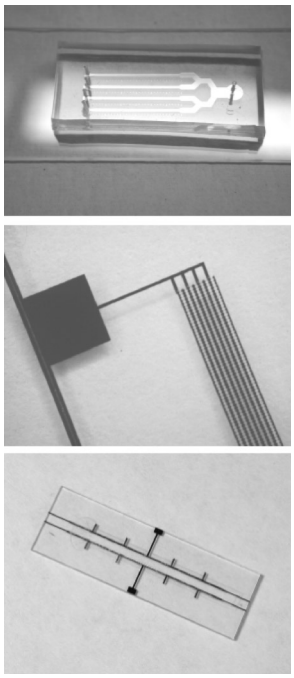

Fig. 11: (Top) Microfluidic cell-adhesion assay device that is fabricated using rapid prototyping techniques; (Middle) Cell electroporation lysis device that contains arrays of electrodes; (Bottom) Organelle sorting device that uses miniaturized isoelectric focusing field flow fractionation technique.

Vapor Microbubbles for Cell Actuation

Personnel
R.A. Braff and A.L. Gerhardt (M.L. Gray, M.A. Schmidt, and M. Toner)

Sponsorship
AfCS (Alliance for Cellular Signaling)

Microfluidics is becoming increasingly important to the success of a wide variety of micromachined devices, particularly those with biological applications. However, many obstacles still exist in the production of a robust and simple microfluidic device. One area that is in need of improvement is microfluidic actuators, valves, and pumps.

We are developing guidelines to use thermally formed microbubbles as a means of fluidic actuation. The use of microbubbles is attractive due to the simple fabrication and operation of such devices. However, prior work in this area was hindered by several issues inherent to vapor bubble formation that severely limited the reliability of bubble-based devices. We have shown that it is possible to control the location at which bubbles form, to control the size of the bubbles, to make formation temperature more repeatable and reduced, and to have bubbles that collapse completely in less than 10 seconds (See Figure 12).

The achievement of controllable microbubbles makes possible many microfluidic applications, one of which we have demonstrated. We have built a device that is capable of capturing, holding, and selectively releasing single bioparticles using microbubble actuation (See Figure 13). The next generation bioparticle actuator is in the development stages of being scaled into an array for the analysis of a large population of individual cells.

The arrayed bioparticle actuator features the ability to observe cells from both vertical positions, two cellular medium channels to facilitate experimental and control fluid flows simultaneously, facile four-cell observation in one microscope view, and a pogo-pin contact scheme for short chip replacement times between assays (See Figure 14).

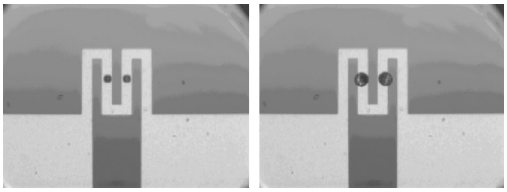

Fig. 12: A platinum heater with machined bubble nucleation sites, before and after bubble formation.

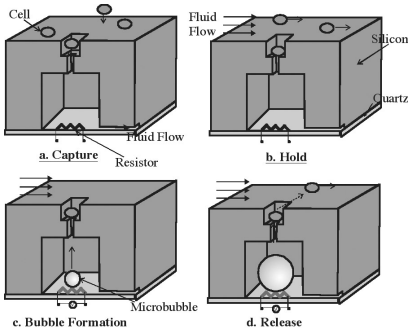

Fig. 13: Schematic of microbubble bioparticle actuator. (a) A small backflow draws particle into capture well. (b) A bulk flow sweeps uncaptured particles away. (c) The platinum heater is turned on, and a vapor bubble begins to form in the bubble chamber. (d) The volume expansion of the bubble creates a jet of fluid that releases the particle from the capture chamber and is entrained in the bulk flow.

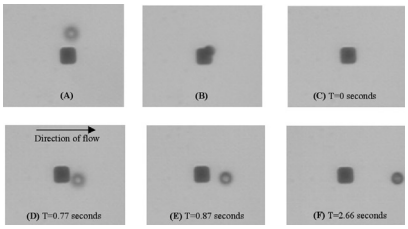

Fig. 14: Microbubble bioparticle actuator in operation. In (A) and (B), a 10μm polystyrene bead is drawn into the capture well where it is held against a bulk flow in (C). In (D), the bead is released by a jet created by a bubble in the chamber below. In (E) and (F), the bead is entrained in the bulk flow.

Microfluidic Logic

Personnel
T. Thorsen

Sponsorship
n/a

Advanced image analysis tools are used in the Thorsen group in Hatsopolous Microfluids Laboratory at M.I.T. to complement core research structured around addressable silicone microfluidic networks. Monolithic multilayer elastomeric devices, which use multiple thin polymer layers to create three-dimensional microfluidic networks, are an important platform from which simple valve and pump structures can be used to build complex dynamic microfluidic networks. These elastomeric devices have the advantage of low cost, rapid prototyping, scalability, and highly flexible design constraints.

We developed high-density microfluidic chips that contain plumbing networks with thousands of micromechanical valves and hundreds of individually addressable chambers (See Figure 15). These fluidic devices are analogous to electronic integrated circuits fabricated using Large Scale Integration (LSI). A key component of these networks is the fluidic multiplexor, which is a combinatorial array of binary valve patterns that exponentially increases the processing power of a network by allowing complex fluid manipulations with a minimal number of inputs.

The simple, modular fabrication technology has made the project an attractive platform for the Undergraduate Research Opportunities Program (UROP) as an educational tool providing the students with hands-on research experience in design, manufacture, and fluid mechanics.

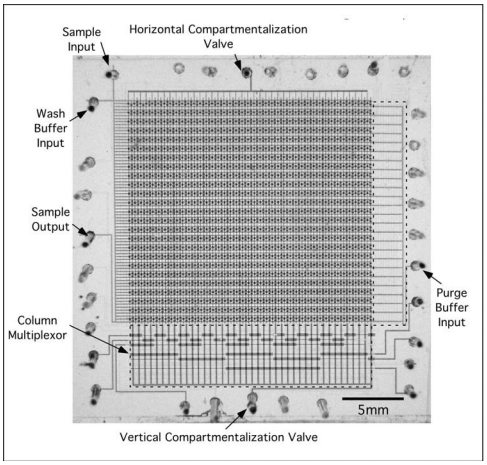

Fig. 15

A Differential Microcantilever Stress Sensor for Biomolecular Detection

Personnel
C. Savran and T. Burg (S. Manalis)

Sponsorship
DARPA Bio-Info-Micro, NSF Center for Bits and Atoms, and Media Lab TTT Consortium

Conventional procedures based on two-dimensional gel electrophoresis for profiling the concentrations of specific proteins and their byproducts are time-consuming, labor-intensive, and require significant technical expertise to obtain quantitative information. One approach for circumventing these limitations is to develop the equivalent of a DNA microarray for identifying proteins.

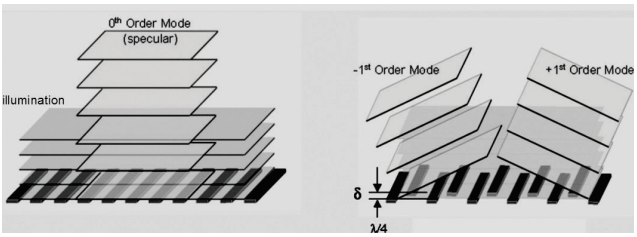

Fig. 16: Concept for measuring displacement with InterDigitated (ID) fingers. When the fingers are illuminated with a laser, the reflected light produces a diffraction pattern composed of several modes. The intensities of these modes depend on the relative out-of-plane distance between the ID finger sets.

Recently, Fritz et al. (*Science 2000*) demonstrated that a microcantilever with immobilized receptor molecules can translate the binding of the target protein to a mechanical bending of the cantilever. Although the physical origin of the stress-induced bending has not yet been elucidated, an investigation by Wu et al. (*PNAS 2001*) suggests that the bending results from a combination of steric crowding of the target molecules and the free energy change between the receptor and receptor – target complex.

We have developed a differential microcantilever stress sensor that translates the binding of molecules on the sensor surface into a mechanical displacement that modulates the intensity of visible light (*Savran et al., JMEMS 2002*). The shape of the cantilevers is defined such that when they bend, the fingers of one cantilever are vertically displaced relative to the interdigitated fingers on the other. When illuminated with coherent light, the fingers form a phase-sensitive diffraction grating, and the out-of-plane displacement is determined by measuring the intensity of a diffracted mode. The concept of modulating coherent light with a diffraction grating is shown in Figure 16 and the application of this concept to a differential pair of cantilevers fabricated at the MTL is shown in Figure 17.

The differential microcantilever offers two improvements over the conventional cantilevers used in previous experiments. First, the cantilever bending is measured by interferometry which is one of the most sensitive methods for measuring position. The power spectral density of the differential deflection (See Figure 18) reveals that the resolution is limited by the cantilever's thermomechanical noise of 0.008 Å/$Hz^{½}$ for frequencies above 40 Hz. Second, the design of the interferometer inherently measures the relative bending between two identical cantilevers. The relative, or differential, measurement is critical for eliminating unwanted signals resulting from changes in temperature, pH, ionic strength, and to some degree, nonspecific binding. Acquiring a differential measurement before the output of the detector is amplified can also improve the overall resolution by eliminating unwanted signals from background fluctuations and nonspecific binding. We are currently using the differential cantilever to detect the concentration of proteins that are difficult to detect via fluorescent labels.

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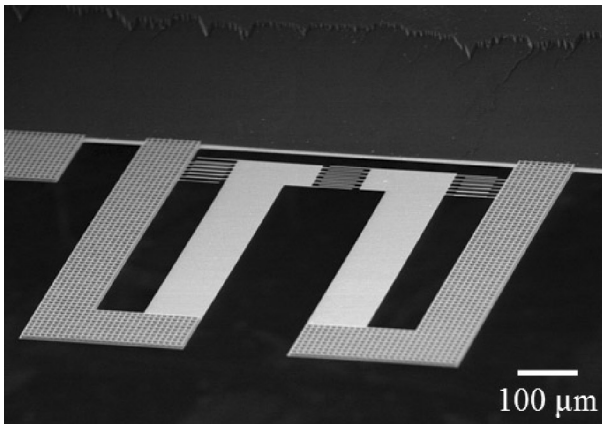

Fig. 17: Scanning electron micrograph of a differential microcantilever stress sensor.

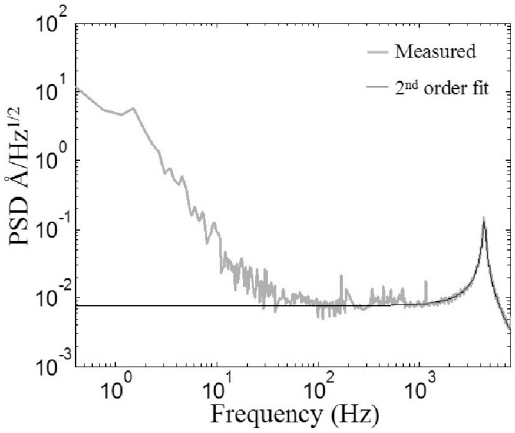

Fig. 18: Power Spectrum Density (PSD) of the differential cantilever deflection.

Self-Activated Microcantilever-based Gas Sensor

Personnel
Y.K. Min (H.L. Tuller)

Sponsorship
NSF and Daewoo Electronics Fellowship

We are studying a Self-Activated Microcantilever-based (SAM) gas sensor providing features useful in control devices. The SAM gas sensor has a Si-based micromachined structure with gas sensing and piezoelectric components. The influence of crystallinity, microstructure and deposition conditions on gas sensor response of sputtered ZnO thin films is under investigation. The sensor response to a number of gases is being investigated and modeled. Efforts to integrate sensor and actuator functions are being pursued.

Gas-Liquid Flow, Separation and Mass Transfer in MicroChemical Systems

Personnel

A. Guenther, M. Jhunjhunwala, T. Kraus, and N. de Mas
(M. A. Schmidt and K. F. Jensen)

Sponsorship

ARO MURI and MIT Microchemical Systems Technology Center

We characterize the dynamics of gas-liquid flow in microchannels and apply such information for a systematic design of gas-liquid microreactors with a significantly increased throughput. The inherently transient nature of gas–liquid flows in microchannels is represented in slug, wavy annular, and bubbly flow regimes. The design of multichannel gas-liquid systems with desired flow and mass transfer characteristics across tens to hundreds of reaction channels requires understanding of the underlying multiphase fluid flow phenomena. We use single, silicon-based channels with hydraulic diameters between 40 and 400 μm that are fabricated by deep reactive ion etching and coated with a 0.5 μm oxide layer. Pyrex is anodically bonded to the silicon, providing optical access for flow visualization. Characterization is done using fluorescence and confocal microscopy, and integrated concentration and flow regime sensors. Superficial gas and liquid velocities were varied between 0.01-10 m/s and 0.001-10 m/s, respectively.

Gas-liquid separation. Using a microfabricated capillary array, we are able to conduct a complete "on-chip" gas-liquid separation, Figure 19, that can be integrated into gas-liquid microreactors. Such a methodology did not exist previously, limiting the development and usefulness of microfluidic gas-liquid systems whenever good contacting and subsequent separation of gas and liquid streams was important or unavoidable. Our concept allows manipulation of any pattern, steady or transient, gas-liquid mixtures in microchannels, their reliable separation into individual phases at high velocities and for altering gas and liquid fractions. It allows the introduction of a gas/liquid stream into the flow channel and their contacting in any desired way and separation into individual streams, in precise amounts and at well defined locations along the flow path. With alternate methods, this is presently only possible for steady liquid-only systems or for steady and segregated gas-liquid flows.

Mixing. Mixing on microscale has previously been done either by focusing the streams or by patterning the channels. Both require additional features or fabrication steps. Figure 19 shows fluorescence micrographs illustrating the effect an inert gas phase has on an otherwise quiescent, laminar co-flow of two differently colored miscible liquid streams, L_1 and L_2. The degree of liquid mixing is quantified using confocal microscopy where an ensemble of planar scans is obtained. We demonstrate that the transient nature of gas-liquid flows can be used to significantly improve mixing of miscible liquids compared with existing methods.

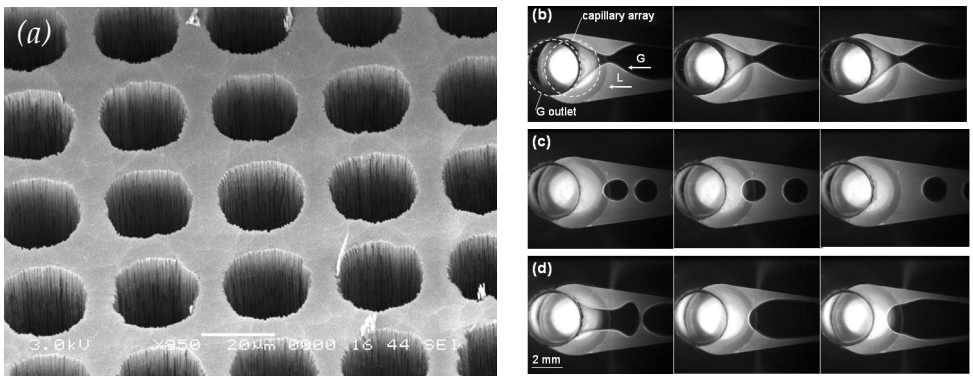

Fig. 19: (a) Microfabricated capillary array in silicon. Annular (b), bubbly (c) and slug flow (d) into the separator.

continued

Flow regime and concentration sensing. We developed a low-cost sensor (See Figure 21) for gas/liquid and liquid/liquid flows in microchannels that does not require direct optical access. It allows detection of individual slugs, bubbles, or drops and can be used to continuously determine their number and velocity. Monitoring the flow regimes in multiphase microchemical systems is important since the reactor performance is directly linked to it. The sensor can be integrated in vertically stacked and horizontally expanded multichannel systems without requiring design changes. It can be used in highly corrosive, purified or toxic media, and comprises of standard, mass-produced components. It can be encapsulated, allowing its use in industrial environments. The analysis of the signal is simple and robust.

Mass transfer measurements. For the model system of oxygen absorption in an oxygen-water flow, mass transfer is linked to the flow regime predictions. Sensing ports are integrated at different streamwise positions on the chip (See Figure 20). They allow a fraction of the liquid phase to be drawn out and passed over an oxygen sensitive foil. In combination with fluorescent microscopy, the local liquid concentration can be determined. A systematic investigation of gas-liquid flow combined with quantitative measurements of mass transfer rates provides a fundamental framework for design and operation of multichannel gas-liquid systems.

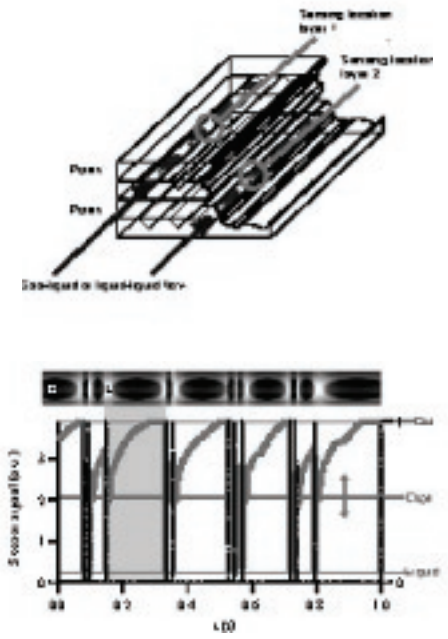

Fig. 21: Integrated flow regime sensor.
Top: schematic of flow regime sensing in a multiplayer reactor stack without optical access.
Bottom: transient sensor signal.

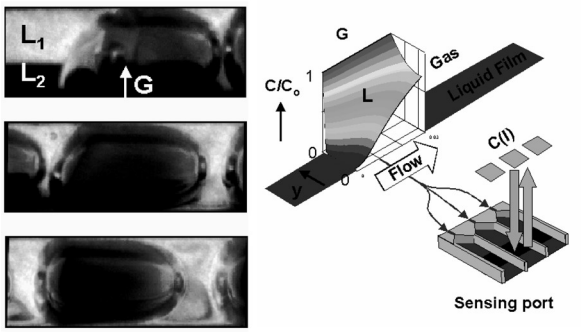

Fig. 20: Left: Mixing of two liquid streams (L1 and L2) by introducing a passive gas stream (G) into a 400 µm channel through one side inlet of cross-section 10x40 µm at 0.67m/s. Streamwise locations (top to bottom) are: gas inlet, 1mm, 3mm downstream of the gas inlet. Right: Schematic of on-chip concentration sensing for gas absorption in an annular oxygen-water flow. The intensity of red light reflected from the sensor film is measured with fluorescence microscopy and represents the oxygen concentration in the liquid.

Microreactors for Catalyst Testing

Personnel

S. K. Ajmera, C. Delattre, and C. D. Baertsch (K. F. Jensen, and M. A. Schmidt)

Sponsorship

MIT MicroChemical Systems Technology Center

We are exploring the use of microfabricated chemical reactors for the improved testing of heterogeneous gas phase catalytic processes. In order that results from the microreactor are relevant to macroscale processes, we are designing microfabricated packed-bed reactors that utilize standard catalyst particles. Through the use of novel flow geometries and fluid distribution mechanisms directly integrated into the reactor design, we have designed a silicon cross-flow micro packed-bed reactor that approaches a gradientless reactor for quantitative kinetics determination. The cross-flow reactor achieves uniform flow distribution over a wide (25.5 mm) but shallow (400 μm long × 500 μm deep) catalyst bed to realize differential conversions with sufficient reaction to allow monitoring with conventional analysis techniques. A set of shallow microfabricated channels maintains a spatially uniform pressure drop irrespective of variations in catalyst packing. Experiments and finite element simulations confirm the bed is isobaric with even distribution of flow and a pressure drop ~1600x smaller than traditional micro packed-bed designs. Quantitative analysis of transport effects indicates that the microreactor length scale suppresses thermal and mass gradients in the catalyst bed. These characteristics make the cross-flow microreactor a superior tool to obtain kinetics and optimize reaction conditions.

Reaction experiments with CO oxidation and acetylene hydrogenation on supported noble metal catalysts confirm the ability of the microreactor to obtain quantitative and accurate information such as turnover frequency (activity), reaction order (mechanistic), selectivity, activation energy, and deactivation that compares well with parameters previously determined in macro-scale systems. Reactor modeling indicates that the catalyst bed operates differentially even at total conversions that would be considered large in traditional reactors adding to the utility of the cross-flow microreactor as an efficient laboratory tool. In addition, CO pulse chemisorption methods have been developed for *in-situ* analysis of catalyst metal surface area within the microreactor, providing a fully functional chemical reactor/analysis tool for catalyst testing (See Figure 22). High temperature/high pressure fluidic interconnects have also been developed for microreactor packaging. This complete technology will allow the operation of multiple reactors in parallel which will enable multi-reactor high-throughput quantitative catalyst testing as well as the development of mini-chemical plants for chemical production utilizing multi-step synthesis.

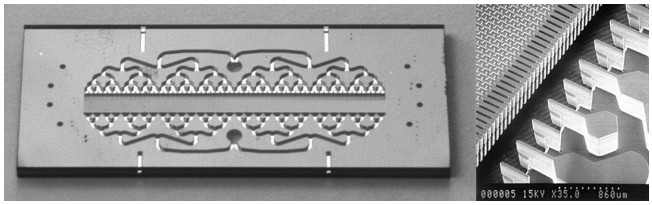

Fig. 22: Photograph of cross-flow microreactor for catalyst testing (Felice Frankel) and electron micrograph of catalyst channel detail.

Scalable Multiphase Microchemical Systems for Direct Fluorination

Personnel

N. de Mas, A. Günther, and T. Kraus (K.F. Jensen and M.A. Schmidt)

Sponsorship

Novartis Foundation and MIT MicroChemical Systems Technology Center

Miniaturization and integration of chemical synthesis with chemical analysis to realize stand-alone microchemical systems could ultimately revolutionize chemical research and development by providing flexible tools to rapidly screen and optimize reactions, catalysts, and materials synthesis. In addition, small reactor volumes enhance the control of fast, exothermic reactions and allow new reaction chemistries deemed too difficult to control in conventional macroscopic reactors to be carried out safely. One example of such type of chemistry is the direct fluorination of organic molecules.

We have developed a microfabricated gas-liquid reactor using standard silicon processing and metal deposition techniques that enables efficient and safe direct fluorination reactions (See Figure 23). Gas and liquid reagents are contacted concurrently at room temperature in the microfabricated reactor and flow distribution patterns are systematically characterized by flow visualization (See Figure 24). To increase the reactor throughput we operate a large number of replicated microfluidic channels in parallel with controlled flow distribution (See Figure 24). Gas-liquid flow regime and temperature in the channels are monitored in situ. Additional separation and detection units could be integrated on chip to create platforms for automated and efficient chemical synthesis.

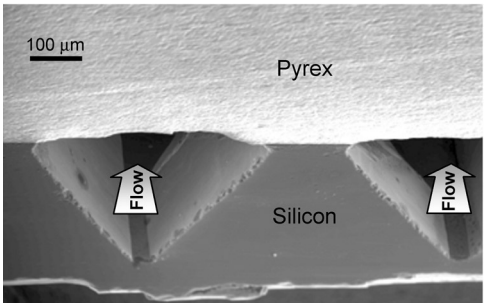

Fig. 23: Cross-sectional scanning electron micrograph of the reaction microchannels.

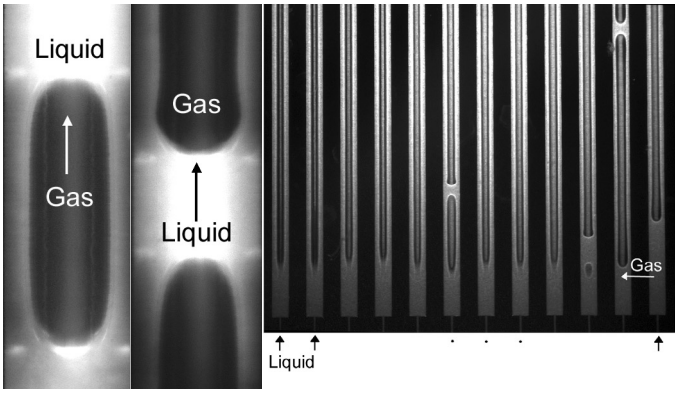

Fig. 24: Gas-liquid flow in a single microchannel with a field of view (FOV) of 435 µm x 1.3 mm (left) and multiple microchannels, FOV of 10 mm x 12 mm (right).

MicroChemical Systems for Separations

Personnel
B. Wilhite, J. Kralj, and E. Murphy (K.F. Jensen and M.A. Schmidt)

Sponsorship
ARO MURI and MIT MicroChemical Systems Technology Center

Several unit operations are used on the macro scale to separate chemical species; examples include membrane separation, extraction, distillation, and chromatography. We have identified separation methods that take advantage of enhanced performance created by the small length scales of microfabricated chemical systems.

Palladium Micromembranes. High hydrogen purity is required in a variety of processes, from the microelectronics industry to PEM fuel cells. Microfabricated Palladium Membranes (See Figure 25) have been shown to enable hydrogen purification at high fluxes and high selectivity.

Work is currently underway to refine our fabrication processes to maximize device lifetime and stability. We are also investigating the use of alternate substrates for improved performance and ease of packaging.

Liquid-Liquid Extraction. The production of fine chemical or pharmaceutical compounds requires multistep synthesis, including the mixing, reacting, and separating of chemical compounds. Since multi-step syntheses typically involve reactive intermediates, it is desirable to run a separation immediately following reaction to reduce product degradation and the overall time required for synthesis. We have designed and fabricated a first generation extractor that utilizes electrocoalescence to separate two emulsified immiscible liquids. Electrical phenomena in general are advantageous because they are non-invasive and can readily be implemented in microfluidic devices. Current work involves characterizing the performance of the extraction system.

Chromatography. This technique is widely used on the macroscale for highly selective separations such as those required for analytical chemistry and pharmaceutical production. A method for performing continuous chromatographic separations on the microscale would open the possibility of fabricating multistep designs requiring highly selective separations. The use of simulated moving bed chromatography as a separation tool on microscale is currently under investigation.

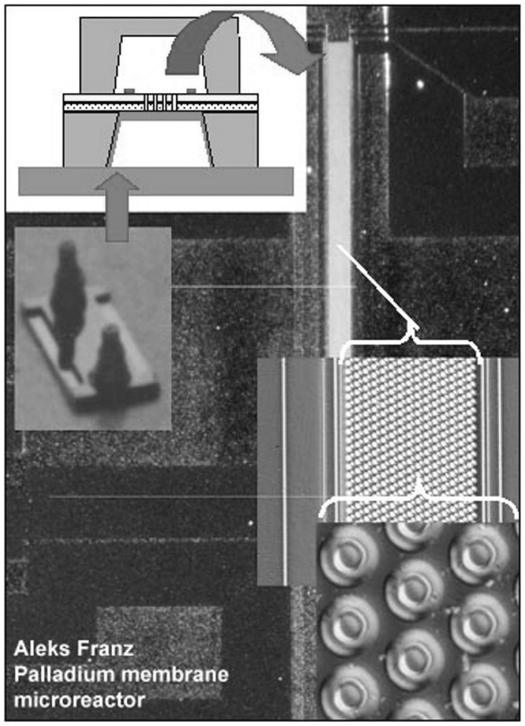

Fig. 25: Palladium micromembranes for hydrogen purification. Membrane device, 200 nm palladium film supported on silicon nitride and oxide membrane with 4 micron holes, image of membrane structure and integrated heater, actual device components.

Three Dimensional Integration of Microfluidic Devices

Personnel
T. Inoue, E. Murphy, and N. Szita
(K.F. Jensen and M.A. Schmidt)

Sponsorship
Institute for Soldier Nanotechnology and
Microchemical Systems Technology Center

The objective of this project is to develop general schemes that enable flexible integration of microfluidic components. In particular, general strategies are being developed to integrate microfluidic devices made by different microfabrication methods with mixed fluidic, electrical, and optical circuit boards as well as hollow fiber platforms compatible with textile technology. Laser direct write techniques are being developed for rapid prototyping of microfluidic and packaging components. The team uses standard microfabrication techniques in silicon and glass as well as new polymer based approaches allowing for flexible, low cost interconnection schemes. Interconnection strategies based on flip chip technology concepts are being developed. UV-based direct laser writing is being pursued as a tool for rapid prototyping of microfluidic devices and packaging components. Different laser direct write approaches and laser wavelength have been surveyed. The use of UV lasers (*e.g.*, ArF excimer laser at 193 nm) allows for laser ablation of commonly used polymers, such as polyimide, PMMA, and polycarbonate as well as glass and ceramics. The technique can be operated as a direct write procedure where the scanning beam ablates material to form microfluidic channels and vias. Alternatively, the UV beam can be used with a mask to ablate an entire section, or a subsection, of a microfluidic design. The latter approach has the advantage of producing smoother surfaces, an important issue for microfluidics, and offering higher throughput than direct write, but at the expense of having to develop a mask. We are exploring the characteristics of both writing approaches in developing the technique for fabrication and integration of microfluidic components.

Low Leakage Micro Switch Valves for Gas Chromatography

Personnel
J. Sihler (A. H. Slocum and J. H. Lang)

Sponsorship
ABB

Microvalves for gas chromatography have high requirements in terms of low leakage, reliability, and chemical inertness. We are designing and building a symmetrical 3-way micro gas valve with an electrostatic actuator that has been chosen for low energy consumption. Figure 26 shows a cross section of the valve. If the plate is electrostatically pulled downwards, the fluid will flow through outlet A; if the plate is pulled up, the fluid will escape through outlet B. The fundamental sealing mechanism is a flat plate on a flat surface, where the width of the valve seat is orders of magnitude larger than the mean free path of the gas. Smooth surfaces are in general easily available (i.e. the surface of a regular silicon wafer is smooth to within 10 Angstroms). Utilizing these surfaces in a microvalve design has the potential of economically creating very well-fitting valve surfaces capable of sealing with a very low leakage. If the valves are to be arranged in an array, the very center silicon layer as well as the back side of the base wafers can be used to create the fluid and electrical interconnections. In this case, the valve chip is packaged with an anodically bonded Pyrex wafer on either side.

Thus far, one-sided prototype valves have been built and are currently under test. Figure 27 shows the test results of the electrostatic actuator. The displacement of the valve plate from its initial relaxed position in the center is plotted with respect to the applied voltage. Pull-in has been observed at 41 Volts where the valve plate displaces by its full stroke of 10 micrometers. Upcoming tests will examine the sealing capability of the closed valves using a He-leakage tester as well as the flow rate dependence on the pressure drop across the open valve.

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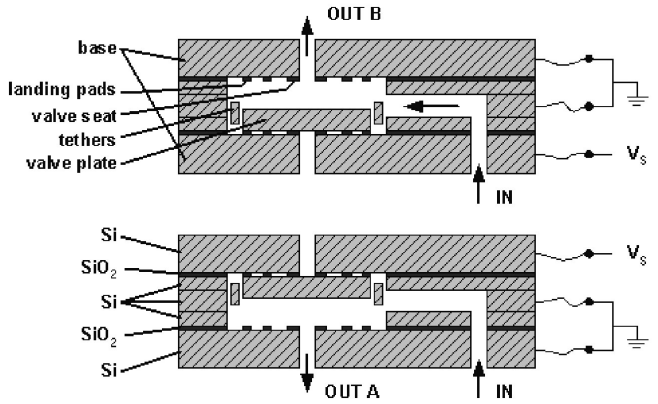

Fig. 26: Switch valve cross section

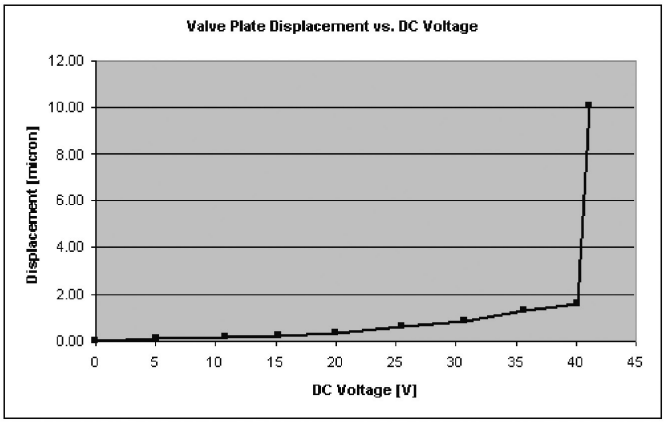

Fig. 27: Valve plate displacement vs. applied DC voltage

Fuel Processing in Microfabricated Chemical Systems

Personnel

L.R. Arana, C.D. Baertsch, B. Blackwell, A. Mitsos (K. F. Jensen, and M.A. Schmidt)

Sponsorship

ARO MURI and DARPA

Chemical fuels store substantially more energy per unit weight and volume than the most advanced batteries currently available. For this reason, portable fuel cell systems operating on chemical fuels have received a great deal of attention in hopes of outperforming batteries in low-power, portable electronics. Given the current state of the art in fuel cell technology, a feed of pure hydrogen is desirable to reach optimal fuel cell efficiencies. However, hydrogen storage presents a challenge due to safety concerns and its low compressibility. Point-of-use hydrogen generation from a conveniently stored liquid fuel (e.g., butane) is a desirable albeit challenging solution to this problem. Our research program investigates the potential of MEMS (Micro-Electro-Mechanical Systems) microfabrication technology to make safe, portable, efficient chemical fuel processors for point-of-use hydrogen generation.

We have developed a fuel processor (See Figure 28) comprised of an integrated high-temperature chemical reactor and heat exchanger. Thin-walled silicon nitride tubes enable a high degree of thermal isolation of the high-temperature reaction zone, and integrated silicon slabs enable heat exchange between process streams. Electrical and combustion heating of the reactor to temperatures over 900°C have demonstrated its high degree of thermal isolation and mechanical stability. In addition, net hydrogen production has been demonstrated through autothermal (no electrical power input) ammonia and butane combustion coupled with ammonia decomposition. Our ongoing research effort can be divided into four major thrusts: fuel processor design and modeling, fabrication and packaging technology, heterogeneous catalysis in microchannels, and reactor testing/overall system assessment.

Fuel processor design and modeling. The optimization of the reactor design is a valuable and challenging aspect of the research effort. One major consideration in reactor design is thermal management, which in this

continued

application means being able to integrate exothermic combustion and endothermic hydrogen-producing reactions such that they exchange heat with each other but lose little heat to the environment. Detailed modeling of fluid dynamics, i.e. heat and mass transfer, and chemical reactions is an important component of the reactor design effort.

Fabrication and packaging technology. The improvement of fabrication and packaging technology is another key aspect of the research program. While a working fabrication process has been developed, improvements to and optimization of the process are still actively being investigated. This includes, but is not limited to, the development of a process for vacuum packaging of the fuel processor.

Heterogeneous catalysis in microchannels. Heterogeneous catalysis, specifically as it applies to reactions in the micro fuel processor, is an essential component of the research effort. Our catalysis research focuses on (1) investigation of methods for the controlled deposition of high-surface-area porous catalyst films (washcoats) into the microchannel structures, (2) development of accurate techniques to characterize these catalyst washcoats *in-situ* (for measurement of active surface area, adhesion to substrate, etc.) before and after carrying out high-temperature chemical reactions, (3) examination of catalyst performance (rate, selectivity, deactivation, etc.) for high temperature fuel reforming and H_2 production reactions, and (4) implications of catalysis (catalyst selection, reaction scheme, etc.) on the optimization of the fuel processor system.

Reactor testing and overall system assessment. Testing of the fuel processor in a variety of hydrogen production schemes is part of the effort to properly assess its potential in portable fuel cell systems. Fuels include butane, methanol, and ammonia, and reaction pathways include partial oxidation, and combustion coupled with thermal decomposition or steam reforming. The need for separations systems and auxiliary equipment, such as pumps, valves, sensors, control systems and plumbing is also being evaluated.

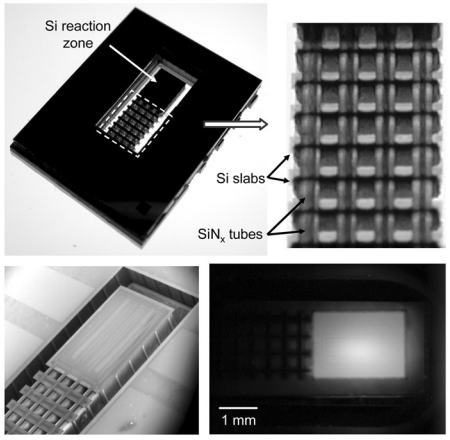

Fig. 28: Micro fuel processor. Photograph of device (top) with close-up of suspended tube/slab structure. Electron micrograph of reactor/heat exchanger section (lower left). Glowing reactor during autothermal combustion and ammonia cracking (Note, that the tubes and surroundings remain at low temperatures).

Microchemical Systems for Fuel Processing and Conversion to Electrical Power

Personnel

L. Arana, C. Baertch, J. Cui, J. Hertz, A. Ie, C. Lee, A. Mitsos, O. Nielsen, T. Stefanik, K. Turner, and S. Weiss
(K.F. Jensen, P. Barton, S.M. Spearing, M.A. Schmidt, H. Tuller, and J.Y. Ying)

Sponsorship

ARO MURI

This program aims to develop a fundamental understanding of the different physical phenomena underlying fuel processing at millimeter to micron scale as well as to establish the engineering principles needed to realize portable electrical power generation from hydrocarbon fuels.

Portable, high density power sources have been identified as an enabling technology. A continued reliance on batteries, combined with their relatively low projected energy densities, create serious logistical mission constraints. Taking advantage of the high energy density of chemical fuels to generate power becomes an attractive technological alternative to batteries. However, development of fuel processors capable of chemical/electrical conversion with a net power output on a portable scale represents a significant technological challenge.

Microreactors as miniature fuel processors represent an emerging technology that could significantly impact our ability to produce high density power sources in the future. The program aims to develop a fundamental understanding of the many different physical phenomena underlying fuel processing at millimeter to micron scale as well as to establish the engineering principles needed to realize portable electrical power generation from hydrocarbon fuels based upon advances in microfabrication, fuel cells, catalysis, materials characterization, and systems engineering. Competing approaches to fuel conversions are addressed with particular emphasis on two basic strategies:

- Conversion of hydrocarbons to hydrogen for use in a hydrogen fuel cell by partial oxidation, reforming, and product separation steps.

- Direct conversion of hydrocarbon fuels in a microfabricated solid oxide fuel (SOFC) cell system integrated with microfluidic controls.

In order to address the many different aspects of microfabricated fuel processing systems, we have a multidisciplinary research team that combines the necessary expertise, specifically in the areas of thermomechanical properties of materials, materials synthesis, microfabrication, chemical reaction engineering, heat transfer, catalysis, simulations, and systems engineering. This multidisciplinary research program has set the following goals for the proposed effort:

- Development of design and microfabrication strategies for microchemical systems capable of operating at elevated temperatures and being rapidly cycled between low and high temperatures. This will entail the development of novel fabrication strategies involving high temperature materials such as oxides not currently used in standard, mainly silicon-based, microfabrication methods.

- Synthesis and characterization of novel catalytic materials for low temperature partial oxidation and reforming as well as for novel SOFC electrodes. In particular, tailored heterogeneous catalytic surfaces for microchemical systems will be generated by forming nanostructured features on surfaces of micron-scale flow channels.

- Fundamental understanding of and engineering approaches to integration of materials with different thermophysical properties into systems undergoing large spatial and temporal temperature variations.

- Fundamental understanding of transport and reaction processes in microchemical systems. Development of engineering design principles and simulation tools for microreactor systems.

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- Systems engineering concepts and tools for understanding and predicting the performance of integrated microchemical systems at steady state and during transients, i.e., dynamic behavior.

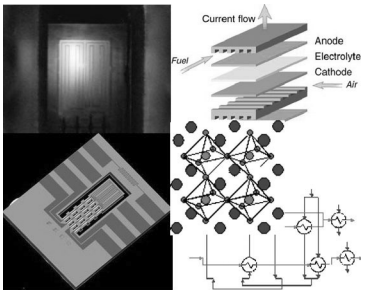

Fig. 29: Different elements of the fuel processing program; fuel processor, microcombustor, solid oxide fuel cell schematic, crystal structure of catalysts, energy integration diagram.

Piezoelectric Micro Power Generator (PMPG): A Novel MEMS-Based Electrical Power Source

Personnel

R. Sood and Y.B. Jeon (S.G. Kim and S. Sarma)

Sponsorship

Auto-ID Center

Concept and Key Idea

A MEMS-based energy harvesting device is designed and fabricated that converts ambient, acoustical energy to electrical energy via the piezoelectric effect. The electrical energy is subsequently stored within the device to act as a constant, electrical power source in replacement of a common battery or wired supply.

Design and Fabrication

The PMPG (Piezoelectric Micro Power Generator) is a device currently in the microfabrication stage. It converts ambient acoustical and/or vibrational energies to electrical energy via the piezoelectric effect. Unlike conventional batteries, the PMPG will provide power for an infinite duration of time, provided there is ambient energy available. It consists of a composite cantilever beam with top interdigitated electrodes and an added proof mass.

The ambient energy is coupled into the first resonance mode of the mechanical structure. When the device is in resonance, the generated electrical signal will be sinusoidal in nature. The signal must, therefore, be rectified before the resulting charge can be stored. The PMPG is designed to deliver a high open circuit voltage and electrical power specification due to its exploitation of the d_{33} excitation mode of the piezoelectric material (PZT). The d_{33} mode has been calculated to provide up to 20 times the open circuit voltage value of a d_{31} device with the same beam dimensions. The converted electrical energy is then stored, effectively creating a portable, electrical power source capable of driving low power digital circuits among other applications. These devices are, therefore, suitable for powering small wireless sensors or Auto-ID tags. The PMPG would replace chemical batteries in these low power applications and would, in fact, be better because the PMPG will have a virtually infinite operation lifetime.

continued

Figure 30 shows a picture of the ideal, released PMPG. The device employs a surface micromachining process using XeF_2 vapor etcher in order to create the released micro-cantilever structure. The composite beam includes a SiO_2/ZrO_2 membrane layer that acts as an electrical diffusion barrier, a PZT piezoelectric layer and a Pt interdigitated electrode layer. Figure 31 is an electrical equivalent circuit model of the PMPG, along with the rectifying circuitry necessary before charge storage. Figure 32 contains two polarization curves of a sample PMPG device. After poling, the electric dipoles within the PZT are aligned, allowing for device operation. A small array of these devices is expected to permit a power density of approximately $10\mu W/mm^2$. The final PMPG is released from the bulk silicon by way of a XeF_2 isotropic etch step. Acoustic operation frequency is set between 20 kHz and 40 kHz, outside of the audible range. Figure 33 shows an overhead view of an actual, pre-released device.

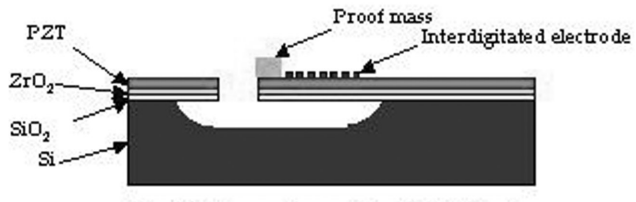

Fig. 30: Surface micromachined PMPG device

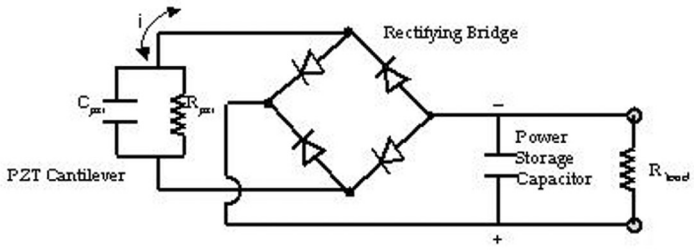

Fig. 31: Electrical equivalent circuit model of PMPG with full-wave rectifier

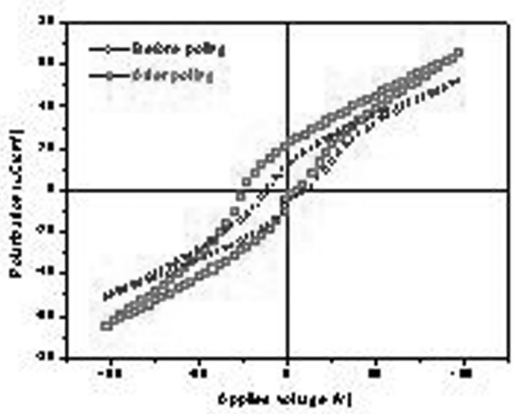

Fig. 32: PE hysteresis curves of the PMPG device before and after poling

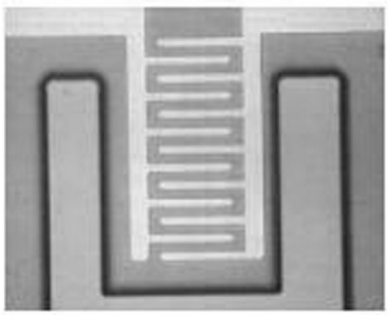

Fig. 33: Top View of interdigitated PMPG fabricated

Development of Hydrocarbon-Fueled Silicon Combustors for Micro Gas Turbine Engines

Personnel

C. M. Spadaccini, J. Peck, N. Miki, and L. Ho (I.A. Waitz)

Sponsorship

ARL, ARO, and DARPA

Recent advances in the field of silicon micro-fabrication techniques and silicon-based MicroElectroMechanical Systems (MEMS) have led to the possibility of a new generation of micro heat engines for power generation and micro air-vehicle propulsion applications. The design for a silicon-based, micro gas turbine generator capable of producing 10-50 Watts of power in a volume less than 1 cm^3 while consuming 7 grams of fuel per hour has been developed.

An engine of this type will require a high temperature combustion system to convert chemical energy into kinetic and thermal energy. To accomplish this, a unique set of challenges must be overcome:

1. Shorter residence time for mixing and combustion.
2. Heat loss due to high surface area-to-volume ratio.
3. Material and structural constraints of silicon.
4. Rudimentary 3-D geometry due to limits of micro-fabrication techniques.
5. Micro-engine thermodynamic cycle constraints.

All of the above impact the design and development of a suitable micro-combustion system.

The baseline micro-combustor device is comprised of all the non-rotating functional components of the micro gas turbine engine. The device measures 2.1 x 2.1 x 0.38 cm and is aligned-fusion bonded from 6 silicon wafers. Figures 34 and 35 show a schematic and a SEM of this micro-combustion system. Fabricated largely through Deep Reactive Ion Etching (DRIE), the structure required anisotropic dry etching through a total thickness of 3,800 μm. Complete with a set of fuel plenums, fuel injector holes, pressure ports, and compressor and turbine static airfoils, the design of the six-wafer structure required a multi-disciplinary approach that accounted for all the chemical, structural, and fluidic interactions as well as engine system considerations.

For the propulsion and power generation applications of interest, the principal figure of merit is power density. The baseline device achieved power densities in excess of 1100 MW/m^3 with hydrogen-air combustion. This corresponds to exit gas temperatures over 1700 K and combustor efficiencies greater than 95%. In an attempt to achieve higher power densities, a staged combustor has also been developed. With this device, a 100% increase in power density was achieved for some operating conditions. These power densities are about two times larger than those produced by a conventional gas turbine combustor and are an order of magnitude larger than other power MEMS devices. Hydrocarbon fuels, such as ethylene and propane, have been burned in these devices at lower power densities, 500 MW/m^3 and 150 MW/m^3 respectively. Data from both the staged and baseline combustors has been used to develop a non-dimensional operating space which can be used as a design tool for gas phase combustors.

A combustor which utilizes heterogeneous catalysis to improve hydrocarbon-air reaction rates has been identified as a means of increasing power density for hydrocarbon fueled micro-combustors. A six-wafer catalytic micro-combustor similar to that shown in Figure 34 was fabricated. During the fusion bonding process, the combustion chamber was fitted with a piece of platinum coated foam to serve as the active catalytic surface. With propane fuel, this device operated at significantly higher mass flow rates than its gas-phase counterpart and achieved an ~8-fold increase in power density. However, this combustor did not achieve high exit gas temperature and overall efficiency. As a result, low order models have been used to identify the device as diffusion controlled, and design recommendations for a second-generation catalytic micro-combustor have been made.

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Thermophotovoltaic Micro-Generators

Personnel

O.M. Nielsen and C.D. Baertsch
(K.F. Jensen and M.A. Schmidt)

Sponsorship

DARPA

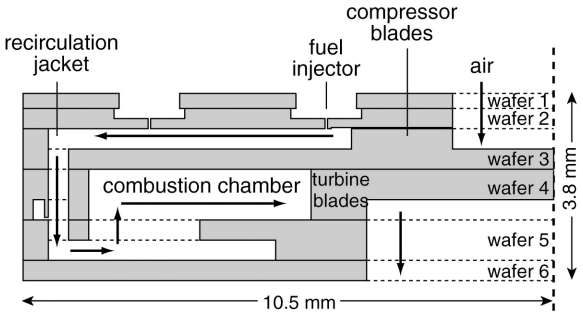

Fig. 34: Schematic of six-wafer combustion system.

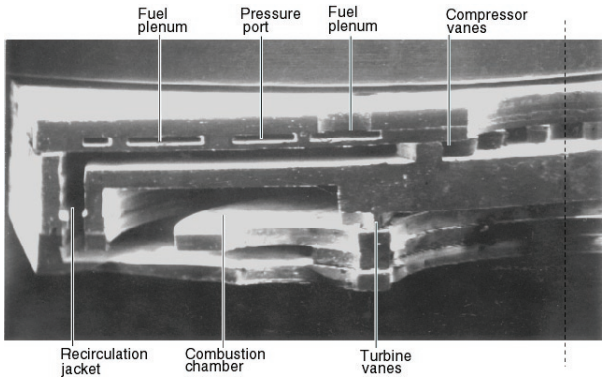

Fig. 35: SEM cross-section of six-wafer combustion system.

Based on a suspended-tube micro chemical reactor developed at MIT, this project aims at converting heat released from the reactor by radiation into electrical power by the use of low-bandgap photovoltaic cells. The devices are ultimately likely to be operated at around 1000ºC, at which temperature the radiation is mostly in the infrared regime, calling for low-bandgap converter materials such as GaSb or GaInAsSb. The cells are obtained commercially or from other research programs, while the emitter structure, photon recycling scheme, thermal management, and packaging (including vacuum) are developed within the project.

The ThermoPhotoVoltaic (TPV) micro-generator has been successfully operated with a net 1 mW (32 mW/cm^2) electrical power output, at an efficiency of 0.08%. The emitter temperature was approximately 770ºC during operation, and one GaSb photocell was used for energy conversion. According to conservative estimates for a TPV micro-generator with some basic improvements (two photocells, vacuum packaging, and 1000ºC emitter temperature), 16 mW (250 mW/cm^2) net power and 2.4% efficiency should be obtainable with the current structure. The advantage of increasing the emitter temperature cannot be over emphasized, as is clear from the test results shown in Figure 36.

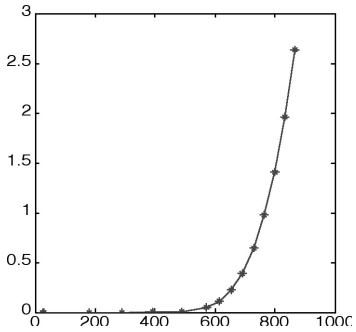

Fig. 36: Photocell power output and system efficiency, as a function of temperature, during electrical heating of the SμRE.

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Among the photons emitted, only those that have energies above the photovoltaic cell bandgap can be converted into electricity. This combined problem of emitter characteristics and photon recycling will be approached in different ways. Since radiation is a surface property, the reactor (emitter) surface can be tailored to yield more desirable radiation spectra. Many different material and structural systems are possible candidates (e.g. SiC, photonic crystals), but fabrication complexity must be weighed heavily in making choices. Photon recycling schemes include filters and back-side reflectors on the photovoltaic cells. Most likely, a combination of these different approaches will be pursued.

A new, optimized reactor structure for TPV purposes is currently under fabrication. Packaging of the entire structure, including the photovoltaic cells, will be investigated. Vacuum packaging will be essential, and some work has already been done. The ultimate goal is to demonstrate a device that can convert chemical energy to electricity with an overall efficiency in the 10-15% range. Power density goals are on the order of 1 W/cm^2. The work is targeted at developing a replacement technology for batteries in certain applications based on higher energy conversion efficiencies and energy densities.

Micro-fuel Cell

Personnel
J. Hertz and T. Stefanik (H.L. Tuller)

Sponsorship
DoD Multidisciplinary University Research Initiative (MURI) administered by the Army Research Office.

The feasibility of integrating a solid oxide fuel cell structure into a micromachined silicon structure is being investigated as part of a larger multidisciplinary group. The performance of thin film electrolytes and electrodes is being studied as a function of composition, microstructure, and device structure. Processing procedures are being developed which enable the functional solid state ionic films to be incorporated into a micromachined silicon structure.

Lateral RF MEMS Switch with PZT Actuation

Personnel
Y. Shi and T. M. Lee (S.-G. Kim)

Sponsorship
KIMM

Concepts and Key Idea
A new RF MEMS switch with lateral contacts is being designed and developed for wireless mobile communication applications. The objective of this project is to develop a RF switch with much improved robustness, compactness, reliability, and low cost comparing to the existing RF switches. The major advantages of the piezoelectric lateral contact RF switch will be very low driving voltage (less than 5 Volt), very low contact resistance (less than 0.1 Ω), and very high reliability (more than 100 billion cycles), which are essential for real applications without scarifying the benefits of MEMS switches, such as low insertion loss, near zero power consumption, and very high isolation, etc. The device is enabled by strain-amplified PZT actuators which provide the mechanical movement creating the open or short circuit in the RF transmission line.

Design and Fabrication
To achieve the major objectives of very low contact resistance and very high reliability, maintaining a large and real electric contact area is critical, which requires the elastic-plastic deformation of the metal-metal contact layers. PZT actuator is chosen for the large force and displacement it can provide. Lateral contact switch configuration is adopted to take full advantages of the PZT actuators. The switch function of the device is achieved through the lateral contact of two switching components. The mechanical movement and force required for the contact is realized through large-strain thin film piezoelectric actuators which use PZT ($Pb(Zr,Ti)O_3$ as the active material. The displacement from PZT is amplified by more than 10 times by the amplification mechanism for each individual actuator. Actuators are also combined in parallel or series to provide larger displacement or bigger force requirements. Lateral displacement of 10 μm can be achieved with less than 5 volts actuation in a footprint of less than 500 μm x 500 μm. Larger contact area (> 10 μm^2) and larger gap (about 5 μ) are maintained between the two switching components which provide low insertion loss, but high isolation and high power handling capacity. Su-8 has been chosen as the switch structure material for its unique property of making near vertical sidewall structures and also its good mechanical properties. Mathematical modeling for the contact behavior and FEM simulation of the device design is being done to optimize the overall performance of the switch. A schematic view of the device with e-beam Au layer on the side and folded Au layer are shown in Figure 37 and Figure 38 respectively.

PZT is deposited using Sol-gel method, and several approaches have been investigated to fabricate the displacement amplification mechanism of the actuator. Spin-on Su-8 has been chosen as the structure materials for its unique properties and compatibility with the actuator. The most critical part of the switch fabrication is the deposition of contact metal on the contact areas on the sidewall of the Su-8 structure. We have chosen Gold layer for our initial tests. The electrical contacts are crucial for the performance of the switches. Two methods have been investigated to create the metal contact layers. The first one is to fold a thick metal film already deposit on the bottom surface of the structure into the gap between the two contact components, while the second is to deposit the metal film on the contact surface using e-beam evaporation or sputtering process. The Gold layer on the side wall of a Su-8 structure with negative slope using e-beam evaporator is shown in Fig. 39. An initial test shows the resistance across the side wall is less than 0.4 Ω, which can be improved further by having a relatively vertical or positive side wall slope. The sidewall slope due to fabrication will have significant influence not only on the metal layer quality, but also on the ohmic contact. Efforts have been made to ensure high quality metal-metal contacts required. Fabrication of the device is still ongoing.

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MEMS Tunable Capacitor and LC Tank

Personnel

X. Yang (A. H. Slocum, J. H. Lang, and M. A. Schmidt)

Sponsorship

Deshpande Center

Currently there is a great demand, especially in the wireless communication area, for frequency agile devices that are capable of frequency tuning and selection in the ultra-high and super-high frequency. Furthermore, integration of such devices with the transceiver circuit is highly desirable in order to reduce total costs and power consumption. The goal of this research project is to use MEMS technology to develop a high Q, highly tunable LC oscillator that is suitable for frequency agile tuning from 2 to 5 GHz or higher.

The design of the capacitor originates from the ideas of "Nanogate" and "Zipper Actuator", two devices being developed in the group, and uses the fact that two smooth, perfectly matched surfaces can be pried apart with an external actuator, and the gap between the surfaces can be accurately controlled. An LC tank is devised by incorporating a cavity inductor with the capacitor design.

A 2-D cross section of the tunable capacitor is shown in the Figure 40. It comprises three wafers anodically bonded together: the top and the bottom wafers are Pyrex wafers while the device wafer is a SOI (Silicon-On-Insulator) wafer. The device wafer contains a membrane that is supported on tethers from the sidewall and the fulcrum (with a ring shape) that's anchored to the top Pyrex wafer. The fulcrum is the pivot of rotation for the membrane. The outer rim of the membrane forms the zipper actuator that pins down to the bottom Pyrex wafer when a voltage is applied. Using the fact that gold does not bond to oxide, we can obtain a perfect match of the dielectric of the capacitor with its bottom electrode upon bonding. The capacitance at this position corresponds to the maximum. When voltage is applied to the zipper actuator, the center of the membrane bows up and hence changes the gap of the capacitor that's formed between the membrane and the bottom aluminum electrode. The change in the gap results in the change in the capacitance, and hence, a tunable capacitor is formed.

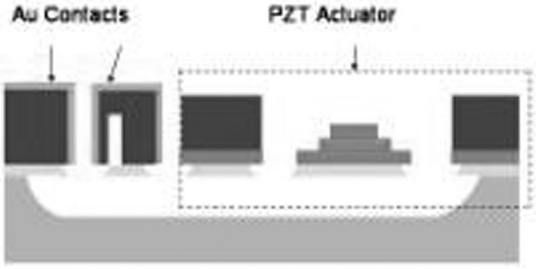

Fig. 37: A schematic view of the switch.

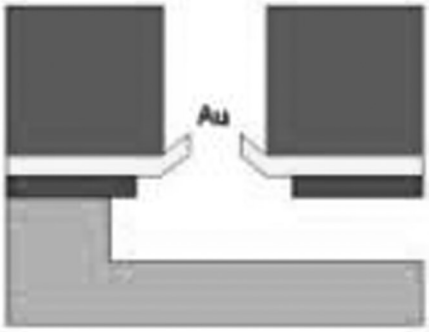

Fig. 38: Folding Au layers into sidewall

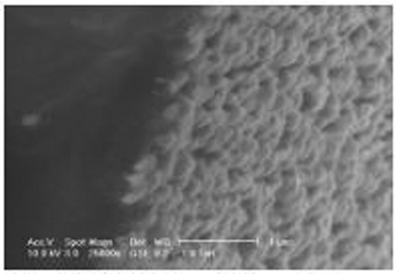

Fig. 39: SEM picture of side wall Au

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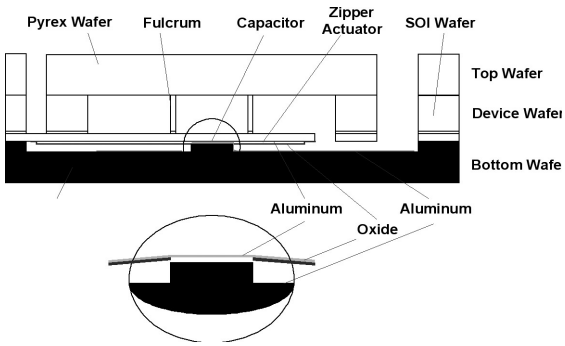

Fig. 40: 2-D schematic of the design of a tunable capacitor.

Currently, fabrication of the tunable capacitor is underway. A major challenge was to form the cylindrical fulcrums with walls less than 50 μm thick and 300 μm tall. This has been done successfully using STS. Figure 41 is the SEM photo of the cross-sectional view of the fulcrum.

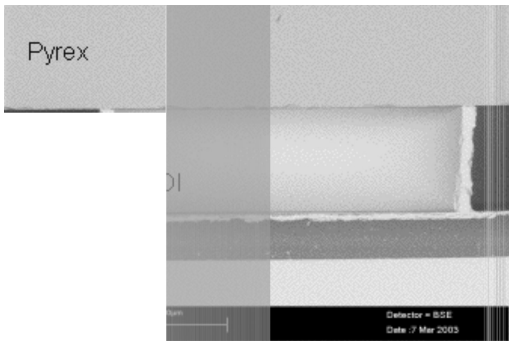

Fig. 41: SEM photo showing the cross-sectional view of fulcrum.

There are many challenges in the project in terms of fabrication, RF design, packaging, and integration. The fundamental contributions expected include: to demonstrate a high tuning ratio capacitor that has not been reported before; to create innovative fabrication solutions that could benefit other users; to develop a frequency agile MEMS LC tank; and to explore the potential of RF MEMS in fulfilling RF communication needs.

DRIE-Fabricated Curved-Electrode Zipping Actuators with Low Pull-In Voltage

Personnel

J. Li (J.H. Lang and A.H. Slocum in collaboration with M.P. Brenner)

Sponsorship

n/a

Electrostatic curved-electrode zipping actuators have been developed to generate high force and large displacement simultaneously. Laterally-moving actuators fabricated with DRIE could provide greater stroke and force without a significant increase in actuator size. However, DRIE constraints limit the minimum electrode-cantilever gap during a deep etch, and hence, result in actuators with larger starting voltages. The goal of this project has been to build a monolithic low pull-in electrostatic curved electrode actuator fabricated by Deep Reactive Ion Etching (DRIE).

We have designed and fabricated the actuators. Figure 43 shows two such curved-electrode zipping actuators with compliant cantilevers utilized to actuate a bistable MEMS relay. Figure 42a shows the relay beam (11) ready to be actuated by the actuators (3&7) through a T-bar (6). As shown in Figure 42b, the starting cantilevers (2&9) are attracted and pulled in to the corresponding actuator cantilevers when electrified. The gap is closed, and a very high electric field and force is created. The actuator beams then zip along the fixed electrodes (1&10) at relatively low voltage to actuate the bistable relay beam as shown in Figure 42c. Finally, an electrode (5) with its two compliant starting cantilevers (4&8) is used to pull the relay beam back to the initial position as shown in Figure 1d.

The device is fabricated using DRIE. After etching, 0.2-micron of oxide is grown on both the surface and side-walls. A shadow wafer is then used to etch the oxide off the top surface of the electrodes to achieve good electrical contact. The device wafer is bonded with a Pyrex handle wafer, and the electrodes are isolated with snap off tabs as a last step. Contact metalization makes low resistance relay contacts.

Figure 43 shows an optical micrograph of actuators with starting cantilevers fabricated into a bistable relay. Figure 43a shows the relay as fabricated. In Figure 43b the starting cantilever bends up at low voltage to close the gap and pull in. In Figure 43c the actuator cantilever zips completely to toggle the bistable relay beam as shown in Figure 43d. The actuators each measure 4.5 mm * 100 μm * 300 μm, excluding the contact electrodes and the relay beam. The pull-in voltages of the actuators were measured to be between 75 and 85 V. After pull-in, the actuator cantilever zipped along the electrode with increasing voltage, pushing the relay to its opposite bistable position. The voltage required to toggle the relay beam was measured to be between 100 and 140 V. During this actuation, the two actuator cantilevers developed a combined 8-mN force while translating 80 μm before toggling the bistable relay beam. Actuators and relay beams were operated using a bipolar drive at 100 Hz for over 120 hours through more than 40 million cycles without stiction or fracture. The devices have been switched with voltage pulses as short as 400 μs. The time taken for the actuator to close the relay was measured to be 3 ms.

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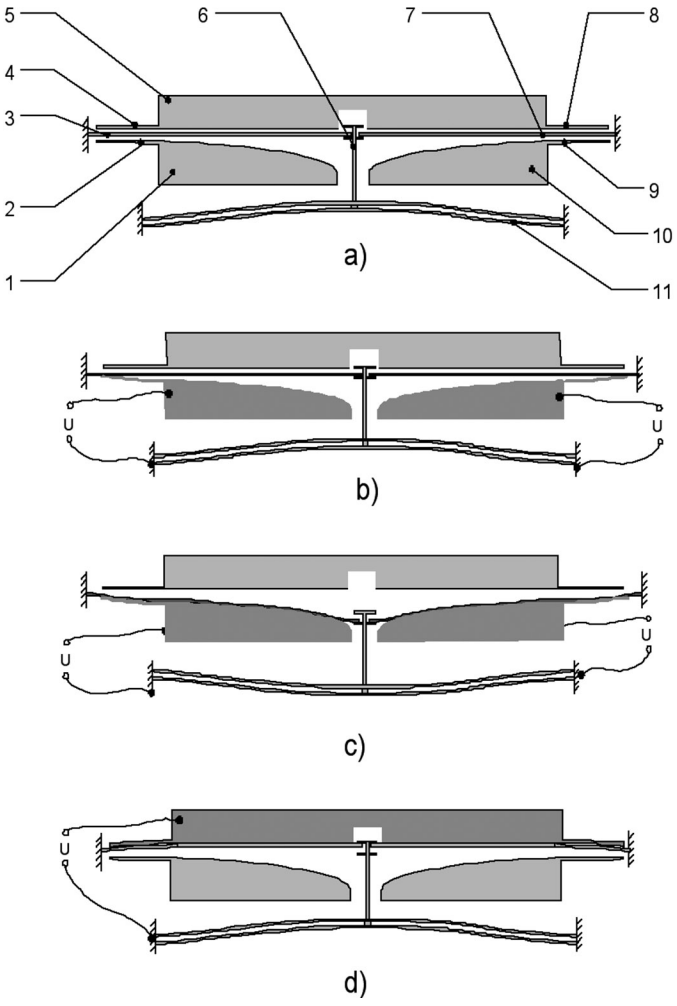

Fig. 42

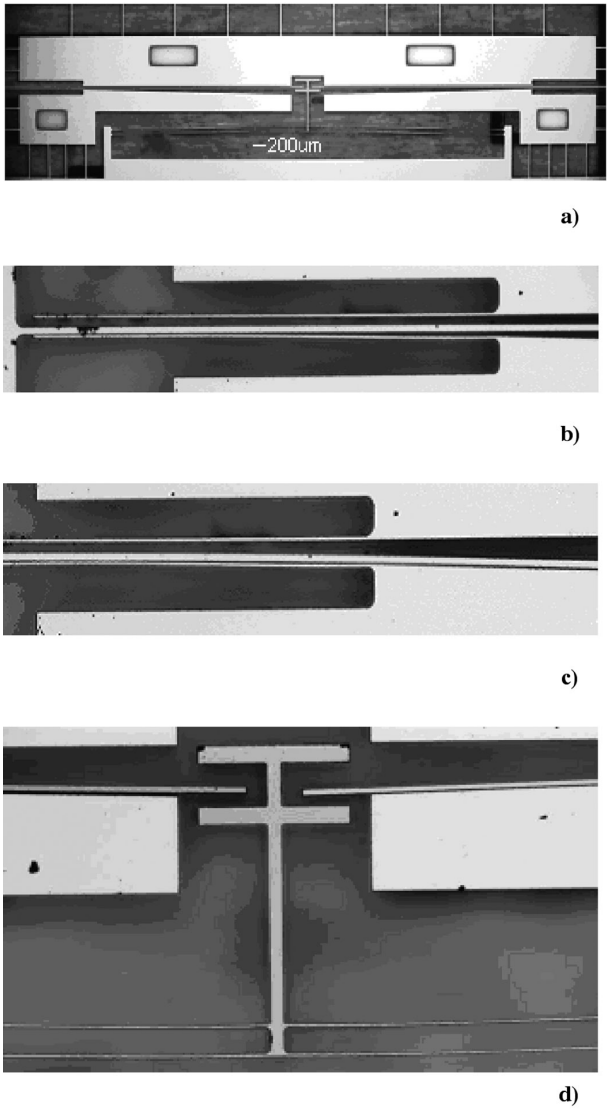

Fig. 43

MEMS Amplification of Piezoelectric Strain for In-Plane Actuation

Personnel
N.J. Conway (S.-G. Kim)

Sponsorship
KIMM

Concepts and Key Idea
Though MEMS piezoelectric actuators can provide very high force output at low driving voltages, they have a very small strain, typically only a couple of tenths of one percent, leading to very limited applications in real world. A new method of amplifying the small strain of in-plane piezoelectric actuators has been developed. Very compact in-plane piezoelectric actuators with a few percent of strain will enable very compact MEMS devices replacing the existing bulky electrostatic actuators. The entire device is designed and fabricated using batch micro-fabrication techniques, averting the need for costly micro-assembly of the actuator with a piezoelectric element (See Figure 44).

Design and Fabrication
The strain amplification is achieved through the fabrication of a compliant mechanism. A piezoelectric membrane, made of PZT, is situated in the middle of four parallel guiding linkages comprising the actuation mechanism. The pivot points are small length flexural pivots or living hinges designed to approximate an ideal pivot, but without any backlash associated with a real pivot. Because the angles the pivots subtend are small, the pivots behave close to ideal. By amplifying the membrane displacement, the compliant structure sacrifices some piezoelectric force, however, the PZT membrane provides sufficient force that the output force is still desirable (order 100 μN). Each actuator has a form factor of 500 μm X 500μm X 30μm, and the expected output displacement is 6 μm. The actuator can easily be arrayed in n-parallel to gain an n-times force advantage or in series to gain an n-times displacement advantage, with the drawback of increased form factor.

The compliant mechanism is made of SU-8, which allows the entire device to be surface micro-machined. The PZT membrane is fabricated first, followed by the SU-8, followed by a release. A process for single-crystal silicon-based compliant mechanism has also been devised. Batch-fabricated in-plane micro-piezoelectric actuators have not been done before to our knowledge. As this is an ongoing project, no experimental results of a final device are available.

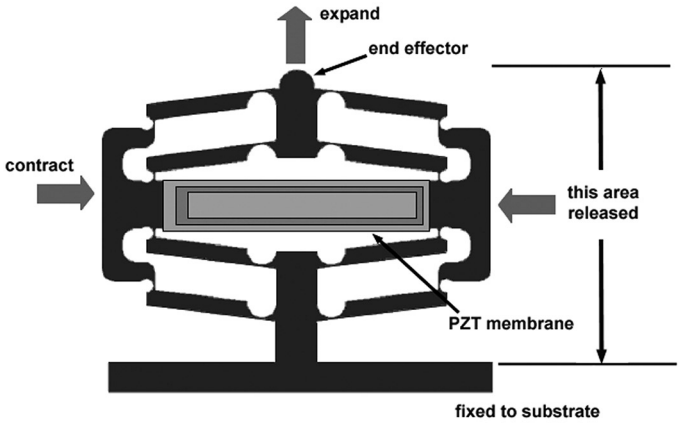

Fig. 44: A Bow Actuator Design for Strain Amplification

Water-Immersible Micromachined $Pb(ZrTi)O_3$ Thin Film Actuator

Personnel
Y.B. Jeon and C.W. Wong (S.-G. Kim)

Sponsorship
Department of Mechanical Engineering

Concept and Key Idea

There have been many efforts to overcome two major problems in SPM technologies: slow scanning speed and inability to measure living cells underwater. We demonstrate the water-immersible thin film PZT actuator; the whole PZT is sandwiched between the top and bottom metal electrodes to prevent water permeation and can be used for *in-vivo* or *in-vitro* SPM measurements of living cells under water or biological fluid. This can also be used for the direct actuation of microfluidic devices in various wet applications.

Design and Fabrication

In order to be water-immersible, the electrodes need to be electrically insulated and the piezoelectric layer needs to be waterproofed. This paper describes our design solution and process for a water-immersible piezoelectric device, which separates the bottom electrode from the top electrode by having a narrow ditch covered with PZT film. The whole PZT film is then encapsulated with the top metal electrode, which seals envelopes together with the metal layer left outside ditch of the lower electrode. In this structure, the whole PZT is sandwiched between the top and bottom metal electrodes to prevent water permeation. Figure 45 shows the water-immersible PZT cantilever beam designed.

The width of the ditch is the key design parameter for both electrical separation and good microstructure of PZT on top of the ditch. We tested several widths of the ditch and got good dense PZT microstructure and electrical insulation with the 2 μm width of ditch. The surfaces of the PZT film on the 2 μm separated Pt bottom electrode region ("P" region in Figure 45) were observed at three adjacent points by AFM (Figure 46). The piezoelectric constant, d_{31} is about -100pC/N. The dielectric polarization and fatigue properties of the devices were measured in air and water. The spontaneous polarization, remnant polarization, coercive field, and dielectric constant are 54 $\mu C/cm^2$, 15 $\mu C/cm^2$, 60 KV/cm and 1200, respectively (Figure 47(a)) and the polarization property of the device was unchanged whether it was in the air or under the water until $1x10^9$ cycles (Figure 47(b)).

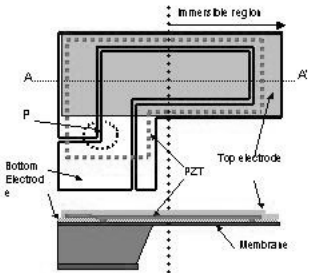

Fig. 45: Device schematic of water-immersible piezoelectric actuator.

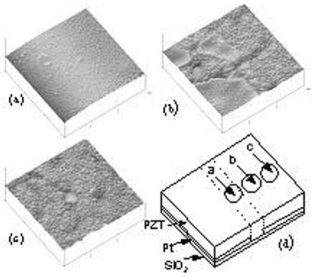

Fig. 46: AFM images of the PZT film surface and intersection diagram pf the PZT film on the separated Pt bottom electrode region; (a) PZT surface exact on the separated Pt; (b) PZT surface near on the separated Pt; (c) PZT surface on Pt bottom electrode; (d) Schematic diagram of the regin "P" in Figure 1(a) which was observed by AFM.

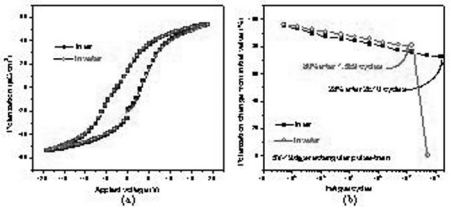

Fig. 47: Polarization property changes of the PZT films. (a) P-E hysteresis curve deposition; (b) Fatigue properties against number of cycles in air or water.

Wafer Bond Alignment and Strength Characterization

Personnel
C. Tsau and H. Verma (C.V. Thompson, M.A. Schmidt and S.M. Spearing)

Sponsorship
SRC

We are exploring the property-process relationship of wafer-level thermocompression bonding process. This bonding technique relies on the simultaneous application of pressure and temperature to bring mating surfaces to close proximity and bond. In our study, we bond two silicon wafers together with thin, patterned gold. Gold is the preferred bonding material because it does not oxidize easily, which simplifies the surface treatment prior to bonding. The bond is performed between 260 and 300°C, permitting the bonding of MEMS and/or IC wafers together after the devices have been fabricated. In addition, because gold is conductive, parts of the bonding layer may also be used for local signal routing. Lastly, hermetic seals may be achieved, which is important in some inertial sensor applications.

We have established a wafer-level bonding protocol for 4" wafers using a commercial bond tool (Electronic Visions) and a mechanical testing technique for quantifying the bond toughness. The four-point bend-delamination technique measures the critical load at which crack propagates at the bonding interface. The specimen geometry and the critical load then allow the critical strain energy release rate, or the input energy at which delamination is required, to be calculated. We have performed bonding at varying temperatures (260 and 300°C) and pressures on the gold (7 to 120 MPa) (See Figure 48). Our current effort is directed towards understanding the source of non-uniformity and variation in the bond toughness.

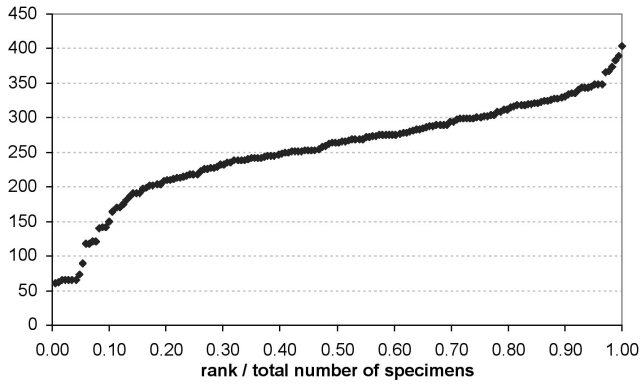

Fig. 48: Bond toughness data for specimens bonded at 300°C and 73 MPa (on gold).

Microelectromechanical (MEMS) Thin Film Stress Sensors

Personnel

R. Bernstein, A.L. Giermann, S.C. Seel, and D. Moore (C.V. Thompson)

Sponsorship

CMI, NSF, and SMA

We have designed and fabricated several microelectromechanical devices for measurements of film stress during deposition and post-deposition processing.

The operation of one class of devices is based on buckling of membranes and beams. Single-crystal Si membranes can be made through patterned anisotropic etching of bonded silicon-on-insulator wafers (See Figure 49a). Films can then be deposited on these membranes, and if the films are under a state of sufficiently high compressive stress, they will cause the membranes to buckle. The buckling state can be characterized using a variety of tools, but optical profilometry provides a particularly straightforward technique for characterization of the buckled membrane shape, with sufficiently high vertical spatial resolution to allow determination of film stresses through comparison with models for buckling. If the compressive insulating oxide film is left as part of the membrane, membranes within a size and thickness range will be buckled in the as-fabricated state (See Figure 49b). This state can be characterized before and after film deposition to measure the changes caused by the deposited film, thereby allowing characterization of the stress in the film. This technique allows determination of the stress states of both tensile and compressive films and can also be used when films are deposited on both sides of the membranes (e.g., by chemical vapor deposition). Buckling of composite, doubly-supported beams can also be used for film stress measurements.

The second class of devices under investigation is based on micromachined cantilevers, made of single crystal silicon alone, silicon nitride alone, or as part of a composite beam structure. The deflection of these cantilevers can also be characterized with very high vertical spatial resolution using an optical profilometer. The '*sample*' cantilever can be 'actuated' by another cantilever, for example a rectangular AFM cantilever, as shown in Figure 50. Both cantilevers can be imaged concurrently. This second cantilever, also known as the '*sense*' cantilever, is made of single crystal silicon, so the mechanical properties are well known. Because of this, the force applied to the sample cantilever can be calculated and from this, the modulus of the sample cantilever can also be calculated. We are also using these simple devices for the study of thin film plasticity which is typically investigated by application of strains due to differential thermal expansion between a film and its substrate during heating and cooling. However, these cantilevers can be isothermally deflected through application of a known force at their tip using the sense cantilever, causing a known strain in films deposited on the sample cantilevers. The stress state resulting from deformation can be characterized using the optical profilometer measurements of the beam shape during and after release of the applied force. Studies of time-dependent changes in beam shapes also allow the study of time-dependent inelastic phenomena. Because micromachined cantilevers can be made very thin, Transmission Electron Microscopy (TEM) can be used to study the effects of inelastic deformation at the nano-scale. Continuous films will be studied, as will small structures (for example, sub-micron square dots) whose small dimensions limit dislocation formation and motion.

A third device has been developed for *in-situ* studies of stress evolution during film formation and during post-deposition processing. This device is made using a (110) Si wafer that is bonded to an oxidized (100) wafer and thinned to a thickness of 20μm. A cantilever beam with 4 resistors wired in a Wheatstone bridge structure is then fabricated in the (110) Si layer (See Figure 51). Three resistors are oriented so as to have no piezoresistance, and one is oriented so as to have high piezoresistance. When films are deposited on these piezocantilevers, forces exerted in the silicon cause stresses that can be characterized through measurement of the piezoresistance. *In-situ* stress measurements require only electrical feed-throughs in the UHV deposition system and can be made with a sensitivity of less than 1MPa-μm, even with these relatively thick beams. These piezocantilevers can be readily heated and cooled and can be used for measurement of stresses caused

continued

by films deposited via chemical vapor deposition (in which deposition occurs on both sides of the cantilever). These devices have been used for *in-situ* measurements of stress during formation and growth of polycrystalline films. We are currently investigating alternative, and simpler, fabrication processes.

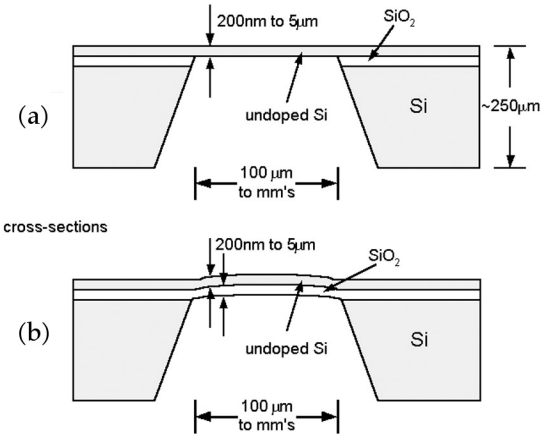

Fig. 49: (a) Micromachined single crystal Si membrane. (b) Pre-buckled composite Si-SiO_2 membrane

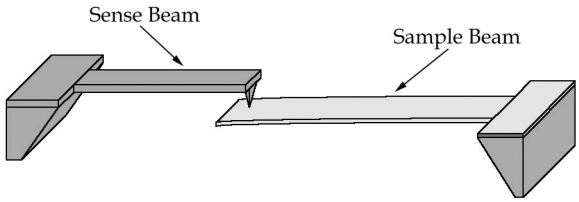

Fig. 50: Micromachined 'sample' cantilever being actuated by AFM 'sense' cantilever

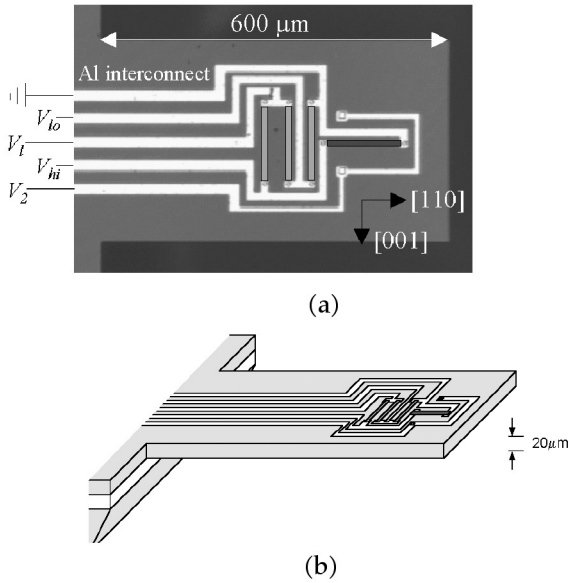

Fig. 51: (a) Top view and (b) Perspective view of a micromachined piezocantilever for in-situ *stress measurements during film deposition*

3D Nanomanufacturing via Folding of 2D Membranes

Personnel

S. Jurga and C. Hidrovo-Chavez (H. I. Smith, and G. Barbastathis)

Sponsorship

NSF and CMSE

Functional Three-Dimensional (3D) Nanostructures are necessary in numerous technological domains. The 3rd dimension promises to extend the pace of ever faster processors and higher-capacity memories beyond "the end of Moore's law," *i.e.*, when feature sizes of planar electronics reach their minimum practical limit. Commercial research in that direction is already in progress. In applications other than electronics, the need to conquer the 3rd dimension is even more urgent. Examples are: optical elements integrating sensing and processing for defense or commercial applications, miniature reactors for chemical and biochemical analysis in homeland security, drug delivery by miniaturized microfluidic implants, micromechanical and nanomechanical energy storage elements, environmental monitoring and industrial quality control applications, etc. However, 3D fabrication is not nearly as well understood and developed in the state of the art. Our CMSE seed grant research aims to take the 3D challenge with a specific method for 3D fabrication and assembly, which we refer to as "membrane folding." For a three dimensional technology to be successful and widely applicable to the worlds of solid-state electronics, MEMS, and nanomanufacturing, it must satisfy the functional requirement of sufficient connectivity between the micro and nano devices that compose the system (i.e. the transistors and capacitors of a microchip). Additionally, a winning technology must avoid fighting against the momentum of an existing industry with established tool-sets and large capital investments; a new 3D technology must be easily integrated and compatible with current methods of fabrication that remain planar in nature (i.e. photolithography, plasma etching and deposition, which are all 2D).

Our approach is a two step process designed to satisfy the following functional requirements: (a) integration of dimensional scales from the nano to the micro and beyond; (b) maximum utilization of existing fabrication tools; and (c) flexibility in achieving a large number of possible 3D configurations with minimum cost and maximum repeatability and yield that meets the connectivity constraint, provides an additional means for actuation, and allows for the seamless integration of existing 2D fabrication methods as well as new advances in the state of the art photolithography and nanopatterning. In the first step, all devices are fabricated on a planar substrate just as they are in today's semiconductor industry. In the second step an assembly technique is applied which the planar substrate is folded into a 3D or quasi-3D structure by appropriate actuation means. Imagine creating a microchip as a long ribbon, and then folding the ribbon over on itself many times as depicted in Figure 52. Designated compliant zones act as hinges between stiffer regions that contain micro and nano devices. By virtue of compliant circuitry that spans the hinge areas, full 2D connectivity is preserved across the entire length of the ribbon, even after folding. This is important for electronics as well as communication in MEMS sensors and actuators and integrated nano devices. An additional source of connectivity may also be achieved in the vertical, third direction by designing vertical connections to be formed when the planar folds are designed to contact each other at predetermined locations during folding.

Most connectivity remains within the plane and through the compliant hinges, while sparse connections permeate the vertical direction.

In our preliminary work, we have demonstrated a single 180 degree fold in a silicon-based device with magnetic actuation effecting induced folding (See Figure 53). The gold hinges are plastically deformed so that the folded membrane remains near 180 degrees. Electron beam evaporated gold was chosen for the compliant hinges due to its high ductility and comparatively small spring back angle. The hinges also complete a current loop around the perimeter of the membrane. By placing the device in a magnetic field and controlling the magnitude of current in this loop, a Lorentz force is generated that rotates the flap about its hinges. The Lorentz force is highly controllable and thus allows extensive

continued

continued

experimental characterization of the mechanics of folding in our device. In the future, we will also explore different means of actuation such as stress and chemically induced folding. Some of these alternatives are more attractive than the magnetic method from the point of view of alignment and flexibility in 3D assembly. is an ideal means of actuation for the first round of prototypes because it is a highly controllable force that allows for good experimental analysis of the mechanics of folding.

The architecture achieved through various folding techniques is unique to the micro and nano realm because it creates a framework for building devices and structures that were previously impossible to imagine or too expensive to fabricate with other methods. For exampleAt present, our study aims to build 3D diffractive optical elements (3D-DOEs) as a case study in the technology development for folded-membrane devices. Moreover, 3D-DOEs promise better performance in terms of light efficiency and angular selectivity than customary 2D diffractive optical elements that are customarily fabricated nowadays. Spacing multiple diffractive gratings or Ffresnel zone plates (perhaps as many as 50) vertically above one another establishes a matched filter with very high efficiency. The device could be fabricated using a sequence of bonding and etch-back steps, yet this would not only be costly, but very time consuming. Therefore, we plan to achieve the same results in a less expensive and more timely fashion by the folding scheme.

The first 3D diffractive device is displayed in its unfolded state, still attached to the substrate in Figure 54. Electrostatic combdrives tune the period of the binary grating, so as to change the angle of the diffracted orders. The fresnel Fresnel zone plate (essentially a diffractive lens) will be folded over and aligned to the grating as a demonstration of compound diffractive optics in 3D created through folding.

Future work will focus on the final alignment and latching of the folds in addition to new actuation methods for folding that could be categorized as templated-self-assembly. Work in implementing multiple folds and studying their behavior of multiple folds is also underway. These steps are the early formative building blocks for establishing a multi-use platform. 3D assembly through folding lends itself to broader reaching goals such as combining discrete devices of varied functionality (optics, electronics, microfluidics, etc) into one cohesive, self-contained system capable of advanced sensing and response.

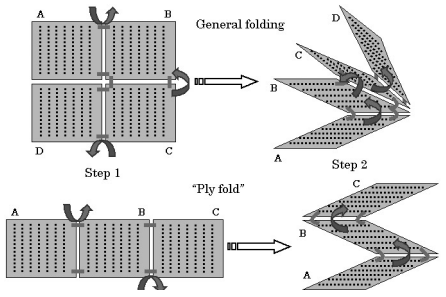

Fig. 52: Examples pre-fabricated thin 2D membranes folded into 3D structures in a two-step process. Black dots denote surface features nanofabricated on the membrane surface, and grey lines denote "hinges."

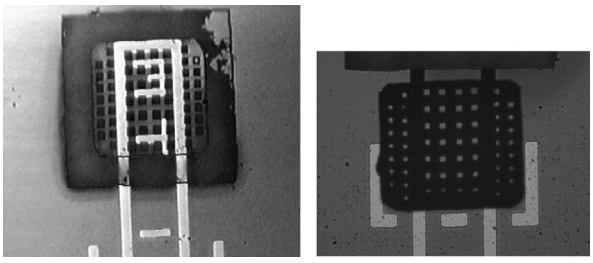

Fig. 53: Membrane flap before folding (left) and after folding to 180 degrees (right). Note the alignment tolerance achieved in folding (alignment fiducials are 50μm wide).

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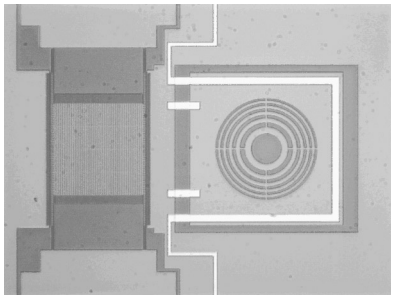


Fig. 54: Top view of tunable grating (left) and static Ffresnel zone plate (right) before folding.

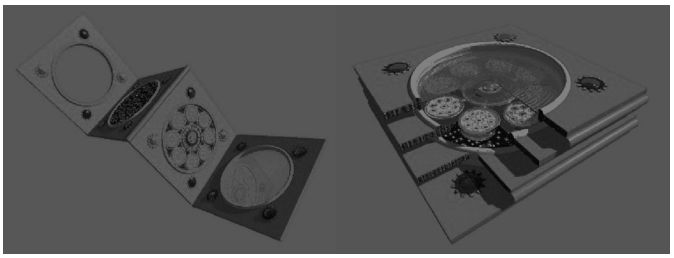


Fig. 55: An example of a heterogeneous system created through folding. Optics, microfluidics, nanopatterning, and circuitry are fabricated within the plane and then folded into one complete functional system.

Nano-Scale Machining with Femtosecond Laser Pulses

Personnel

J.Y. Jia and M. Li (C.V. Thompson)

Sponsorship

Panasonic Boston Laboratory

Researchers at the Panasonic Boston Laboratory have demonstrated the use of femtosecond laser pulses to drill 200nm-diameter holes in silicon films on insulating substrates. This technology has potential applications in microphotonics. We are collaborating in research on microstructural evolution in the vicinity of the drilled holes. This is expected to provide further insight into the drilling mechanism.

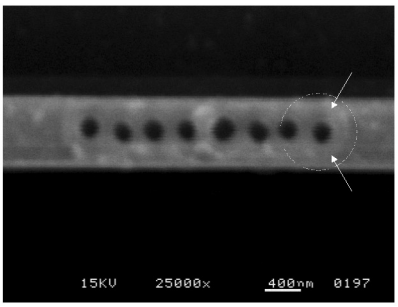


Fig. 56: SEM image of holes drilled into a Si line on oxidized Si. A femtosecond laser was used.

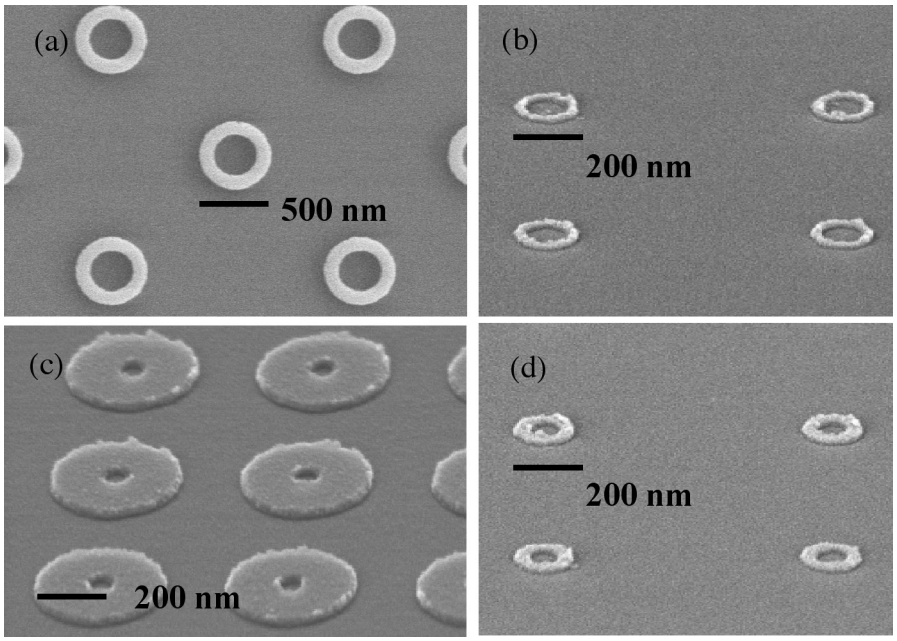
Opposite page:

Plan-view and tilted scanning-electron micrographs of four arrays of Co rings with diameters and linewidths of (a) 520 nm and 120 nm, (b) 190 nm and 30 nm, (c) 360 nm and 160 nm, (d) 180 nm and 50 nm.

Courtesy of C.A. Ross, H.I. Smith, F.J. Castaño, Y. Hao, M. Walsh, D. Gil, A. Eilez, E. Lyons, in collaboration with F. Humphrey and M. Redjdal (Boston University)

Sponsor:
Cambridge-MIT Institute and NSF

Electronic Devices



Electronic Devices

- *Exploring Transport in Ultra-Thin Silicon Films for Double-Gate CMOS*
- *Ultra-Thin Strained Silicon on Insulator*
- *Germanium MOSFETs for CMOS Applications*
- *Impact Ionization in Strained-Si/SiGe Heterostructures*
- *Impact of Ion Implantation Damage and Thermal Budget on Mobility Enhancement in Strained Si n-MOSFETs*
- *MOSFET Channel Engineering Using Strained Si, SiGe, and Ge*
- *Implementation of Both NMOS and PMOS Having High Hole and Electron Mobility in Strained Si /Strained Si_{1-y} Ge_y on Relaxed $Si_{1-x}Ge_x$ ($x<y$) Virtual Substrate*
- *RF Power CMOS*
- *A Metal/Polysilicon Damascene Gate Technology for RF Power LDMOSFETs*
- *Partially- and Fully-Depleted Strained-Si/strained-$Si_{1-y}Ge_y$ MOSFET's Fabricated on Relaxed $Si_{1-x}Ge_x$-On-Insulator (SGOI)*
- *InP-HEMTs for Ultrahigh-Frequency Power Devices*
- *Hydrogen Degradation of InP High Electron Mobility Transistors*
- *Electrical Reliability of RF Power GaAs PHEMTs*
- *Coplanar Integration of Lattice-Mismatched Semiconductors with Silicon by Wafer Bonding Ge/SiGe/Si Virtual Substrates*
- *CMOS-like Fabrication of InP-HEMTs for 100 Gbit/s Photonics*
- *Nanomagnets and Magnetic Random Access Memories*
- *AlGaAs/GaAs HBT with Enhanced Forward Diffusion*
- *The MIT Microelectronics WebLab v. 5.0*

Exploring Transport in Ultra-Thin Silicon Films for Double-Gate CMOS

Personnel

I. Lauer (D. Antoniadis)

Sponsorship

SRC

Deeply-scaled Double-Gate (DG) and Ground-Plane (GP) MOSFETs require ultra-thin silicon channels in order to maintain electrostatic integrity. Experimental evidence has shown reduced mobility compared to bulk for silicon films between 15 nm and 7 nm. However, theory indicates that between 5 nm and 3 nm increased occupancy of the 2-fold valleys results in increased mobility compared to bulk. This work seeks to gather experimental evidence for the increased mobility in sub-5 nm films.

A schematic of a process to build ultra-thin channel DG/GP MOSFETS is shown in Figure 1. Starting with SOI wafers (1-1), LOCOS isolation is performed (1-2), followed by silicon thinning (1-3). Then a gate oxide is grown, polysilicon is deposited, and the over-sized bottom gates are patterned (1-4). LTO is then deposited, planarized (1-5), and the wafer is bonded to a handle wafer (1-6). The bulk of the original SOI wafer is then removed by mechanical grinding and chemical etching, using the buried oxide as an etch stop. The buried oxide is then removed with a timed etch, exposing the silicon channel (1-7). The top gate oxide is grown, polysilicon is deposited, and the short top gate is patterned (1-8). Spacers are defined (1-9), followed by raised source/drain growth (1-10). Salicide is then formed (1-11). Interconnects are added to finish the device.

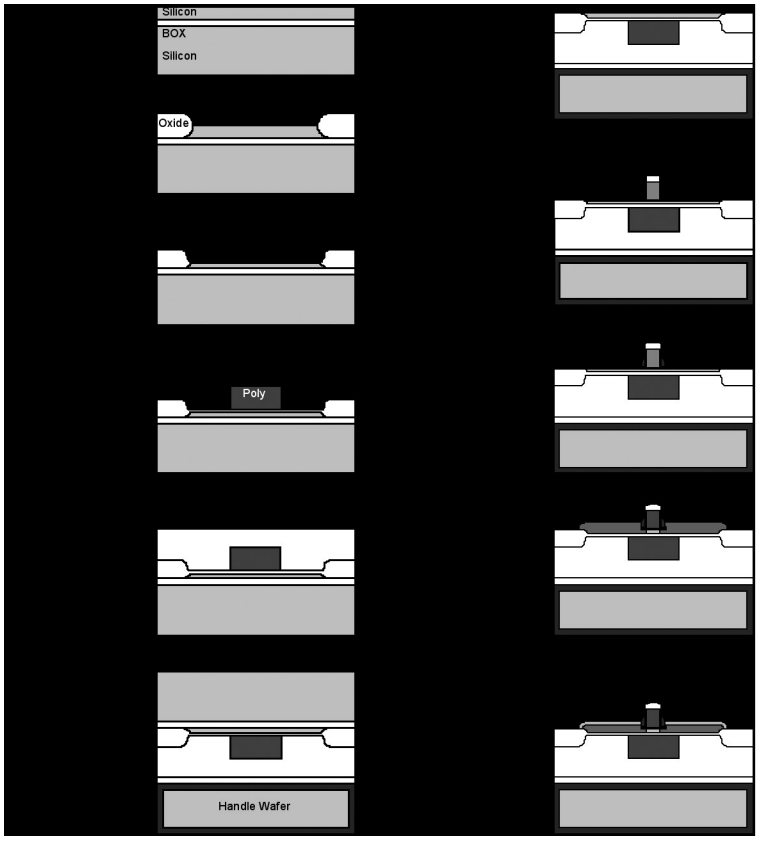


Fig. 1: Ultra-Thin Si DG MOSFET Fabrication

Ultra-Thin Strained Silicon on Insulator

Personnel
T. Drake (J. L. Hoyt)

Sponsorship
SRC and MARCO Focused Research Center on Materials, Structures, and Devices (MARCO/DARPA)

Epitaxial strained Si films grown on relaxed epitaxial SiGe exhibit biaxial tensile stress. MOSFETs fabricated with strained Si channel layers exhibit significantly enhanced mobility and current drive. Incorporating strained silicon in ultra-thin body and double-gate MOSFET structures offers potential advantages. First, these structures enable reduction of channel doping compared to bulk MOSFETs. Second, double gate transistors enable operation of the device at low vertical effective fields where the strain-induced mobility enhancement for holes is maximized. Finally, if strained Si is incorporated directly on insulator, without the presence of SiGe in the final structure, some of the problematic effects of SiGe (e.g. Ge diffusion and enhanced n-type dopant diffusion) can be eliminated. Thus, there is strong motivation to study the fabrication and material properties of ultra-thin strained Si films on insulator. This work focuses on the creation of strained silicon layers directly on insulator and the critical issue of whether the strain remains *after* the SiGe layer that originally induced the strain has been removed.

Fundamental limits to CMOS scaling are rapidly approaching as devices are scaled below the 50 nm range. Therefore, new methods and materials for CMOS fabrication must be investigated to allow continued device improvement. It is well known that SOI devices provide benefits of reduced parasitic capacitance allowing for high-speed operation while minimizing power dissipation. Ultra-thin body SOI devices have the added benefit of improved electrostatic integrity, and thus, can be scaled to the shortest channel lengths. Recent work on surface-channel strained Si MOSFETs fabricated on relaxed $Si_{1-x}Ge_x$ show significant performance improvements. Most notably strain-induced transconductance leads to up to 60% enhancement for NMOSFETS over Si controls. In this work, a novel fabrication method for ultra-thin strained silicon on insulator substrate is demonstrated. Thermal stability of these films is also investigated.

Our research is focused on both the fabrication of strained Silicon Silicon On Insulator (SSOI) as well as the investigation of an ultra-thin body devices. In order to fabricate high quality ultra-thin body strained Si MOSFETs, thin strained silicon on insulator layers must be produced. In this work the fabrication of ultra-thin strained silicon directly on insulator is demonstrated, and the thermal stability of these films is investigated. Ultra-thin (~13 nm) strained silicon on insulator SSOI layers were fabricated by epitaxial growth of strained Si on relaxed SiGe, wafer bonding, and an etch back technique employing two etch-stop layers for improved across across-wafer thickness uniformity. The epitaxial heterostructure used in this work is shown in Figure 2.

A cross sectional transmission electron micrograph of the final strained silicon on insulator structure is shown in Figure 3. Raman analysis of SSOI using 325 nm excitation shows the strained Si peak at 512 cm^{-1}. The shift from the relaxed Si peak at 521 cm^{-1} corresponds to a strain of 1.2%, in excellent agreement with the strain in the as-grown film prior to layer transfer. In addition, no shift in the strained Si peak is observed after Rapid Thermal Annealing (RTA). Using 325 nm Raman spectroscopy, no strain relaxation is observed following rapid thermal annealing of these layers to temperatures as high as 950ºC (Figure 4). The thermal stability of these strained silicon films after removal of the strain inducing SiGe layer which induced the strain is promising for the future fabrication of enhanced performance strained Si ultra-thin body and double-gate MOSFETs.

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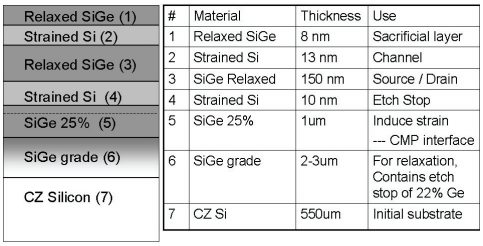

#	Material	Thickness	Use
1	Relaxed SiGe	8 nm	Sacrificial layer
2	Strained Si	13 nm	Channel
3	SiGe Relaxed	150 nm	Source / Drain
4	Strained Si	10 nm	Etch Stop
5	SiGe 25%	1um	Induce strain --- CMP interface
6	SiGe grade	2-3um	For relaxation, Contains etch stop of 22% Ge
7	CZ Si	550um	Initial substrate

Fig. 2: As grown epitaxial heterostructure for creation of ultra thin strained-silicon on insulator via a bond and double etch stop process.

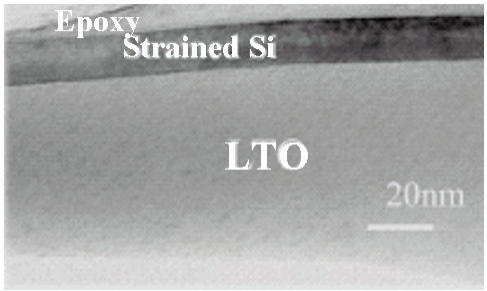

Fig. 3: XTEM of ultra-thin strained-Si on insulator. Strained Si thickness is 13-15 nm

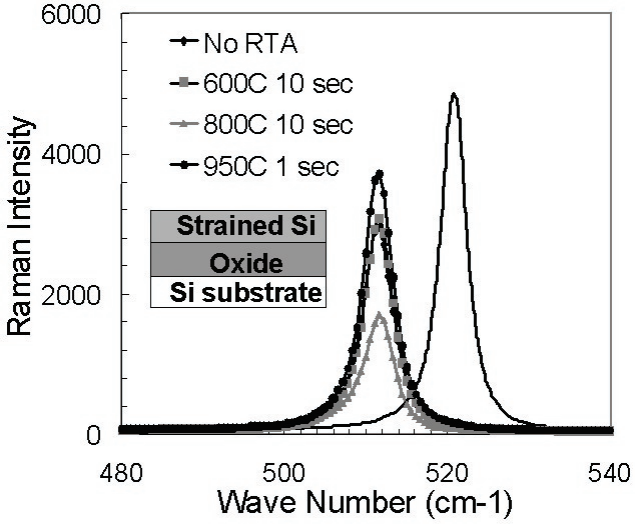

Fig. 4: Raman analysis of SSOI using 325 nm excitation shows shift of 9 wavenumbers between silicon and strained-silicon peak corresponding to a strain of 1.2%, in excellent agreement with the strain in the as-grown film prior to layer transfer. In addition, no shift in the strained-Si peak is observed after RTA. Raman data courtesy N. Klymko, IBM Microelectronics.

Germanium MOSFETs for CMOS Applications

Personnel

A. Ritenour and M.L. Lee (D.A. Antoniadis and E.A. Fitzgerald in collaboration with S. Yu, Intel Corporation)

Sponsorship

MARCO Focused Research Center on Materials, Structures, and Devices (MARCO/DARPA)

New material systems are playing an increasingly important role in MOSFET scaling. Strained-silicon and silicon germanium have received significant attention because they offer improved carrier transport relative to bulk silicon. However, neither material offers enhancement in both electron and hole transport. Germanium, on the other hand, has a bulk electron mobility that is a factor of 2.6 larger than silicon and a hole mobility that is a factor of 4 larger. The advent of high-k dielectrics presents a new opportunity to reconsider high mobility semiconductors like germanium that have been dismissed in the past because they lacked a high quality thermal oxide.

The goals of this project are to demonstrate enhanced carrier transport in germanium and strained germanium MOSFETs, develop process technology suitable for ultra-scaled germanium MOSFETs, and explore fundamental issues associated with germanium devices. Germanium PMOSFETs have been fabricated on both bulk germanium wafers and epitaxial germanium-on-silicon. Figure 5 shows the layer structure of the epitaxial germanium-on-silicon substrates. Hafnium dioxide and tantalum nitride were used for the gate stack. These films were deposited through a collaboration with Professor D.L. Kwong at the University of Texas at Austin. Silicon fabrication processes were modified to make them compatible with germanium. Figure 6 shows the extracted hole mobility from a bulk germanium PMOSFET. The mobility is enhanced by a factor of two compared to silicon. Future work will focus on the fabrication of short-channel germanium CMOS on epitaxial germanium-on-silicon.

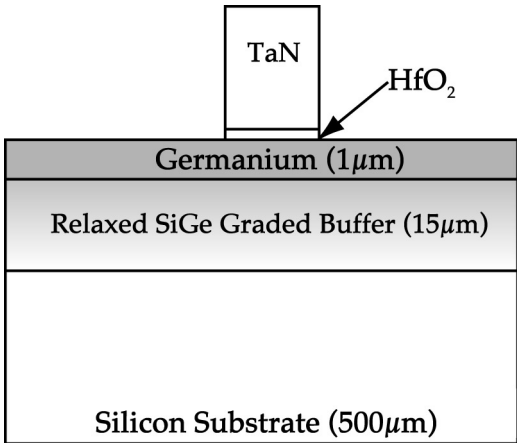

Fig. 5: Layer structure of epitaxial germanium-on-silicon. The 1 μm germanium device layer was grown on a relaxed SiGe graded buffer using UHVCVD.

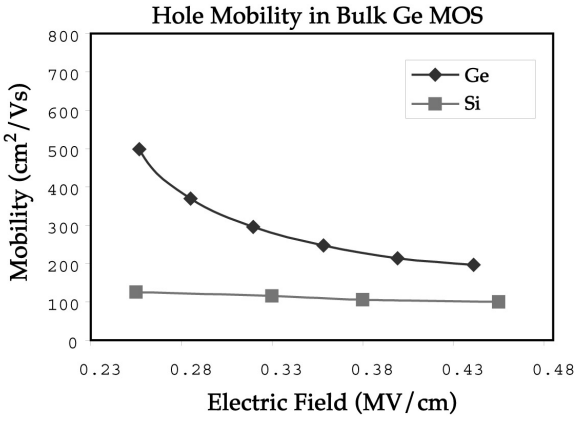

Fig. 6: Comparison of hole mobility in Ge and Si PMOSFETs. The germanium devices show a factor of two enhancement in mobility.

Impact Ionization in Strained-Si/SiGe Heterostructures

Personnel
N. Waldron (J.A. del Alamo)

Sponsorship
DARPA

Strained-Si is actively being pursued as a technology that can continue to drive CMOS further along the scaling road map. The resulting enhancement in the fundamental transport properties of Si due to the introduction of strain yields improved device speed and diminished power dissipation. Currently, the main focus of research for strained-Si/SiGe MOSFET technology is for digital applications. However, the potential exists to use strained-Si for analog mixed-signal applications such as wireless communication products. The development of high-performance Si-based RF power devices that can operate in the 10-20 GHz range at power levels of 100s of mW would rival the performance of GaAs technology, but with a lower associated cost and with the potential for System-on-Chip integration.

Impact ionization is an important consideration for RF power devices. It determines the breakdown voltage and by extension the maximum power that a device can deliver. Impact ionization will be of particular concern to strained-Si technology. The strained-Si/SiGe heterostructure comprises of a relaxed SiGe buffer layer on which the thin strained-Si layer is epitaxially deposited. The bandgap of SiGe and strained-Si is lower than that of bulk Si. Also, the strain induced in the thin Si layer breaks the degeneracy of the conduction band, resulting in reduced scattering compared to bulk Si. Both will have the effect of increasing the impact ionization rate.

Test structures were designed and fabricated in order to investigate impact ionization effects in the strained-Si/SiGe heterostructure (see inset in Figure 7). The heterostructure comprises of a fairly thick relaxed SiGe buffer (4 μm) with a thin strained-Si layer on top. In this p-type structure an n-type resistor-like device is made. As higher voltages are applied to the device, the field and electron velocity increase, and impact ionization takes place towards the drain. The hole current thus induced is collected by the body contact which is on the backside of the wafer.

The figure summarizes the results obtained from the test structures. M is the impact ionization multiplication factor, and M-1 is a useful figure of merit to gauge how much extra current is generated by impact ionization. It is clear that the strained-Si samples have much higher II compared to bulk Si as would be expected. What is more interesting is that strained-Si exhibits a strong positive dependence on temperature, which is opposite to what is seen in bulk Si. Both of these results could be problematic for the implementation of strained-Si technology to RF power devices.

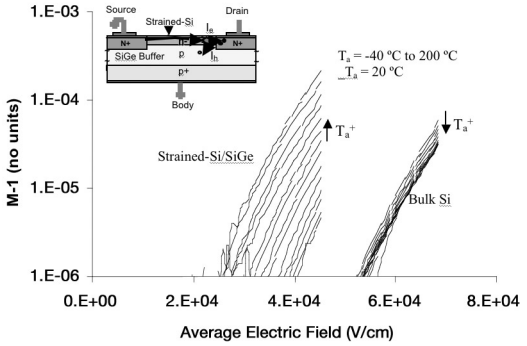

Fig. 7: Impact ionization as a function of average field and temperature for bulk and strained-Si/SiGe samples. $M = (I_s+I_b)/I_b$. II increases with temperature in the strained-Si samples, but decreases with increasing temperature in the bulk samples. Inset shows test structure.

Impact of Ion Implantation Damage and Thermal Budget on Mobility Enhancement in Strained-Si n-MOSFETs

Personnel
G. Xia (J. L. Hoyt)

Sponsorship
SRC and IBM Corp.

Strained-Si technology is a promising method to enhance MOSFET performance. It improves the carrier transport properties by introducing strain to the silicon channel. Enhanced mobility and current drive have been demonstrated in strained Si n-MOSFETs, down to the smallest channel lengths fabricated thus far (~45 nm).

As the scaling of strained-Si MOSFETs continues, the mobility enhancement is more susceptible to degradation during processing. The channel ion implant dose must be increased with scaling. In addition, the lateral damage associated with the source/drain extension regions comprises a larger portion of the channel. Both of these effects increase the possibility of loss of mobility enhancement in scaled strained-Si CMOS. Two processing techniques, ion implantation and thermal processing are of most importance. Ion implantation damage may supply point defects that assist Ge diffusion and the relaxation of strain. Thermal processing can cause strain relaxation by the formation of misfit dislocations and Ge out-diffusion. Residual ion implantation damage, remaining after annealing, may act as carrier scattering centers.

To investigate the impact of these processing factors on strain and mobility enhancement, long-channel strained-Si and bulk n-MOSFETs were fabricated with different Si and Ge implant conditions and thermal budgets. In order to avoid Coulomb scattering effects associated with ionized impurities, neutral Si and Ge were implanted into the channel at six different doses ranging from 4×10^{12} to 1×10^{15} atoms/cm^2. The ion implants were performed prior to gate oxidation. Three Rapid Thermal Annealing (RTA) splits, 1000C-1s, 1000C-10s, and 950C-10s, were used to anneal the implantation damage and activate the source/drains. After processing, effective electron mobility measurements were made using the split-CV method.

For strained-Si n-MOSFETs with implantation, the strained-Si mobility enhancement factor (compared with the universal electron mobility of bulk Si n-MOSFETs without implantation) is degraded depending upon the implant dose and RTA. At a vertical effective field of 0.75MV/cm, the mobility enhancement factor is degraded from 1.6X to 1X for Si implant dose of 5×10^{14} and 1000C-1s RTA (See Figure 8). For each RTA condition, there is a threshold implantation dose, above which the strained-Si mobility starts to degrade significantly (See Figure 9). The threshold dose is smaller for devices with higher thermal budget. For 1000C-1s RTA and Si implant doses up to 3×10^{13} cm^{-2} (damage similar to 10 KeV B, 5×10^{14} cm^{-2}) no impact on strained -Si electron mobility is seen. For 1000C-10s RTA, the Si implant threshold dose is reduced to 3×10^{12} cm^{-2} (damage similar to 10 KeV B, 7×10^{13} cm^{-2}). For bulk Si control devices with implantation, mobility is degraded by 15% at most. The residual ion implantation damage in the channel observed by cross section Transmission Electron Microscopy (TEM) indicates that the scattering by residual damage degrades the mobility. Raman spectroscopy and Secondary Ion Mass Spectroscopy (SIMS) are being performed to investigate the impact of strain relaxation and Ge diffusion on mobility degradation.

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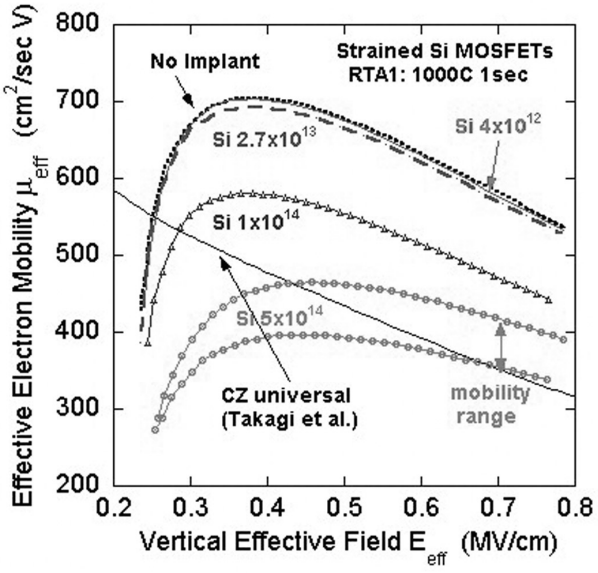

Fig. 8: The effective mobility μ_{eff} vs E_{eff} for the strained Si devices with RTA1 (1000 C for 1 sec) and different implantation conditions.

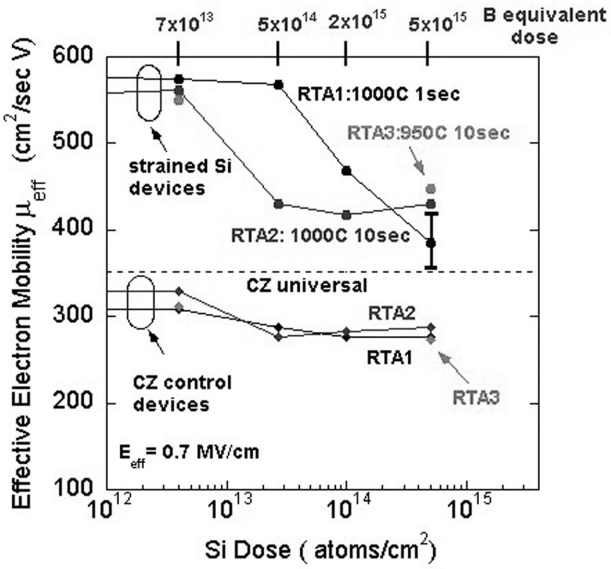

Fig. 9: The effective mobility μ_{eff} at E_{eff} = 0.7MV/cm for strained Si and CZ control devices vs. Si implant dose with different RTAs. The equivalent B doses (in terms of damage profiles) are shown above in blue.

MOSFET Channel Engineering Using Strained Si, SiGe, and Ge

Personnel

M. L. Lee (E.A. Fitzgerald)

Sponsorship

MARCO Focused Research Center on Materials, Structures, and Devices (MARCO/DARPA) and Singapore- MIT Alliance

Strained-Si (ε-Si) grown on relaxed $Si_{1-x}Ge_x$ buffers is drawing ever closer to widespread commercialization due to its ability to improve circuit performance without scaling. Holes in ε-Si show significant mobility gains, but I_d enhancements tend to vary with gate overdrive, and recent reports show that much of the performance gain is lost at the high vertical fields commonly seen in deeply scaled devices. Our work is motivated by the desire to understand hole transport in heterostructures grown on $Si_{1-x}Ge_x$ and to apply this understanding to improving performance in *p*-MOSFETs.

One of the key results from our research is the demonstration of a εSi *p*-MOSFET that exhibits much higher effective mobility in strong inversion than those previously reported. At an inversion carrier density of 1.35×10^{13} / cm^2, we observed a mobility enhancement of 2.9 times over bulk Si. We accomplished this by growing a thin (~30Å) layer of ε-Si upon a $Si_{0.3}Ge_{0.7}$ relaxed buffer. In inversion, the hole wave function is pulled towards the surface, combining the low effective mass of the Ge-rich buffer with the valence band splitting in the ε-Si cap, thus replicating the band structure of a high-mobility compressed $Si_{1-y}Ge_y$ layer. Second, instead of a single layer of ε-Si on the surface, we grew a digital alloy consisting of alternating layers of ε-Si and relaxed $Si_{0.3}Ge_{0.7}$. As the hole wave function is pulled towards the surface, the periodic nature of the digital alloy fixes the effective valence band that the hole "sees." ε-Si *n*-MOSFETs exhibit little variation in mobility enhancement with inversion strength, and the digital alloy channel allows the *p*-MOSFET to perform similarly. Figure 10 shows that mobility enhancements in ε-Si heterostructures can now be engineered to increase, decrease, or remain constant with inversion strength.

Dual-channel heterostructures, in which a Ge-rich buried layer is grown beneath the ε-Si cap, have been shown to give considerably larger hole mobility enhancements than ε-Si alone. We have demonstrated nearly symmetric mobility *p*- and *n*-type MOSFETs where ε-Si and ε-Ge are grown on a $Si_{0.5}Ge_{0.5}$ relaxed buffer (See Figure 11). Taken together, heterostructures incorporating ε-Si, ε-SiGe, and ε-Ge delineate a new scaling roadmap for MOSFET performance.

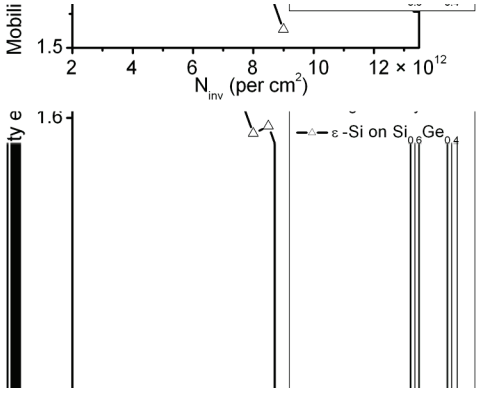

Fig. 10:

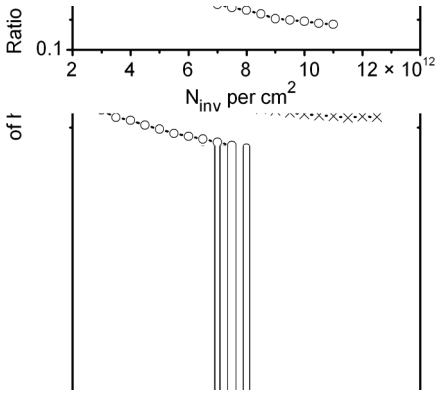

Fig. 11:

Implementation of Both NMOS and PMOS Having High Hole and Electron Mobility in Strained Si /Strained Si_{1-y} Ge_y on Relaxed $Si_{1-x}Ge_x$ (x<y) Virtual Substrate

Personnel

J. Jung and M. Lee (J. L. Hoyt, E. A. Fitzgerald, and D. A. Antoniadis in collaboration with S. Yu, Intel)

Sponsorship

MARCO Focused Research Center on Materials, Structures, and Devices (MARCO/DARPA)

Si/SiGe heterostructure with relaxed SiGe buffer layer, or virtual substrate, has potential advantages for both n-channel and p-channel MOSFET compared to the rival pseudomorphic layer structure on Si which has only PMOS benefit. Recently, high hole mobility in a strained $Si_{1-y}Ge_y$ layer on relaxed $Si_{1-x}Ge_x$ (y> x) virtual substrate was demonstrated in our group. In this work, we proposed implementing both NMOS and PMOS transistors with high electron and hole mobility in strained-Si on top of strained $Si_{0.4}Ge_{0.6}$, both grown on a relaxed $Si_{0.7}Ge_{0.3}$ virtual substrate (See Figure 12). In this structure, the buried $Si_{0.4}Ge_{0.6}$ serves as a high mobility p-channel, and the strained-Si cap serves as a high mobility n-channel. Figure 13 shows the drain current as a function of gate drive of NMOS and PMOS from our first results. It shows about 2.5 and 2.0 times enhancement in drain current of PMOS and NMOS, respectively owing to increased mobility. Ongoing work includes implementation of both NMOS and PMOS with suitable threshold voltage and subthreshold characteristics by applying metal gate or doped poly-Si, and comparison of its characteristics with Si bulk device.

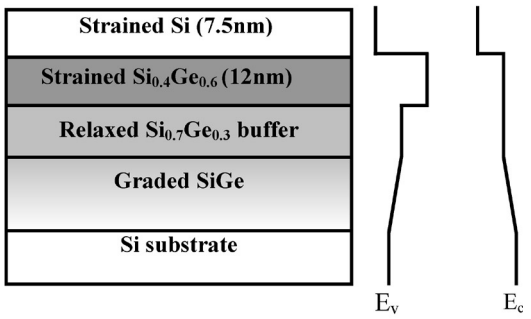

Fig. 12: Schematic CMOS layer structure and band alignment for this proposal. The buried compressively strained-$Si_{0.4}$ $Ge_{0.6}$ channel is channel for holes while the surface strained-Si is channel for electrons.

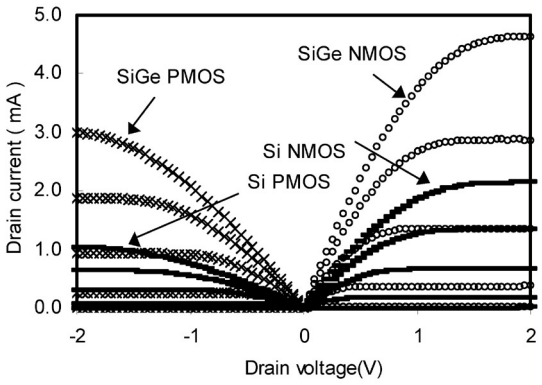

Fig.13: Drain current versus drain voltage as a function of gate drive of SiGe NMOS and PMOS transistors along with Si control device (Gate length =20μm, gate width= 213μm, and 3.8 nm-thick gate oxide). Gate overdrive starts from V_g-V_t = 0V, to |Vg-V_t| = 2V, with 0.5V step. SiGe PMOS and NMOS shows about 2.5 and 2.0 times current enhancement respectively owing to increased mobility.

RF Power CMOS

Personnel
J. Scholvin (J. A. del Alamo in collaboration with S. Parker and D. Greenberg, IBM)

Sponsorship
IBM

This project focuses on fundamental research on the RF power suitability of logic CMOS. The big questions that we wish to be able to answer are: What does it take to bring the power amplifier on chip in wireless system-on-chip applications? When does it make sense to do this?

We will answer these questions by mapping out the potential of deeply scaled standard CMOS or RF-enhanced CMOS to fulfill the RF Power Amplifier (PA) function for wireless applications. The technologies of interest are 0.25 μm and beyond (with emphasis beyond 0.18 μm), and the frequency of interest is between 2 and 10 GHz (primarily 5 GHz). This will involve both measurements of different CMOS technologies and simulations to develop good models as well as an understanding of how CMOS devices behave under large signal operation.

Over the course of the last few months, we have set up a Maury Load-pull system at MIT that allows us to measure the RF power behavior of devices up to 18 GHz (See Figure 14). The system will also be able to measure linearity (through ACPR and IM_3). Preliminary measurement results were obtained on 0.25 μm CMOS technology for 2.4, 4.8, and 7.2 GHz, as shown in Figure 15. As one would expect, the gain decreases as we move to higher frequencies. Also, the gain begins to roll off at lower power levels for higher frequencies. Because of this, the maximum possible PAE (which lies outside the measured range here) will be lower for higher frequencies.

These measurements highlight the potential of 0.25μm CMOS to perform well even at high frequencies. We are currently building models that explain in detail the behavior of the measurements and also take linearity (through IM3) into account. We are also in the process of designing 90 nm technology devices in collaboration with IBM, which should highlight the trade-offs and challenges of RF CMOS in a more dramatic way.

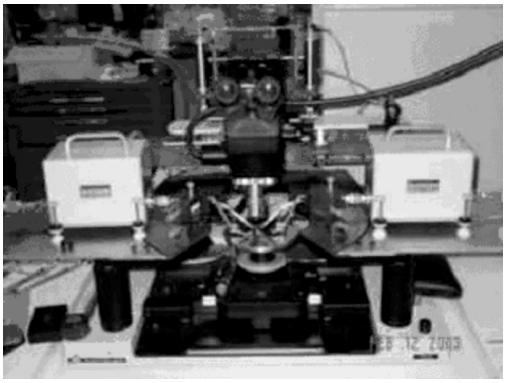

Fig. 14: Probe station and tuners of a new load-pull system assembled at MTL to carry out on-wafer RF power characterization.

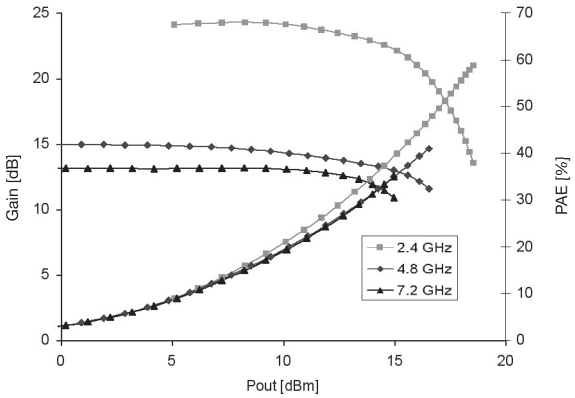

Fig. 15: Gain and Power-Added Efficiency (PAE) as a function of output power for a 300 µm wide NMOS in a 0.25 µm technology at three different frequencies.

A Metal/Polysilicon Damascene Gate Technology for RF Power LDMOSFETs

Personnel
J. G. Fiorenza (J. A. del Alamo)

Sponsorship
SRC and DARPA

RF Lateral Double-diffused Metal Oxide Semiconductor Field-Effect Transistors (LDMOSFETs) are used today at frequencies between 900 MHz and 2 GHz for a wide variety of RF power amplifier applications, including cellular handsets and base stations. In these devices, a low gate sheet resistance is essential to achieve high RF power gain while using wide gate fingers, as needed, to produce the large output power levels demanded by these applications. In order to further enhance LDMOSFET performance at these frequencies and to push the frequency limits of LDMOSFETs to the 5-6 GHz range where new applications are emerging, a new ultra-low resistance gate technology is required. This is the goal of this work.

We have developed a metal/polysilicon damascene gate technology implemented in an SOI LDMOSFET process (See Figure 16). Though promising in digital CMOS, the merits of the metal/polysilicon gate for RF power applications have never been previously demonstrated. The essential advantage of the metal/polysilicon damascene gate is that it is implemented in the back end of a fabrication process. This allows the use of metals with very high conductivity, such as aluminum or copper, enabling a gate sheet-resistance that is far lower than what can be achieved with refractory metals or refractory metal polycides, commonly used in CMOS devices. The metal/polysilicon damascene gate is also self-aligned and therefore, does not increase gate-to-source/drain overlap capacitance, as do aluminum gate strap technologies and T gates that have previously been used with LDMOSFETs.

The suitability of the metal/polysilicon damascene gate for RF power applications was evaluated by comparing the characteristics of an SOI LDMOSFET with a metal/polysilicon damascene gate to that of a co-processed SOI LDMOSFET with a degenerately-doped polysilicon gate. 0.6 μm long devices were fabricated. RF power load-pull measurements were performed at 1.9 GHz. The figure shows the gain and Power-Added Efficiency (PAE) for two typical devices with the different gate technologies. The use of the metal/polysilicon damascene gate greatly improves the gain and PAE, especially for large gate finger widths. For 90 μm finger width, as shown in the figure, the peak PAE is improved from 36% to 55%.

This work demonstrates that the metal/polysilicon damascene gate is very effective for RF power applications. It may prove to be a critical technology for enhancing RF LDMOSFET performance in present applications and for leading LDMOSFET technology to applications beyond 2 GHz.

Fig. 16: Left: sketch of fabricated RF power SOI-LDMOSFETs with metal/polysilicon damascene gate technology. Right: gain and power-added efficiency vs. output power of 0.6 µm SOI LDMOSFETs at 1.9 GHz. The use of a metal/polysilicon damascene gate greatly improves the gain and PAE of the device.

Partially- and Fully-Depleted Strained-Si/Strained-$Si_{1-y}Ge_y$ MOSFET's Fabricated on Relaxed $Si_{1-x}Ge_x$-On-Insulator (SGOI)

Personnel

Z. Cheng, J. Jung, A. J. Pitera, M. L. Lee, and H. Nayfeh (J. L. Hoyt, D. A. Antoniadis and E. A. Fitzgerald)

Sponsorship

Singapore-MIT Alliance (SMA) program, DARPA HGI program, A*STAR Fellowship

Two $Si_{1-x}Ge_x$-On-Insulator (SGOI) CMOS structures are studied: a surface channel strained-Si SGOI structure and a dual-channel (strained-Si/strained-$Si_{1-y}G_y$/relaxed-$Si_{1-x}G_x$) on SGOI structure. In a surface channel SGOI CMOS structure, the strained-Si surface channel provides mobility enhancement for both electrons and holes. To further boost hole mobility, a dual-channel structure can be utilized, where a compressively strained $Si_{1-y}Ge_y$ layer and then a tensile strained Si cap layer are grown on the relaxed $Si_{1-x}Ge_x$–On-Insulator (SGOI) substrate (y>x). The strained-Si layer is used as the electron channel layer for *n*-MOSFET's (surface channel) and the strained-$Si_{1-y}Ge_y$ is used as the hole channel for *p*-MOSFET's (buried channel). *n*- and *p*-MOSFET's SGOI structures were demonstrated in this work. The gate oxide thickness was 5 nm.

Partially depleted surface strained-Si *n*- and *p*-MOSFETs show well-behaved characteristics, with mobilities comparable to those measured on bulk relaxed SiGe virtual substrates, as shown in Figure 17. However, the measured sub-threshold swing for *fully-depleted devices* is larger than that of partially-depleted SGOI MOSFETs. This effect is related to traps at the interface between the relaxed $Si_{0.78}Ge_{0.22}$ and the buried oxide. The measured interface trap density at this bonding interface is 5.2E12 $cm^{-2}eV^{-1}$.

Dual-channel structures consisting of strained-Si/strained-$Si_{0.4}Ge_{0.6}$/relaxed-$Si_{0.7}Ge_{0.3}$ on SGOI were also fabricated. Although the hole mobility was enhanced, the enhancement was dramatically reduced for devices that received an 850C-30 min source/drain annealing step compared to those annealed at 600°C.

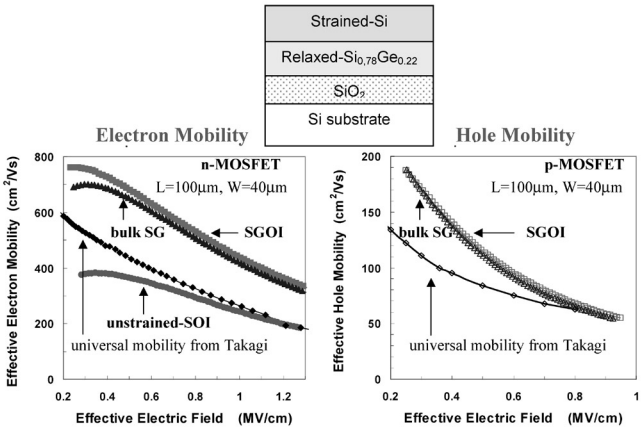

Fig. 17: Partially depleted surface strained-Si n- and p-type MOSFETs on relaxed SGOI substrates show enhanced electron and hole mobilities comparable to those measured on bulk SiGe virtual substrates (bulk SG).

InP-HEMTs for Ultrahigh-Frequency Power Devices

Personnel
T. Suemitsu (J. A. del Alamo)

Sponsorship
NTT

InP High Electron Mobility Transistors (HEMTs) exhibit highest speed characteristics in any kind of transistor. Indeed, a cutoff frequency of over 400 GHz and a maximum frequency of oscillation of over 600 GHz have been reported so far. These high-frequency characteristics are realized by means of the particular property of this material system such as the high electron mobility of InGaAs and large carrier concentration produced by the InAlAs/InGaAs quantum well. The small bandgap of InGaAs, however, leads to a large impact ionization rate at relatively low drain voltages that is regarded as a cause of low breakdown voltage of InP-HEMTs. Generally speaking, the breakdown voltage and the speed performance are a trade-off because the former decreases with, but the latter is improved by, reducing the gate length. Mitigating this trade-off is, therefore, a key issue to help the design of the ultrahigh-speed InP-HEMT circuits, particularly for high-power applications.

Although the physical mechanism of the breakdown is still under investigation, the detailed study using numerical analysis tells us that the accumulation of impact-ionized holes in the body of the device plays an important role on the breakdown. Since the device is surrounded by the n-type ohmic contacts and the semi-insulating buffer, holes are difficult to be extracted from the body of the device. This situation results in the accumulation of holes under the gate that shifts the threshold voltage of the devices. Similar effects are observed in the Silicon-On-Insulator (SOI) MOSFETs, for which the body contact is found to be an effective way to enhance the breakdown voltage.

The InP material system usually consists mainly of arsenides (InAs, GaAs, and AlAs), and it occasionally contains phosphides (InP, GaP, and AlP) for some purposes. Another group of materials, antimonides (InSb, GaSb, and AlSb), on the other hand, has a unique property from the viewpoint of band engineering. The alloys of antimonides, such as GaAsSb and AlAsSb, have relatively high valence band energy that makes the type II junction to InGaAs. The type II junction enables us to produce the quantum well for holes separated from that of electrons and to make an additional electrode to extract the holes like the body contact in SOI MOSFETs.

An approach under consideration is shown in Figure 18. The GaAsSb layer underneath the InGaAs channel acts as the hole path as shown in the band profile in Figure 19. The additional contact to the GaAsSb layer, which is an extension of the source electrode in Figure 18, prevents the impact-ionized holes from accumulating in the body of the intrinsic device.

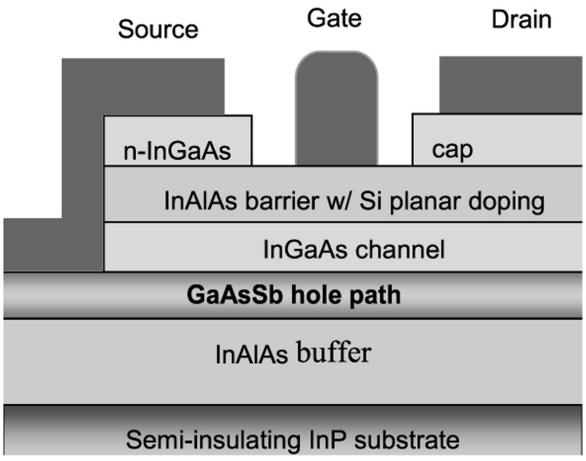

Fig. 18: Cross sectional view of InP-HEMT with hole collector.

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Hydrogen Degradation of InP High Electron Mobility Transistors

Personnel

S. D. Mertens (J. A. del Alamo in collaboration with T. Suemitsu and T. Enoki, NTT)

Sponsorship

NTT, Triquint, and ARL

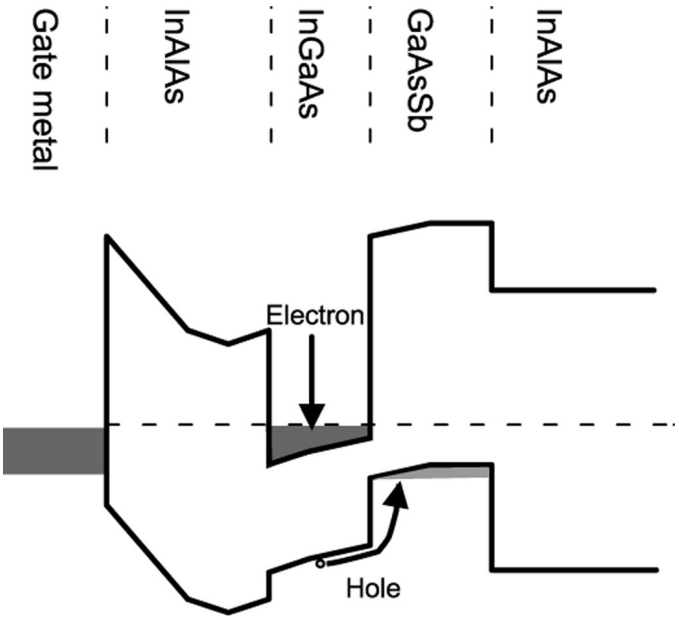

Fig. 19: Band profile of heterostructure under gate.

GaAs and InP High Electron Mobility Transistors (HEMT) hold promise for ultra-high-speed photonics and millimeter wave power-applications. A major reliability concern in some of these devices is the shift of the threshold voltage that is observed when the device is exposed to hydrogen. The goal of this project is to understand this reliability problem and find device level solutions to mitigate it.

Recent research at MIT has shown that H exposure results in the formation of TiH_x in Ti/Pt/Au gates. This produces compressive stress in the gate, which generates a tensile stress in the heterostructure underneath. The resulting piezoelectric polarization charge in the semiconductor causes a threshold voltage shift. For InP HEMTs with Ti/Pt/Au gates of short gate lengths (around 0.1 μm) shifts of several hundred mV have been observed.

In this project, we developed a model for H-induced piezoelectric effect in InP HEMTs that explains the gate length dependence of ΔV_T and provides design guidelines for minimizing H sensitivity. Our modeling approach involves: i) performing two-dimensional mechanical stress simulations in typical heterostructures, ii) computing the resulting piezoelectric charge, and iii) estimating its effect on V_T. Figure 20 shows the piezo-electric charge distribution that is induced in an InP HEMT by an expansion of its 1 μm gate. This calculation framework provides results that are consistent with the experimental measurements and illuminates the key dependencies of ΔV_T on heterostructure and gate design.

We are currently studying InAlAs/InGaAs HEMTs with a thick Ti-layer in the Ti/Pt/Au gate stack. One would expect a very large H-induced piezoelectric ΔV_T in these devices. A thick expanding layer would induce a lot of mechanical stress in the semiconductor, which would result in significant piezoelectric charge underneath

continued

continued

the gate and thus, a large ΔV_T. However, we found that the impact of hydrogen on the threshold voltage of these devices is one order of magnitude smaller than conventional Ti/Pt/Au-gate HEMTs. This can be explained if the formation of TiH_x only occurs in a thin sheet close to the Ti/Pt interface. We have confirmed this through Auger Electron Spectroscopy experiments. Our simulations are also consistent with this picture. They suggest that the separation of the expanding TiH_x-layer from the semiconductor by the thick Ti-layer significantly reduces the stress in the device heterostructure and thus ΔV_T, as is shown in Figure 20.

This work will allow us to better understand the impact of layer structure and gate design on the H-induced V_T shift in GaAs and InP HEMTs. Our ultimate goal is device design guidelines that minimize the H sensitivity of these devices.

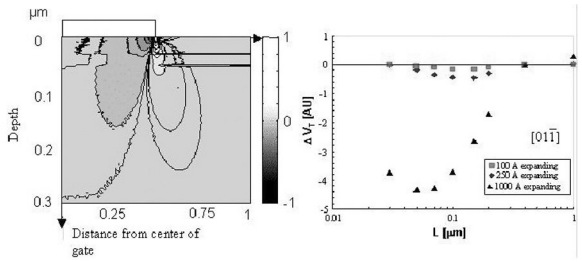

Fig. 20: The left figure shows the relative 2D piezoelectric charge distribution in a 1 μm InP HEMT stressed by an expanding gate. Only half of the device is simulated, as the other half shows a symmetric charge distribution. The right figure shows the calculated value of ΔV_T vs. gate length for an InP HEMT with a Ti/Pt/Au gate stack with a thick Ti layer. Three data sets are shown: 1) the complete Ti layer expands, 2) only the top 250 Å of the Ti layer expands' and 3) only the top 100 Å of the Ti layer expands.

Electrical Reliability of RF Power GaAs PHEMTs

Personnel

A. A. Villanueva (J. A. del Alamo in collaboration with T. Hisaka and K. Hayashi, Mitsubishi Electric)

Sponsorship

Mitsubishi Electric and Lucent Technologies Fellowship

GaAs pseudomorphic High-Electron Mobility Transistors (PHEMTs) have great potential for RF power applications. A major concern with these devices is their gradual degradation that occurs as a result of biasing the device at high voltages for extended periods of time. Although previous research has linked the electrical degradation to impact ionization and hot carrier effects, the details of the underlying physical mechanisms are not known. The goals of this research project are to provide a fundamental physical understanding of the electrical degradation in these devices, and to suggest design strategies that mitigate these effects.

In our study, experimental RF power PHEMTs (non-commercial devices provided by our sponsor, Mitsubishi Electric) were electrically stressed at room temperature. A stressing scheme that keeps the impact ionization rate constant was utilized. Specifically, this consisted of keeping the drain current I_D constant, and the intrinsic drain-to-gate voltage V_{DGo} constant (relative to the threshold voltage). In order to maximize the productivity of our experiments, the bias voltage $V_{DGo}+V_T$ was initially set at a high voltage and then stepped up in regular time periods. During stressing, the devices were characterized at frequent intervals.

Our results showed several forms of degradation; the most significant changes being in the drain resistance, the source resistance, and the threshold voltage. After initial short transients, R_D increased while R_S decreased, and V_T decreased (See Figure 21). Throughout our experiments, we have found these three phenomena to be uncorrelated with one another. In an attempt to isolate all the different degradation mechanisms involved, we also performed stressing experiments on Transmission-Line Model (TLM) structures. TLMs are much simpler devices to study degradation, since they have the same structure as a PHEMT, but do not have a gate (and thus are less complicated to characterize and analyze). Our main observations from the TLM degra-

continued

dation experiments (an initial increase in sheet carrier concentration, followed by ohmic contact degradation) were found to be correlated to corresponding mechanisms in PHEMTs.

Our general findings are that there are three independent mechanisms affecting the three regions of the device: the source, the drain, and the gate. The decrease in R_S can be explained by an increase in sheet carrier concentration on the source side. The increase in R_D can be attributed to ohmic contact degradation, and possibly a decrease in sheet carrier concentration on the drain side. The decrease in V_T can be explained by charge modulation underneath the gate—most likely, hot holes generated by impact ionization neutralizing trapped electrons in the AlGaAs layer. More experiments are being performed to identify the physical causes of these effects.

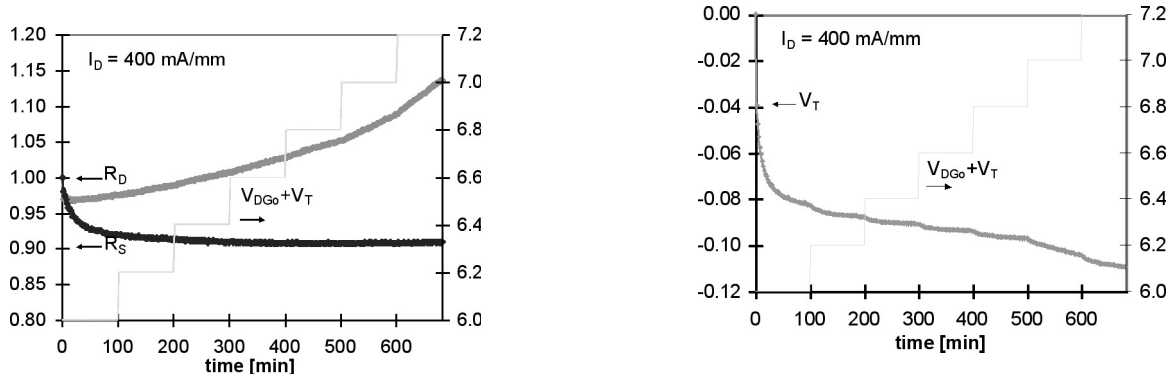

Fig. 21: Time evolution of the normalized drain resistance and source resistance (left) and change in threshold voltage (right), for a voltage step-stress experiment on a PHEMT at constant drain current of 400 mA/mm.

Coplanar Integration of Lattice-Mismatched Semiconductors with Silicon by Wafer Bonding Ge/SiGe/Si Virtual Substrates

Personnel

A.J. Pitera, G. Taraschi, M. L. Lee, C. W. Leitz, and Z. Cheng (E. A. Fitzgerald)

Sponsorship

ARO, DARPA, and Heterogeneous Integration Program

The current challenge in monolithic integration of lattice-mismatched semiconductors with CMOS is fabrication of high-quality device layers on Si substrates. Using SiGe compositional grading to pure Ge, high-quality (TDD=10^6 cm^{-2}) Ge and GaAs can be realized on a Si wafer. These virtual substrates have enabled monolithic integration of the first compound semiconductor laser and the first optical circuit on a Si substrate. More practical hetero-integration with CMOS requires removal of the thick (~10μm) graded buffer. One solution is film transfer using wafer bonding. However, traditional wafer bonding is limited to small diameter substrates due to the size mismatch between bulk Si and Ge/III-V wafers. Using Ge virtual substrates, Ge or GaAs films can be transferred to Si from large diameter wafers while eliminating the large thermal strain energy that arises during bulk wafer bonding. We have successfully transferred monocrystalline Ge films from Ge virtual substrates to Si with the aid of a SiO_2 CMP layer and the SmartCut™ process. Difficulty in CMPing thin Ge layers requires a novel approach for removal of the exfoliation-damaged Ge layer. Therefore, a buried $Si_{0.4}Ge_{0.6}$ etch-stop layer was used to selectively etch the damaged Ge surface after layer transfer. The final result is a Ge On Insulator (GOI) structure fabricated using an epitaxial Ge transfer process which takes advantage of the full wafer diameter of Si. (See Figure 22)

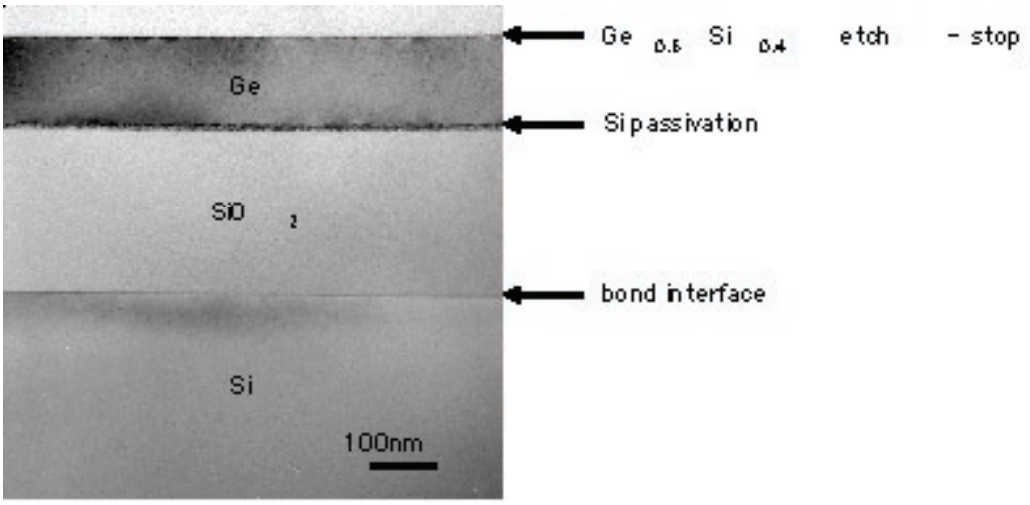

Fig. 22: Ge on Insulator (GOI) structure fabricated by wafer bonding and epitaxial layer transfer from a Ge/SiGe/Si virtual substrate.

CMOS-like Fabrication of InP-HEMTs for 100 Gbit/s Photonics Applications

Personnel
J. Knoch (J.A. del Alamo)

Sponsorship
SRC, Triquint, ARL, and IBM

InP High-Electron Mobility Transistors (HEMTs) have been shown to exhibit the fastest transistor operation of any microelectronics technology. It is believed that InP-HEMT-technology is the only one suitable for fiber optics communication systems at 100 Gbit/s operation and beyond. However, InP-HEMTs suffer from low reliability and manufacturability since the evolution of these devices has mostly been driven by millimeter-wave rather than photonics applications. This is reflected in the fact that only recently, digital ICs for 40 Gbit/s optical fiber communications systems have been demonstrated with a complexity of ~10^2 gates. On the other hand, CMOS-technology is the most advanced microelectronics technology, having achieved integration levels of order ~10^7 gates recently. Hence, it is appealing to explore the possibility of using CMOS-like process techniques for the fabrication of InP-HEMTs.

This project deals with the development of a CMOS-like, fully self-aligned process technology for InP-HEMTs that aims to achieve improved device manufacturability and reliability. In particular, fabrication techniques such as a fully planar process by means of chemical-mechanical polishing, the use of spacers for self-alignment and electroplating, play a key role in this project. Figure 23 shows a cross-section of a tentative device design. This particular design exhibits three main features: i) a shallow-trench-isolation (STI), ii) a self-aligned, high aspect ratio gate, and iii) non-alloyed ohmic contacts.

The benefits of this design are as follows: 1) the shallow-trench isolation provides for device isolation while keeping the wafer surface flat and minimizing parasitic capacitance; 2) the use of spacers allows the generation of a small gate footprint from a larger mask opening that is self-aligned to source and drain; 3) non-alloyed ohmic contacts have a smooth surface and allow well-defined contact geometries, mandatory for scaling-down the devices. As a further benefit of this device design, the gate recess region – known to cause reliability problems – is always covered.

The high manufacturability of InP-HEMTs achievable with the proposed CMOS-like device and process architecture will enable us to significantly improve the reliability, as well as, the uniformity of these devices needed in order to realize complex integrated circuits operating at 100 Gbit/s and beyond.

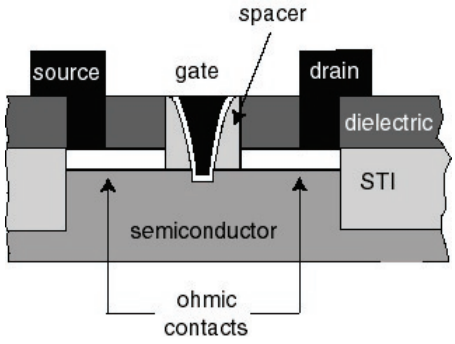

Fig. 23: Cross-sectional view of a tentative device design for an InP-HEMT fabricated using a CMOS-like process.

Nanomagnets and Magnetic Random Access Memories

Personnel

F.J. Castaño, Y. Hao, M. Walsh, D. Gil, A. Eilez, E. Lyons, and W. Jung (C.A. Ross and H.I. Smith in collaboration with F. Humphrey, M. Redjdal, Boston University, and J. Bland, Cambridge University)

Sponsorship

Cambridge-MIT Institute and NSF

We are using a variety of lithography techniques (electron-beam lithography, interference lithography, block copolymer lithography and X-ray lithography) to produce arrays of pillars, bar-shaped, and ring-shaped 'nanomagnets'. These tiny structures have thicknesses of a few nanometers and lateral dimensions typically smaller than 100 nm. Arrays of these elements are made with spatial periods of 100 nm and above. Nanomagnets have been made by electrodeposition, by evaporation and liftoff, or by etching of a sputtered film. We are exploring the switching mechanisms of the particles, the thermal stability of their magnetization, and interparticle interactions, and we are assessing their suitability for various data-storage schemes. The behavior of individual particles can be measured using magnetic-force microscopy, while the collective behavior of arrays of particles can be measured using magnetometry. Comparison of these data shows how the behavior of one magnet is affected by its neighbors, and how much intrinsic variability there is between the particles as a result of microstructural differences. We have also performed micromagnetic simulations to explore the remanent magnetic states, and mechanisms for magnetization reversal in these structures. Small particles have near-uniform magnetization states, while larger ones develop more complex structures such as magnetization vortices or domain walls. Good agreement is obtained between modelled and observed remanent states, taking the shape and crystal orientation into account. We are investigating, in particular, the behavior of multilayered nanomagnets, magnetoresistive structures, and the effects of patterning on strain in magnetostrictive films.

These nanomagnets have potential uses in 'patterned media', Magnetic-Random-Access Memories (MRAM) and other magneto-electronic applications. Current MRAM devices rely on bar-shaped multi-layered magnetoresistive nanomagnets in which a bit of data is stored, depending on the relative orientation between the magnetization of the different magnetic layers in the structure. An alternative possibility for high-density MRAMs is to use a ring-shaped nanomagnet, in which a bit of information is stored by magnetizing the ring clockwise or counterclockwise.

As an example, we have explored, for the first time, the magnetic switching mechanisms of rings with deep sub-micron dimensions (See Figure 24). The experimental results reported to date on micron-sized ring magnets support the existence of just two different magnetic states: one being the flux-closure or 'vortex' state (with clockwise or counter-clockwise magnetization) and the other a state with two domain walls, known as an 'onion' state. Unexpectedly, we found that magnetic rings with small diameters display new metastable states, called twisted states, consisting of a vortex state containing a 360° wall (See Figure 25). The existence of twisted states in nanorings has interesting consequences for the design of magnetoelectronic devices. We are measuring the magnetoresistance of these structures with the aim of incorporating them into magnetic memory or logic devices.

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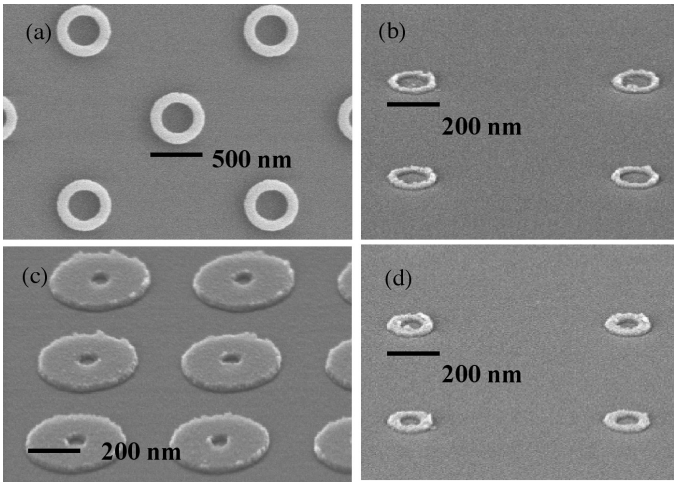


Fig. 24: Plan-view and tilted scanning-electron micrographs of four arrays of Co rings with diameters and linewidths of (a) 520 nm and 120 nm, (b) 190 nm and 30 nm, (c) 360 nm and 160 nm, (d) 180 nm and 50 nm.

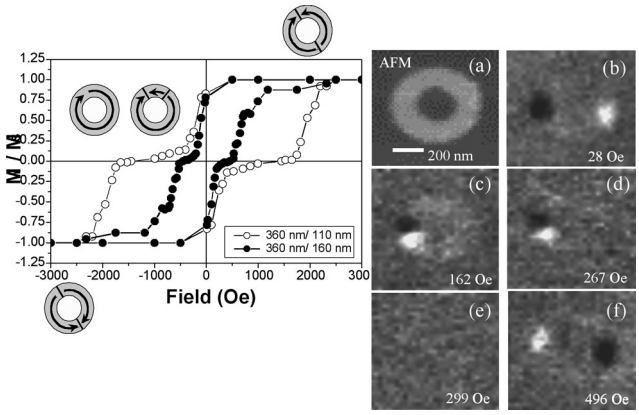


Fig. 25: At left, hysteresis loops calculated from magnetic force microscopy data, as well as a schematic representation of the different magnetic states present in Co nanorings with outer diameter of 360 nm and widths of 110 nm and 160 nm (onion state, top right and bottom left; twisted and vortex states at center). On the right, data from a 520 nm-diameter ring: (a) an atomic force micrograph. (b-f) a sequence of MFM images measured at remanence after first saturating the sample at 1000 Oe, then applying and removing a reverse field of (b) 28 Oe, (c) 162 Oe, (d) 267 Oe, (e) 299 Oe and (f) 496 Oe. After saturation, the ring is in an onion state which is characterized by dark and light contrast at opposite sides of the ring originating from the two domain walls. At a reverse field of 299 Oe, the ring 'disappears' from the image as a vortex state forms, Fig. 25(e). However, over a range of fields smaller than that needed to produce the vortex state, a new state is visible, which we call a twisted state. This state, which can be seen in Fig. 25(c) and (d), is characterized by adjacent light and dark contrast at one side of the ring. Fig 25(f) shows the reversed onion state.

AlGaAs/GaAs HBT with enhanced forward diffusion

Personnel

K. Konistis (Q. Hu and C.G. Fonstad in collaboration with M. Melloch at Purdue University)

Sponsorship

AFOSR

One of the key limits of high-frequency operation of bipolar transistors is the base transient time, which is proportional to the square of the base width when the base transport is dominated by diffusion. Consequently, high-frequency bipolar transistors tend to use thin bases (<100 nm) that result in a short base transient time and a high cut-off frequency f_T. However, for high frequency operations, it is not the current gain that matters most. Rather, it is the unilateral power gain that determines the operating frequency of any three-terminal devices. The frequency f_{max}, at which the power gain is unity, is determined by both f_T and RC time constant. Because of the peculiar geometry of bipolar transistors, the electrical contact to the base is always made from the side. Thus, a thin base, which is important to yield a high f_T, will inevitably result in a high sheet resistance and a lowering of f_{max}. It is this difficult trade-off between f_T and f_{max} that led Prof. S. Luryi and his co-workers to propose a novel heterostructure bipolar transistor, whose band diagram is shown in Figure 26.

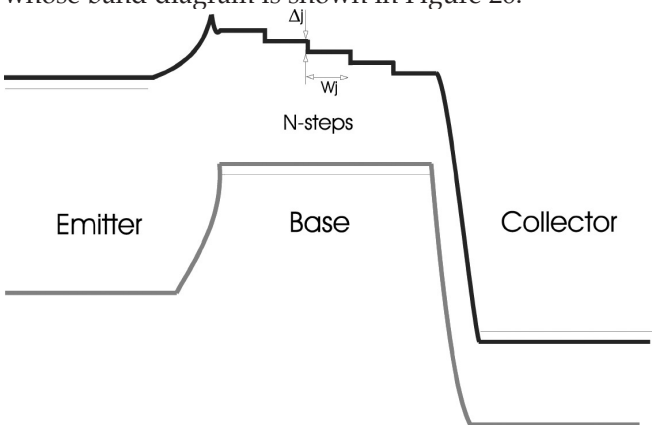


Fig. 26: Energy band diagram of an HBT with stepwise base. The energy drop Δ at each step is slightly greater than the LO-phonon energy (36 meV) in GaAs. Thus, electrons encounter very fast LO-phonon emission scattering (with a time ~0.1 ps) when they go over the edge of a step. Consequently, backward diffusion is significantly reduced and forward diffusion is enhanced.

The main feature of this novel HBT is that its base is graded like a staircase. The height of each step Δ is slightly greater than the LO-phonon energy in GaAs (36 meV). Thus, electrons will encounter very fast LO-phonon emission scattering (with a time ~0.1 ps) when they go over the edge of a step. Consequently, backward diffusion is significantly reduced. In a way, the edge of each step resembles and performs a similar function as the base-collector interface; any injected excess minority carrier will be quickly swept down the energy potential. As a result, each step acts like a minibase as far as the diffusion transport is concerned. The resulting minority carrier concentration assumes a nearly periodic distribution, provided that the energy drop is greater than the sum of LO-phonon and thermal energy to ensure a fast scattering and prohibit backward diffusion. The total base transient time is, therefore, approximately N times the transient time of each step, whose width can be as narrow as 30 nm, yielding a high f_T. On the other hand, all the N steps are connected in parallel for the base contact, reducing the base resistance by an approximate factor of N. The combination of a thin effective base and small base resistance will yield a high f_{max}.

One interesting result of our analysis is the existence of resonances of the unilateral power gain. Their physical mechanism is closely linked with the current-phase delay. A base structure introduces both phase delay and magnitude attenuation of current. As the frequency of operation increases, the phase delay increases, and at a certain frequency, the voltage and current acquire opposite phases which will yield a resonance if the amplitude attenuation is not too overwhelming. A short base offers small phase delay, and resonance occurs at high frequencies where the magnitude attenuation is strong. On the other hand, a long base may provide a large phase delay, but the heavy attenuation at low frequencies smooths out the unilateral gain peaks. For a multi-step base, the total phase delay is the sum of each step, while the total attenuation is the product of each

continued

step, enhancing the possibilities of achieving resonance. As can be seen in Figure 27, the unilateral power gain exhibits multiple resonances beyond typical cut-off frequencies (f_T) for multiple-step HBTs. These resonances can be achieved above 100 GHz, which is promising for the development of high-frequency amplifiers and fundamental oscillators.

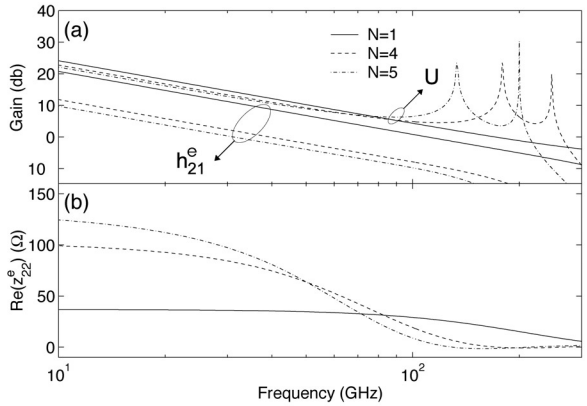


Fig. 27: (a) Unilateral power gain magnitude, current gain magnitude, and (b) output resistance for $X_{step} = 500Å$, $\Delta = 1.2\ \hbar\omega_{LO}$. As the number of steps increases (N = 1,4,5), U extends in frequency by means of resonance.

We have developed an elaborated process to fabricate very high-frequency HBTs using airbridges for electrode isolation. Figure 28 shows the schematic of the device and several SEM pictures taken from different angles. Electrical characterization of the devices will take place shortly.

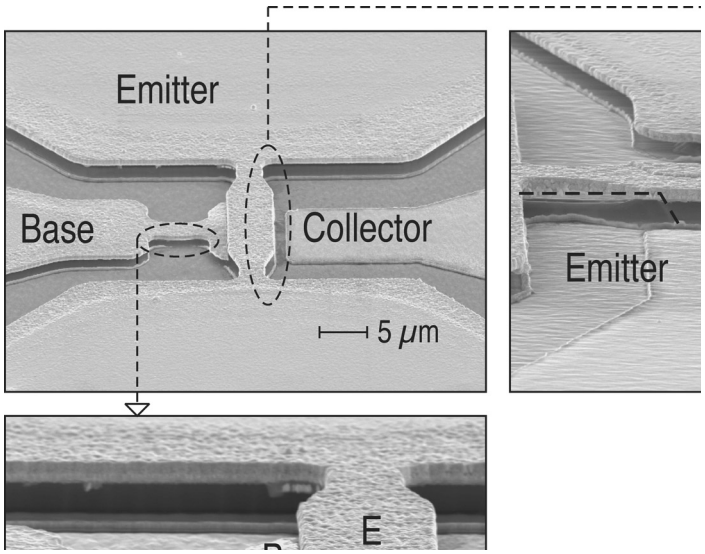


Fig. 28: Schematic and SEM pictures of a HBT device using airbridges for electrode isolation.

The MIT Microelectronics WebLab v. 5.0

Personnel

J. Hardison, D. Zych, V. Chang, and L. Hui (J. A. del Alamo)

Sponsorship

I-Campus (Microsoft)

The MIT Microelectronics WebLab (or WebLab for short) released its version 5.0 in the Spring of 2002. This latest release has been in use in educational assignments since September 2002 (See Figure 29).

WebLab allows the remote characterization of microelectronics devices using a Java applet running on a conventional web browser. Through WebLab, students from anywhere in the world and at any time of their choosing can operate an Agilent 4155B semiconductor parameter analyzer located at MIT and carry out current-voltage measurements of transistors and other semiconductor devices.

Release v. 5.0 features a new graphical interface and includes tools that simplify the management of the system in multiple courses with large numbers of students. The new graphical interface consists on a Java applet that uses the circuit language of electrical engineering to specify the experiment to be performed. This is much more intuitive than the text-based form that was utilized in previous versions of WebLab. The text-based approach, though inspired on the instrument interface, was found to be intimidating and to represent a significant barrier to first-time users. The new graphical interface hides away unnecessary details and eliminates clutter. This is also essential for the implementation of a collaboration system.

The latest release of WebLab also features a new remote management system that has been designed to allow the efficient use of the system in multiple subjects with large numbers of students. Through this system, the WebLab administrator can manage user accounts, user groups, device specifications, device access permissions, as well as examine a variety of system usage records. Additionally, the system features user self-registration and automatic e-mail notifications for users and administrators.

WebLab 5.0 was used in several courses in the Fall of 2002 and Spring of 2003 by nearly 700 students. About 280 of them were MIT students enrolled in two microelectronics subjects (120 in a junior level subject, both semesters, and 50 in a graduate subject). About 30 more graduate students used the system in an electronics materials course offered in Singapore (National Singapore University), and 350 more used in an undergraduate subject in microelectronics from Sweden (Chalmers University). About 10 additional students from industry used WebLab in various courses. In total, over 1300 students have used WebLab in lab assignments for credit since its first introduction in 1998.

The WebLab website can be found at http://weblab.mit.edu.

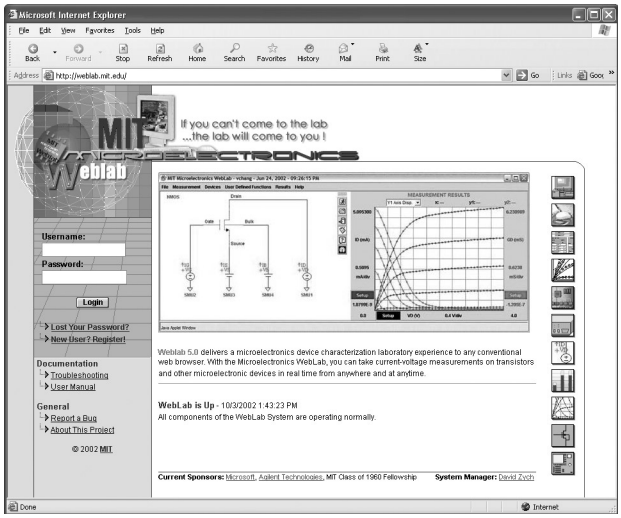


Fig. 29: Screen shot of WebLab 5.0 portal.

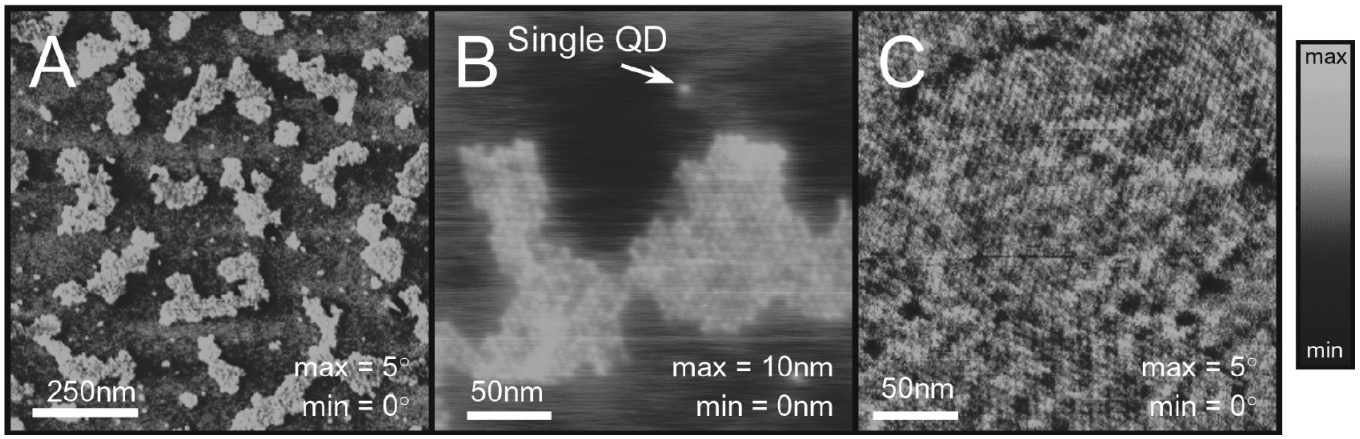
Opposite page:

AFM images showing the surface morphology of various organic/nanocrystal films. (A) Phase image of a partial monolayer of nanocrystals on top of organic thin film after phase segregation during spin-coating. Nanocrystal surface coverage is 21%. (B) Height image of a close-up of (A) showing both an island of nanocrystals as well as individual nanocrystals (QDs) on a flat organic background. (C) Phase image of a complete, hexagonally packed monolayer of nanocrystals phase segregated from the underlying organics. Grain boundaries between ordered domains of nanocrystals are observable.

Courtesy of S. Coe, J. Steckel, and W. Woo (M. Bawendi and V. Bulovic)

Sponsor:
NSF MRSEC Program, Universal Display Corporation, and the Institute for Soldier Nanotechnology (ISN)

Quantum Effect Devices



Quantum Effect Devices

- *On-Chip Oscillator Coupled to the Qubit: Design and Experiments to Reduce Decoherence*
- *Design of Coupled Qubit*
- *Thermal Activation Characterization of Qubits*
- *Type II Quantum Computing Using Superconducting Qubits*
- *Superconducting Persistent Current Qubits in Niobium*
- *Projective Measurement Scheme for Solid-State Qubits*
- *Improved Critical-Current-Density Uniformity of Nb Superconducting Fabrication Process by Using Anodization*
- *Superconducting Circuits and Quantum Computation*
- *Interaction Between Discrete Breathers and Other Non-Linear Modes in Josephson Arrays*
- *Vortex Ratchets*
- *Inorganic Quantum Dots in Organic Host Matrices for Efficient LEDs*
- *Fast On-Chip Control Circuitry*
- *Exciton Physics in Organic Optoelectronics*
- *Efficient Electrically Pumped Polariton Emission in a J-Aggregate OLED at Room Temperature*
- *An On-Chip Frequency-Domain Submillimeter-Wave Spectrometer*
- *Measurement of Qubit States with SQUID Inductance*

On-Chip Oscillator Coupled to the Qubit: Design and Experiments to Reduce Decoherence

Personnel
D. Crankshaw and B. Singh (T. Orlando)

Sponsorship
AFOSR and ARDA

The oscillator in Figure 1 is a simple, overdamped dc SQUID which acts as the on-chip oscillator which drives the qubit. This gives two parameters with which to control the frequency and amplitude of the oscillator: the bias current and the magnetic flux through the SQUID. In this design, the SQUID is placed on a ground plane to minimize any field bias from an external source, and direct injection supplies the flux by producing excess current along a portion of the SQUID loop. When a Josephson junction is voltage biased, its current oscillates at a frequency of $Vbias/\Phi_o$ with an amplitude of *Ic*. For a stable voltage bias, this looks like an independent ac current source. In this circuit, the junction is current biased, and its oscillating output produces fluctuations in the voltage across the junction. Thus the dc voltage, approximately equal to *IbiasRsh*, gives the fundamental frequency, while harmonics distort the signal. If the shunt is small, such that $Vbias >> Ic\,|\,Rsh + j\,\omega Lsh\,|$, the voltage oscillations are small relative to the dc voltage, and the higher harmonics become less of a problem. This allows us to model the junctions as independent sources (*I0* and *I1*) in parallel with the RCSJ model. A dc SQUID with a small self inductance behaves much like a single junction whose *Ic* can be controlled by the flux through its loop. The circuit model is shown in Figure 1. This is similar in concept to our previous work with Josephson array oscillators. The impedance seen by the qubit is given by placing the other elements of the circuit in parallel with the inductance. The maximum amplitude of the oscillating magnetic flux is at the resonance of the RLC circuit consisting of *Rc*, *Cc*, and *Lc*. In this case, the LC resonance occurs at 8.6 GHz. Directly on resonance, the SQUID produces high amplitude oscillations with a short dephasing time. Moving it off resonance lowers the amplitude but lengthens the dephasing time, as shown in Figure 2.

Table 1. SQUID oscillator parameters

Ic	Rn	Cj	Rsh	Lsh	Rc	Cc	Lc	Mc
260μA	7.3 Ω	2100fF	0.19 Ω	0.38 pH	0.73 Ω	4600fF	75 pH	0.6pH

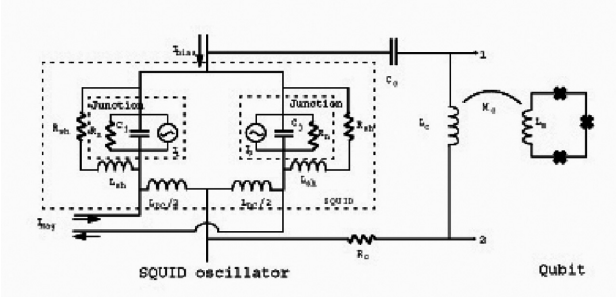


Fig 1: Circuit diagram of the SQUID oscillator coupled to the qubit. The SQUID contains two identical junctions, here represented as independent current sources and the RCSJ model, shunted by a resistor and inductor (Rsh and Lsh). A large superconducting loop (Lc) provides the coupling to the qubit. The capacitor, Cc, prevents the dc current from flowing through this line, and the resistance, Rc, damps the resonance. Zt, the impedance seen by the qubit, is the impedance across the inductor, Z12.

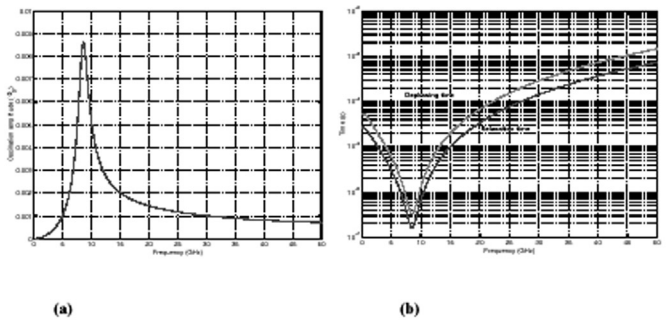


Fig. 2: Graphs showing the amplitude produced by the oscillator (a) and the decoherence times caused by the oscillator (b) as a function of frequency.

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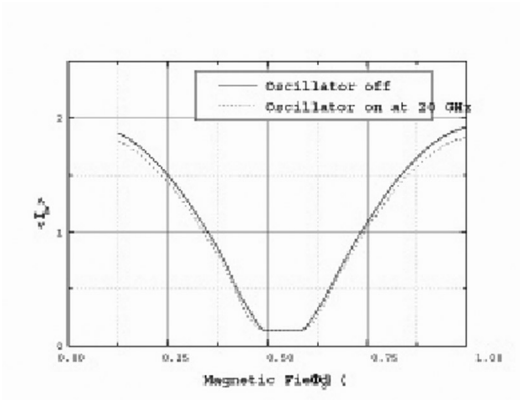

Fig. 3: This graph shows the switching current of the DC SQUID while the oscillator is off and while it is on. The current is clearly suppressed by turning the oscillator on. This oscillator has been fabricated and testing has begun. Although it is too early to comment on its effect on the qubit, it is clear that the oscillator is producing sufficient signal to suppress the current of the dc SQUID magnetometer used to measure the qubit's state, as shown in Figure 3.

Design of Coupled Qubit

Personnel

B. Singh, J. Habif, W. Kaminsky, and D. Berns
(T. Orlando and S. Lloyd)

Sponsorship

ARO and Hertz Fellowship

The main requirement for the coupled qubits is that the coupled qubit system have 4 distinguishable states corresponding to 4 properly spaced energy levels. Distinguishability here refers to the possibility of making a distinction between each of the 4 states by measurement. For a fully functioning 2-qubit quantum computer, it is necessary that the 4 qubit states that are functionally orthogonal be experimentally distinguishable. In the current design, the coupled qubits are actualized as two PC qubits weakly coupled by their mutual inductance. In the single qubit case, the DC measurement SQUID measures the state of the qubit through the flux induced by the qubit circulating current in the DC SQUID. The basic idea is unchanged for the coupled qubit system. In this case, there is one DC SQUID that measures the collective state of the coupled qubits through the total induced flux created by both qubits. For example the | 00> state could correspond to qubits 1 and 2 both having counterclockwise circulating current. In this case, the | 11> state would correspond to both qubits with clockwise circulating current. If the individual qubits were measurable with the DC SQUID, then the | 00> and | 11> states of the coupled qubit system should also be measurable because the total qubit flux induced on the DC SQUID is simply the sum of the individual qubit fluxes. The difficulty in measurement comes in differentiating the | 01> and | 10> states.

A difference in the measured flux from the | 01> and | 10> states can come from a difference in the mutual inductance between the individual qubits and the measurement SQUID and/or a difference in the magnitude of the circulating current for the two qubits. Currently, it is not practical to achieve the separation of flux states from adjusting mutual inductance values. Therefore, the approach has been to create two qubits with differing circulating current magnitudes. The magnitude of the circulating current is determined by the size of the junctions.

continued

Our analysis shows that there are 6 acceptable qubit parameter choices given the fabrication constraints for a single qubit. Since there are 2 qubits in the coupled qubit system, there are a total of 15 possible "distinct" coupled qubit combinations. Not all of these 15 possibilities are practical because some still require rather large qubit-SQUID coupling for distinguishability between the | 01> and | 10> states. The qubit-qubit and qubit-SQUID mutual inductance are parameters that can be varied through choices in geometry. As in the single qubit case, there are inherent tradeoffs in deciding on the appropriate size of the coupling. The need for properly spaced energy levels comes from the mode of operation of the qubit. The qubits will be rotated, be it individually or collectively, through RF radiation of the appropriate frequency. In the first round of experiments, the signal will come from an off-chip oscillator.

For the full functionality of the couple qubit system, it is required that there be 4 non-degenerate energy levels corresponding to the | 00, | 01, | 10, and | 11 states and that the 6 possible state transitions have sufficiently different resonant frequencies. If these conditions are met, then pulses with the appropriate linewidth would be able to do universal quantum computation on the 2-qubit system, including the "CNOT" operation. Following along the previous assumption that the coupled qubit system is accurately described as two individual qubits with weak mutual inductive coupling, it should be clear that the | 00> and | 11> states (corresponding to both qubits in the ground or excited states) should be well separated in energy. To meet the other requirements on the energy levels, the qubit-qubit mutual inductive energy needs to be sufficiently large, and the qubits need to have different junction sizes. The latter requirement is already necessitated by the measurement limitations. The former represents another tradeoff in the design, as there are problems if the coupling is too strong. Beyond the aforementioned desiderata, it is necessary that the magnitude of these resonant frequencies be practical for experiments. For the current fabrication run, there are 6 coupled qubit designs. An effort was made to span the acceptable parameter space for the tradeoffs mentioned above.

Thermal Activation Characterization of Qubits

Personnel

K. Segall, D. Nakada, D. Crankshaw, B. Singh, J. Lee, K. Berggren, N. Markovic and S. Valenzuela
(T. Orlando, L. Levitov, S. Lloyd in collaboration with M. Tinkham, Harvard)

Sponsorship

AFOSR grant funded under DURINT and ARDA

In our work, we have demonstrated two distinct measurable states of the qubit, have observed thermal activation between the two states, and have seen an effect where the measurement device acts on the qubit, an effect that we refer to as time-ordering of the measurements. The PC qubit is surrounded by a two-junction DC-SQUID magnetometer, which reads out the state of the PC qubit. The SQUID is highly underdamped, so the method of readout is to measure its switching current, which is sensitive to the total flux in its loop. A bias current Ib was ramped from zero to above the critical current of the SQUID, and the value of current at which the junction switched to the gap voltage was recorded for each measurement (See Figure 4bc). The repeat frequency of the bias current ramp was varied between 10 and 150 Hz. Typically, several hundred measurements were recorded, since the switching is a stochastic process. The experiments were performed in a pumped 3He refrigerator, at temperatures of 330 mK to 1.2 K. A magnetic field was applied perpendicular to the sample in order to flux bias the qubit near to one half a flux quantum in its loop.

The PC qubit biased near half a flux quantum can be approximated as a two-state system, where the states have equal and opposite circulating current. These two states will be labeled 0 and 1.

The circulating current in the qubit induces a magnetization into the SQUID loop equal to MIcirc, where M is the mutual inductance between the qubit and the SQUID and Icirc is the circulating current in the qubit. The two different circulating current states of the qubit cause two different switching currents in the SQUID. Without loss of generality, we can call 0 the state corresponding to the smaller switching current and 1 the state corresponding to the larger switching current. A central aspect of the measurement is that it takes a finite time to be completed. The current Ib(t) passes the smaller switching current at time t0 and the larger switching current at a later time t1 (See Fig. 1c). Measurement of state 0 occurs before measurement of state 1; this we refer to as time-ordering of the measurements. We call £n = (t1 – t0) the measurement time. Thermal activation of the system during time £n causes a distinct signature in the data and allows us to measure the thermal activation rate. The average switching current as a function of magnetic field is shown in Figure 5. The transfer function of the SQUID has been subtracted off, leaving only the magnetization signal due to the qubit. At low magnetic fields (to the left in Figure 5), the system is found only in the 0 state, corresponding to the lower switching current. As the magnetic field is increased, the system probability is gradually modulated until it is found completely in the 1 state, corresponding to the larger switching current. Focusing on the point in flux where the two states are equally likely, one can see that it is formed from a bimodal switching distribution, with the two peaks corresponding to the two different qubit states.

In Figure 5 we also show the best fit for each curve from our model. The same fitting parameters are used in both cases, with only the temperature allowed to vary. The 0.62 K curve has moved in flux relative to the 0.33 K curve, as expected. The theory predicts both the curve's shape and its relative position in flux. We use this agreement to fit the parameters of our system. There are three fitting parameters for the model to fit the data: EJ, α and Q. EJ is the Josephson energy for each of the two larger junctions in the three-junction qubit, which, for a given current density, is proportional to their physical size. The parameter α is the ratio of the smaller junction to the two larger ones, as previously mentioned. The damping factor Q is associated with thermal activation from the 1 to the 0 state in equation (3). The value of EJ which best fits the data is 4000 μeV. This corresponds to a size of about 0.52 μm x 0.52 μm for each of the two larger junctions. The values of α were found to be 0.58, corresponding to a smaller junction size of

continued

0.39 μm. These values are quite reasonable given the fabrication of our junctions. The larger junctions are lithographically 1 μm in length, while the smaller junctions are lithographically 0.9 μm; however, the fabrication process results in a sizing offset of between 0.4 and 0.55 μm, measured on similar structures.

The value of Q is found to be 1.2x106, with an uncertainty of about a factor of 3, given the sources of error in the measurement and the fitting. This value corresponds to a relaxation time of roughly α£s0 ~ 1 μs. Similar relaxation times have been measured in aluminum superconducting qubits and indicate possible long coherence times in the quantum regime. The value of 106 is consistent with a subgap resistance of 10 MΩ measured in similar junctions. The inferred relaxation time is also consistent with the calculated circuit impedance. This inferred value of Q is important for the long-term prospects of our qubits, as it indicates that it is possible to obtain very low dissipation in our structures.

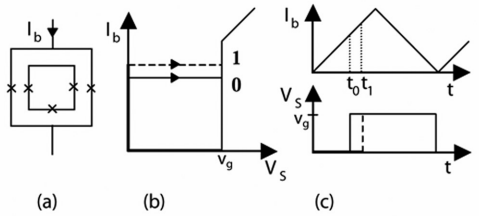

Fig. 4: (a) Schematic of the PC qubit surrounded by a DC SQUID. The X's represent junctions. (b) Schematic curve of the bias current (Ib) vs. the SQUID voltage (Vs) for the SQUID. At the switching point the SQUID voltage switches to the gap voltage vg. The 0 and 1 qubit states cause two different switching currents. (c) Timing of the current and voltage in the SQUID as the measurement proceeds. If the qubit is in state 0, Vs switches to vg at time t0; if the qubit is in state 1, Vs switches at time t1. The time difference t1-t0 forms a timescale for the measurement.

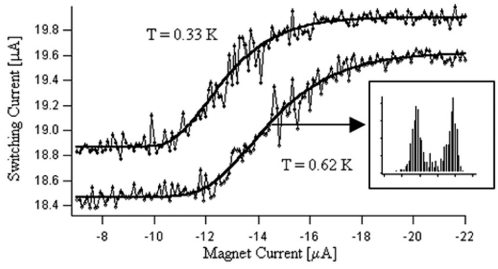

Fig. 5: Switching current versus magnetic field for device A for bath temperatures of T = 0.33 K and T = 0.62 K. The 0.33 K curve is intentionally displaced by 0.3 μA in the vertical direction for clarity. The model (equation (7)), with fitted temperature values of 0.38 K and 0.66 K, fits the data well, describing accurately the dependence of both the location of the midpoint of the transition and the shape of the transition on the device temperature. Inset shows a histogram for a flux bias where the system is found with equal probability in either state. The distribution is bimodal, showing the two states clearly.

Type II Quantum Computing Using Superconducting Qubits

Personnel

T. P. Orlando in collaboration with D. Berns, K. K. Berggren and J. Sage, Lincoln Laboratory, and J. Yepez, Air Force Laboratories)

Sponsorship

AFOSR funded under the Department of Defense and Defense University Research Initiative on Nanotechnology (DURINT)

Most algorithms designed for quantum computers will not best their classical counterparts until they are implemented with thousands of qubits. By all measures, this technology is far in the future. On the other hand, the Factorized Quantum Lattice-Gas Algorithm (FQLGA) can be implemented on a type II quantum computer, where its speedups are realizable with qubits numbering only in the teens. The FQLGA uses a type II architecture, where an array of nodes, each node with only a small number of coherently coupled qubits, is connected classically (incoherently). It is the small number of coupled qubits that will allow this algorithm to be of the first useful quantum algorithms ever implemented.

The algorithm is the quantum mechanical version of the classical lattice-gas algorithm, which can simulate many fluid dynamic equations and conditions with unconditional stability. This algorithm was developed in the 1980's and has been a popular fluid dynamic simulation model ever since. It is a bottom-up model where the microdynamics are governed by only three sets of rules, unrelated to the specific microscopic interactions of the system. The quantum algorithm has all the properties of the classical algorithm but with an exponential speedup in running time.

We have been looking into the feasibility of implementing this algorithm with our superconducting qubits, with long-term plans of constructing a simple type II quantum computer. We currently have a chip scheme to simulate the one dimensional diffusion equation, the simplest fluid dynamics to simulate with this algorithm. The requirements are only two coupled qubits per node, state preparation of each qubit, only one $\pi/2$ pulse, and subsequent measurement. This can be accomplished with two PC qubits inductively coupled, each with a flux bias line next to it (initialization), and each with a squid around it (measurement), with a tunable (frequency and amplitude) oscillator on-chip next to the two qubits (transformation). All classical streaming will, at first, be done off-chip.

Superconducting Persistent Current Qubits in Niobium

Personnel

Y. Yu, K. Segall, D. Nakada, D. Crankshaw, B. Singh, J. Lee, B. Cord, K. Berggren (MIT), N. Markovic and S. Valenzuela (Harvard) (T. Orlando, L. Levitov, S. Lloyd in collaboration with M. Tinkham, Harvard)

Sponsorship

AFOSR, funded under the Department of Defense and Defense University Research Initiative on Nanotechnology (DURINT) and by ARDA

Quantum Computation is an exciting idea whose study combines the exploration of new physical principles with the development of a new technology. In these early stages of research, one would like to be able to accomplish the manipulation, control, and measurement of a single two-state quantum system while maintaining quantum coherence. This will require a coherent two-state system (a qubit) along with a method of control and measurement.

Superconducting quantum computing has the promise of an approach that could accomplish this in a manner that can be scaled to large numbers of qubits. We are studying the properties of a two-state system made from a niobium (Nb) superconducting loop, which can be incorporated on-chip with other superconducting circuits to perform the control and measurement. The devices we study are fabricated at Lincoln Laboratory, which uses a Nb-trilayer process for the superconducting elements and photolithography to define the circuit features. Our system is, thus, inherently scalable, but has the challenge of being able to demonstrate appreciable quantum coherence.

The particular device that we have studied so far is made from a loop of Nb interrupted by 3 Josephson junctions (See Figure 6a). The application of an external magnetic field to the loop induces a circulating current whose magnetic field either adds to (say circulating current in the clockwise direction) or opposes (counterclockwise) the applied magnetic field. When the applied field is near to one-half of a flux quantum, both the clockwise and counterclockwise current states are classically stable. The system behaves as a two-state system. The potential energy versus circulating current is a so-called double-well potential (See Figure 7), with the two minima representing the two states of equal and opposite circulating current.

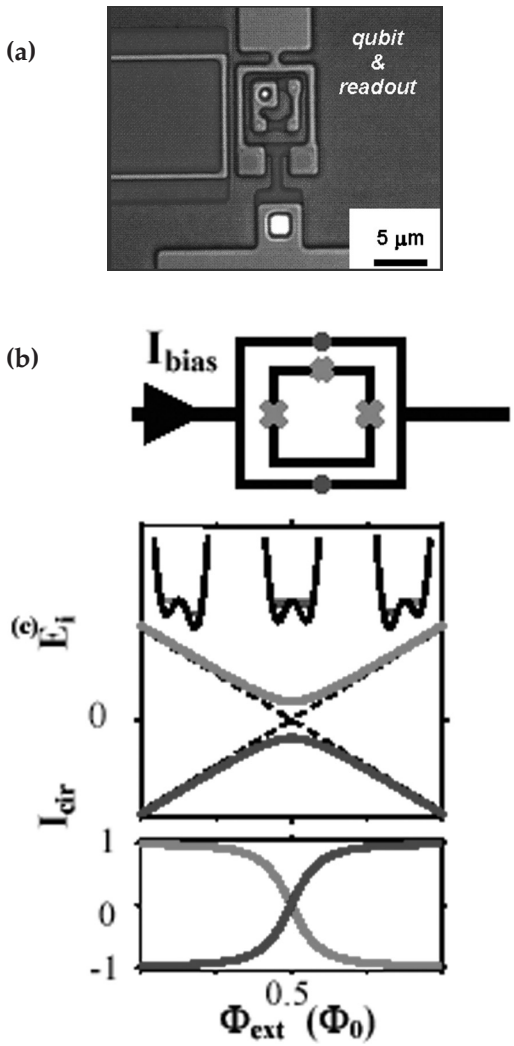

Fig. 6. (a) SEM image of the persistent current qubit (inner loop) surrounded by the measuring dc SQUID. (b) a schematic of the qubit and measuring SQUID, the x's mark the Josephson junctions. (c) The energy levels for the ground state (dark line) and the first excited state of the qubit versus applied flux. The double well potentials are shown schematically above.

continued

continued

The lower graph shows the circulating current in the qubit for both states as a function of applied flux. The units of flux are given in terms of the flux quantum.

Figure 6a shows a SEM image of the persistent current qubit (inner loop) and the measuring dc SQUID (outer) loop. The Josephson junctions appear as small "breaks" in the image. A schematic of the qubit and the measuring circuit is shown in Figure 6b, where the Josephson junctions are denoted by x's. The sample is fabricated at MIT's Lincoln Laboratory in niobium by photolithographic techniques on a trilayer of niobium-aluminum oxide-niobium wafer.

The energy levels of the ground state (dark line) and the first excited state (light line) are shown in Figure 6c near the applied magnetic field of 0.5 Φ_o in the qubit loop. Classically, the Josephson energy of the two states would be degenerate at this bias magnetic field and increase and decrease linearly from this bias field, as shown by the dotted line. Since the slope of the *E* versus magnetic field is the circulating current, we see that these two classical states have opposite circulating currents. However, quantum mechanically, the charging energy couples these two states and results in a energy level repulsion at Φ_{ext} = 0.5 £X0, so that there the system is in a linear superposition of the currents flowing in opposite directions. As the applied field is changed from below Φext = 0.5 Φ0 to above, we see that the circulating current goes from negative to zero at Φext = 0.5 Φ_o, to positive as shown in the lower graph of Figure 1c. This flux can be measured by the sensitive flux meter provided by the dc SQUID.

A SQUID magnetometer inductively coupled to the qubit can be used to measure the magnetic field caused by the circulating current and thus, determine the state of the qubit. The SQUID has a switching current which depends very sensitively on magnetic field. When the magnetic field from the qubit adds to the external field, we observe a smaller switching current; when it subtracts from the external field, we observe a smaller larger current. We measure the switching current by ramping up the bias current of the SQUID and recording the current at which it switches. Typically, a few hundred such measurements are taken. We have performed these measurements versus magnetic field, temperature, and SQUID ramping rate.

In the upper plot of Figure 7, we show the average switching current versus magnetic field for our qubit-SQUID system. The SQUID switching current depends linearly on the applied magnetic field. A step-like transition occurs when the circulating current in the qubit changes sign; hence, changing whether its magnetic field adds to or subtracts from the applied field. In Figure 6, the qubit field adds to the SQUID switching current at lower fields (< 3mG), but subtracts from it at higher fields (>3mG). Each point in the upper curve is an average of 1000 single switching current measurements. If we look at a histogram of the 1000 switching currents in the neighborhood of the transition, we discover that it represents a joint probability distribution.

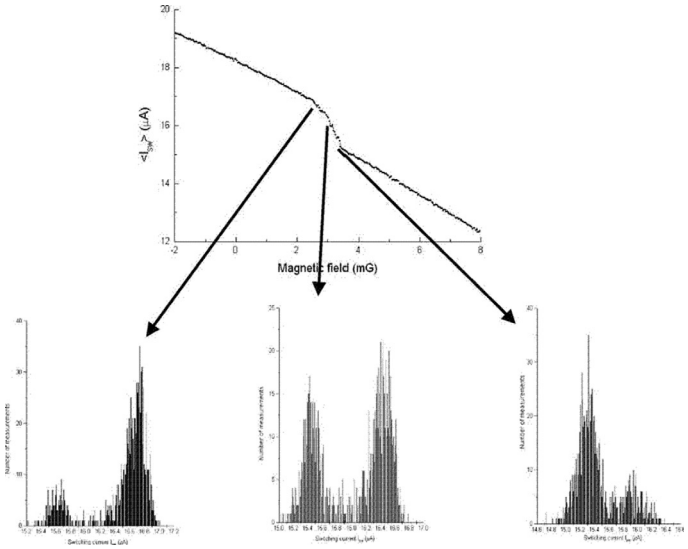

Fig. 7: Measurements of the switching current of the SQUID versus magnetic field.

continued

Two distinct switching currents representing the two states of the qubit can be clearly resolved. Changing the magnetic field alters the probability of being measured in one state or the other. In Figure 8, we show the potential energy for the system as we sweep through the transition. (We used a different assignment for "zero" field in Figure 8 than Figure 7, which is why the step occurs at a different magnetic field value). In the first part of the transition, the system has a higher probability of being measured in the left well, which corresponds to the circulating current state which adds to switching current of the SQUID. At the midpoint of the transition, the system is measured in both wells with equal probability. At higher fields the system has a larger probability of being measured in the right well. The mechanism for the system to move between the wells at these temperatures (>300 mK) is thermal activation. We have measured the system at lower temperatures, and there the mechanism is unclear. The focus of our future efforts is to determine if the mechanism changes to quantum mechanical tunneling at lower temperatures and how coherent the tunneling can be. If we are successful, that will be the first indication that superconducting quantum computers in Nb are possible.

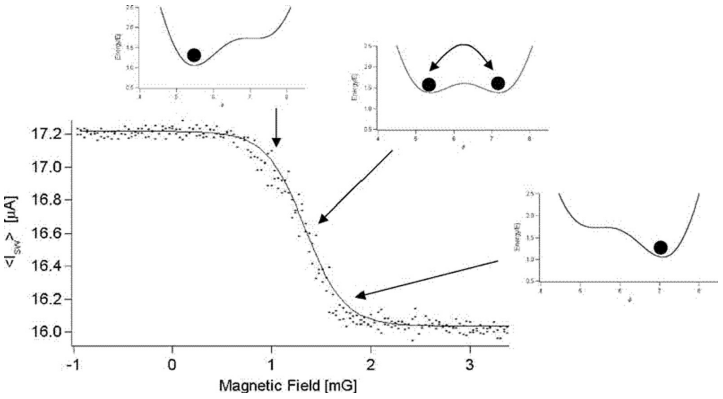

Fig. 8: Switching current versus magnetic field with the background field of the SQUID subtracted off.

Projective Measurement Scheme for Solid-State Qubits

Personnel

L. Tian (S. Lloyd and T. P. Orlando)

Sponsorship

Department of Defense University Research Initiative on Nanotechnology (DURINT)

Effective measurement for quantum bits is a crucial step in quantum computing. An ideal measurement of the qubit is a projective measurement that correlates each state of the quantum bit with a macroscopically resolvable state. In practice, it is often hard to design an experiment that can both projectively measure a solid-state qubit effectively and meanwhile, does **not** couple environmental noise to the qubit. Often in solid-state systems, the detector is fabricated onto the same chip as the qubit and couples with qubit all the time. On the one hand, noise should not be introduced to the qubit via the coupling with the detector. This requires that the detector is a quantum system well-isolated from the environment. On the other hand, to correlate the qubit states to macroscopically resolvable states of the detector, the detector should behave as a classical system that has strong interaction with the environment, and at the same time interacts with the qubit strongly. These two aspects contradict each other, hence, measurements on solid-state quantum bits are often limited by the trade-off between these two aspects. In the first experiment on the superconducting persistent-current qubit (pc-qubit), the detector is an under-damped dc SQUID that is well-isolated from the environment and behaves quantum mechanically. The detected quantity of the qubit, the self-induced flux, is small compared with the width of the detector's wave packet. As a result, the detector has very bad resolution in the qubit states. This is one of the major problems in the study of the flux-based persistent-current qubits. Various attempts have been made to solve the measurement problem. We present a new scheme in Figure 9 that effectively measures the pc-qubit by an on-chip detector in a "single-shot" measurement and does not induce extra noise to the qubit until the measurement is switched on. The idea is to make a switchable measurement (but a fixed detector) that only induces decoherence during the measurement. During regular qubit operation, although the qubit and the detector are coupled, the detector stays in its ground state and only induces an overall random phase to the qubit. The measurement process is then switched on by resonant microwave pulses. First, we maximally entangle the qubit coherently to a supplementary quantum system. Then, we measure the supplementary system to obtain the qubit's information.

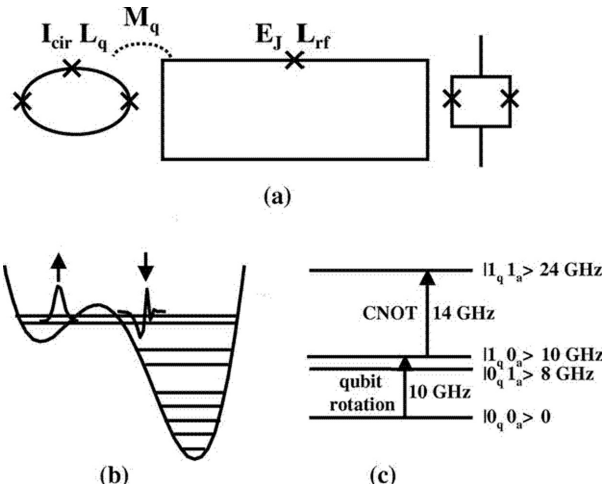

Fig. 9: (a). The circuit for the measurement scheme, from left to right: the qubit, the rf SQUID and the dc SQUID magnetometer. The pc-qubit couples with the rf SQUID via the mutual inductance M_q. (b). Energy levels of rf SQUID with its potential energy when biased at f_{rf} =0.4365 flux quantum. The effective two-level systems (ETLS) are labeled with arrows and their wave functions are shown. (c). The states of the interacting qubit and the rf SQUID. The energies are in units of GHz.

Improved Critical-Current-Density Uniformity of Nb Superconducting Fabrication Process by Using Anodization

Personnel

D. Nakada, K. K. Berggren, and E. Macedo (T. P. Orlando and B. Cord in collaboration with W. Oliver, Lincoln Laboratories)

Sponsorship

DOD, ARDA, ARO, and AFOSR

We developed an anodization technique for a Nb/Al/AlO*x*/Nb superconductive-electronics fabrication process that results in an improvement in critical-current-density *Jc* uniformity across a 150-mm-diameter wafer. The superconducting Josephson junctions studied were fabricated in a class-10 cleanroom facility at MIT Lincoln Laboratory. The Nb superconducting process uses optical projection lithography, chemical mechanical planarization of two oxide layers, a self-aligned via process, and dry Reactive Ion Etching (RIE) of the Nb and oxide layers. The most critical step in the fabrication process, however, is the definition of the tunnel junction. The junction consists of two Nb layers, the Base Electrode (B.E.) and Counter-Electrode (C.E.) separated by a thin AlO*x* barrier. Fig. 10a shows a cross-section of the Josephson junction region after RIE is performed on the counter-electrode. After RIE, the junction region could be vulnerable to chemical, plasma and/or other damage from subsequent processing steps; we, therefore, anodized the wafer to form a 50-nm-thick protective metal-oxide layer around the junction perimeter. Anodization is an electrolytic process in which the surface of a metal is converted to its oxide form; this metal oxide layer serves as a protective barrier to further ionic or electron flow. Figure 10b shows that after anodization the junction region is "sealed" from the outside environment by a thick NbO*x* layer. Anodization is useful in minimizing damage to the junction region. We also used Transmission Electron Microscopy (TEM) images to inspect the anodic film (Figure 11a, b and Figure 12).

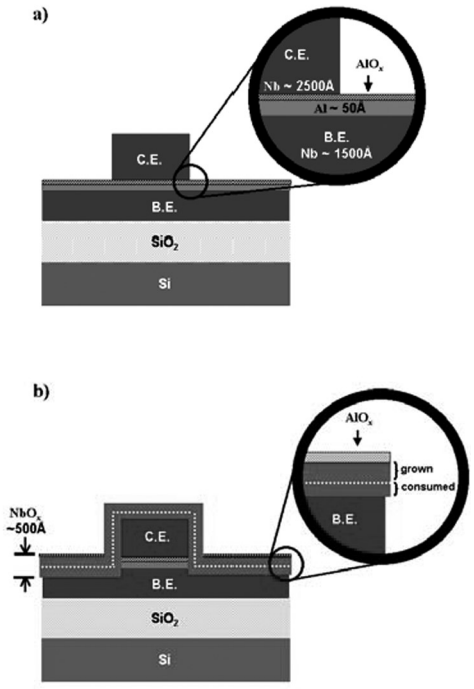

Fig. 10: a) Nb Josephson junction after Counter-Electrode (C.E.) etch but immediately prior to anodization. Inset shows thin AlOx barrier vulnerable to outside environment. b) Junction region after anodization. The surface of the counter and Base-Electrode (B.E.) is converted to a metal oxide layer approximately 500Å thick. The dotted line shows the original surface. Inset shows amount of anodic oxide grown and consumed. The anodic oxide causes the surface to swell up and out slightly during growth.

This work was sponsored by the Department of Defense under the Department of the Air Force contract number F19628-00-C-0002. Opinions, interpretations, conclusions and recommendations are those of the author and are not necessarily endorsed by the Department of Defense.

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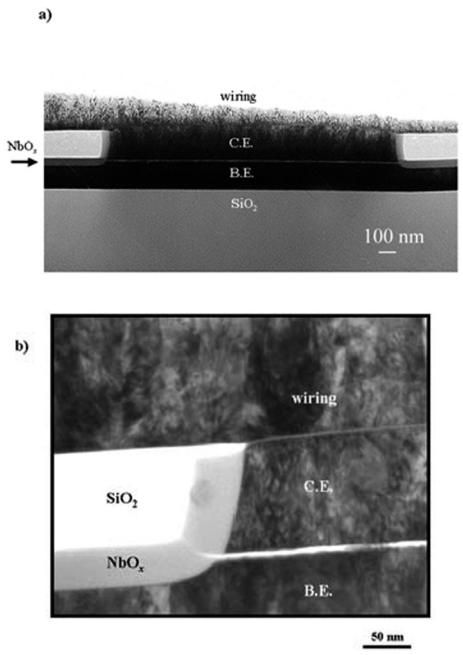

Fig.11: a) TEM image of an anodized junction showing clearly the sealing of the junction edge by NbOx. Note the clean interface between the counter-electrode and wiring layer where the NbOx has been removed by CMP. b) TEM image shows AlOx barrier within the NbOx layer. Critical current Ic measurements of Josephson junctions were performed at room temperature using specially designed test structures. We used an automatic probing station to determine the Ic values of junctions distributed across an entire wafer. We then compared the Jc uniformity of pairs of wafers, fabricated together, differing only in the presence or absence of the anodization step. The cross-wafer standard deviation of Jc was typically ~ 5% for anodized wafers but > 15% for unanodized wafers (Fig. 3). Overall, unanodized wafers had a factor of ~ 3 higher standard deviation compared to anodized wafers. A low variation in Jc results in a higher yield of device chips per wafer with the desired current density. As a result of the improved cross-wafer distribution, the cross-chip uniformity is greatly improved as well; typically < 1% for anodized chips. Control of Jc is important for all applications of superconductive electronics including quantum computation and rapid single-flux quantum (RSFQ) circuitry.

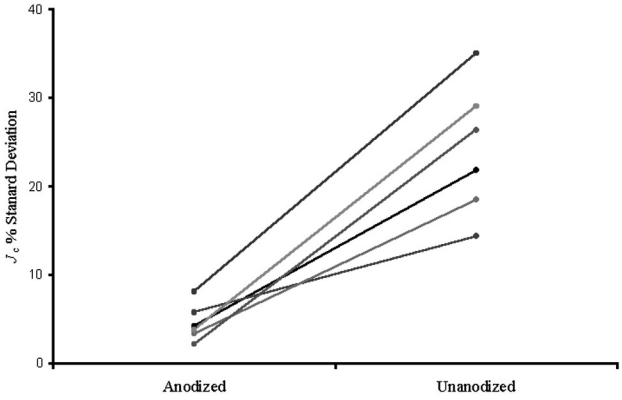

Fig. 12: Comparison of cross-wafer critical-current-density standard deviation of anodized/unanodized wafer pairs. The wafers shown have Jc values ranging between 102A/cm2 and 103A/cm2. Lines connect data points on wafers whose trilayers were deposited together.

Superconducting Circuits and Quantum Computation

Personnel

D. S. Crankshaw, D. Nakada, L. Tian, J. Lee, B. Singh, D. Berns, W. Kaminsky, B. Cord, M. Kota, A. Cough, Y. Yu, and K. J. Segall (T. P. Orlando, L. Levitov, S. Lloyd, J. E. Mooij in collaboration with J. Mazo, F. Falo, (University of Zarragossa), K. K. Berggren, W. Oliver (Lincoln Laboratories), M. Tinkham, N. Markovic, S. Valenzuela, (Harvard University), M. Feldman, M. Bocko, J. Habif, (University of Rochester, and E. Trais (Cadence, Inc))

Superconducting circuits are being used as components for quantum computing and as model systems for non-linear dynamics. Quantum computers are devices that store information on quantum variables and process that information by making those variables interact in a way that preserves quantum coherence. Typically, these variables consist of two quantum states, and the quantum device is called a quantum bit or qubit. Superconducting quantum circuits have been proposed as qubits, in which circulating currents of opposite polarity characterize the two quantum states. The goal of the present research is to use superconducting quantum circuits to perform the measurement process, to model the sources of decoherence, and to develop scalable algorithms. A particularly promising feature of using superconducting technology is the potential of developing high-speed, on-chip control circuitry with classical, high-speed superconducting electronics. The picosecond time scales of this electronics means that the superconducting qubits can be controlled rapidly on the time scale, and the qubits remain phasecoherent.

Superconducting circuits are also model systems for collections of coupled classical non-linear oscillators. Recently, we have demonstrated a ratchet potential using arrays of Josephson junctions as well as the existence of a novel non-linear mode, known as a discrete breather. In addition to their classical behavior, as the circuits are made smaller and with less damping, these non-linear circuits will go from the classical to the quantum regime. In this way, we can study the classical-to-quantum transition of non-linear systems.

Interaction Between Discrete Breathers and Other Non-Linear Modes in Josephson Arrays

Personnel

K. Segall and J. J. Mazo (T. P. Orlando)

Sponsorship

NSF and Fulbright/MEC Fellowship

Linear models of crystals have played a fundamental role in developing a physical understanding of the solid state. However, many phenomena are unexplained until one considers non-linear interactions. One particularly interesting phenomena is that of *discrete breathers*, which are time periodic, spatially localized modes. In a crystal, a discrete breather is localized in that a few atoms are vibrating while the neighboring atoms stay still. Josephson junctions are a solid state realization of non-linear oscillators, and they can experimentally be coupled in various ways using standard lithographic fabrication techniques. In Figures 13A and 13B, we show a regular array of Josephson junctions, denoted by x's, which are driven by a uniform current (driving current not shown). Each junction is governed by equations isomorphic to a damped pedulum; the phase of the pendula is equivalent to the superconducting phase difference across the junction. A discrete breather is shown in 13B, where a few of the junctions have their phases rotating in time while the others do not. Experimentally, a rotating phase corresponds to a net DC voltage, which can be easily measured. Breathers in Josephson arrays have been studied in previous work in our group here at MIT.

In Figure 13A, we demonstrate another kind of non-linear mode, a *moving vortex*. This is mathematically equivalent to a kink or solitonic mode. Vortices in Josephson arrays carry a quantum of magnetic flux and have been studied extensively in superconducting systems. A vortex corresponds to a 2π phase shift in the phases of the vertical juntions in the ladder; when a uniform current is applied, the vortex moves down the ladder. As the vortex passes a given junction, it causes its phase to undergo a rotation and thus create a voltage. This is indicated by the time sequence shown in Figure 13A. Our work is aimed at studying the interaction of discrete breathers with other kinds of non-linear modes, like a moving vortex. Such questions are of fundamental importance for the Non-linear Dynamics community. In Figure 14, we show a mathematical simulation of a

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collision between a vortex and a breather. The vertical axis is the junction number in the array; the array in the simulation has 60 junctions. The horizontal axis is time. The color indicates the junction voltage or rotation speed, with blue indicating low voltage and red indicating high voltage. Initially, there is a breather located about junction 10 and a vortex located in junction 45. As time proceeds, the vortex moves toward the breather and eventually collides with it. The result of the collision is that the breather acts as a pinning center for the vortex. As time proceeds further, (not shown) the vortex will eventually depin and cause the breather to decay into a different mode. We have also seen other collision scenarios in our simulations, such as ones where the breather is destroyed or where the breather pins a train of moving vortices. We are also looking for such behavior experimentally, with fabricated junction arrays and DC electronics.

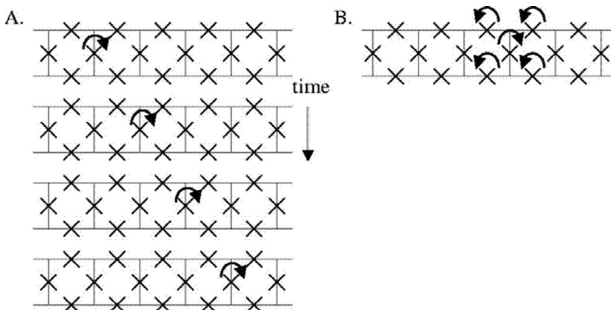

Fig. 13: Representation of two different non-linear modes in a Josephson Ladder: (a) Moving vortex: The vortex causes the phase of a junction to rotate as it passes by. (b) Discrete breather: A few junctions have their phases continually rotating while the neighboring ones do not.

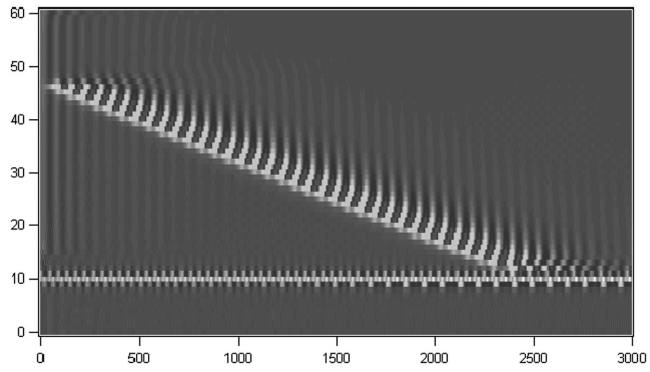

Fig. 14: Interaction of a breather with a moving vortex. Time (in arbitrary units) is on the horizonal axis, the junction number is on the vertical axis, and the color indicates the junction voltage (red=high, blue=low). The vortex starts in junction 45 and moves toward the breather, which is in junction 10. The vortex collides with the breather and is pinned by it, with the breather surviving at later times.

Vortex Ratchets

Personnel
K. Segall and J. J. Mazo (T. P. Orlando)

Sponsorship
NSF and Fulbright/MEC Fellowship

The concepts of a *ratchet* and of the *ratchet effect* have received attention in recent years in a wide variety of fields. Simply put a ratchet is formed by a particle in a potential which is asymmetric, i.e. it lacks reflection symmetry. An example is the potential shown in Figure 15, where the force to move a particle trapped in the potential is larger in the left (minus) direction and smaller in the right (plus) direction. The ratchet effect is when net transport of the particle occurs in the absence of any gradients. The transport is driven by fluctuations. This can happen when the system is driven out of equilibrium, such as by an unbiased AC force or non-gaussian noise.

Ratchets are of fundamental importance in biological fields for study of dissipation and stochastic resonance, in mesoscopic systems, and in our case in superconducting Josephson systems. The key question is to study how the ratchet potential affects the transport of the particle. In our group, we study the ratchet effect in circular arrays of superconducting Josephson Junctions. In such arrays, magnetic vortices or kinks can be trapped inside and feel a force when the array is driven by an external current. The potential that the vortex feels is given by a combination of the junction sizes and the cell areas; by varying these in an asymmetric fashion, we can construct a ratchet potential for a vortex. The picture in Figure 15 is of one of our fabricated circular arrays; the potential shown in Figure 15 is the numerically calculated potential for a kink inside the array. We have verified the ratchet nature of the potential with DC transport measurements, as published in early 2000.

This work is now moving in the quantum direction: smaller junction arrays where quantum effects are important. A quantum ratchet will display new behavior as the temperature is lowered, as both the ratchet potential and quantum tunneling can contribute to the kink transport. We have designed and fabricated such arrays and are presently testing them. The experiment we conduct in these newer devices is to measure the switching current, which is the current that is required to cause the vortex to depin and the system to switch to a running mode or finite voltage state. In the mechanical analog, it represents the critical force to move the particle, and in a ratchet potential it is different in one direction than the other. For a classical ratchet, the direction with the lower critical force will always have the larger depinning rate. However, in a quantum ratchet the direction with the lower transition rate will depend on the temperature. A crossover in the preferred direction, the direction with the larger depinning rate, is the signature of possible quantum behavior. In Figure 16, we show the switching current as a function of temperature for the two directions. A crossover is clearly seen. We are in the process of doing further experiments and calculations to verify that we have truly made a quantum ratchet.

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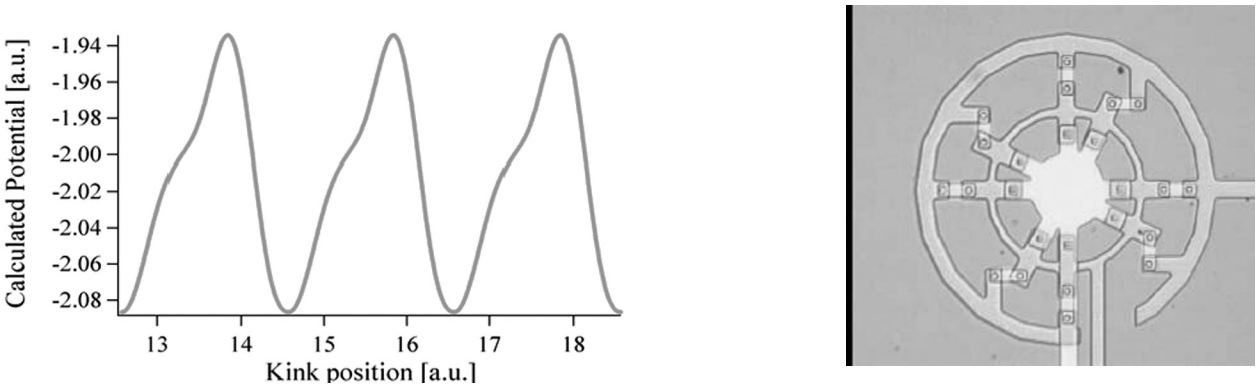

Fig.15: A ratchet potential and its realization in a Josephson array. The array has alternating junction sizes and plaquete areas to form the asymmetric potential for a vortex trapped inside the ring. The outer ring applies the current such that the vortex transport can be measured. The potential is numerically calculated for the array parameters.

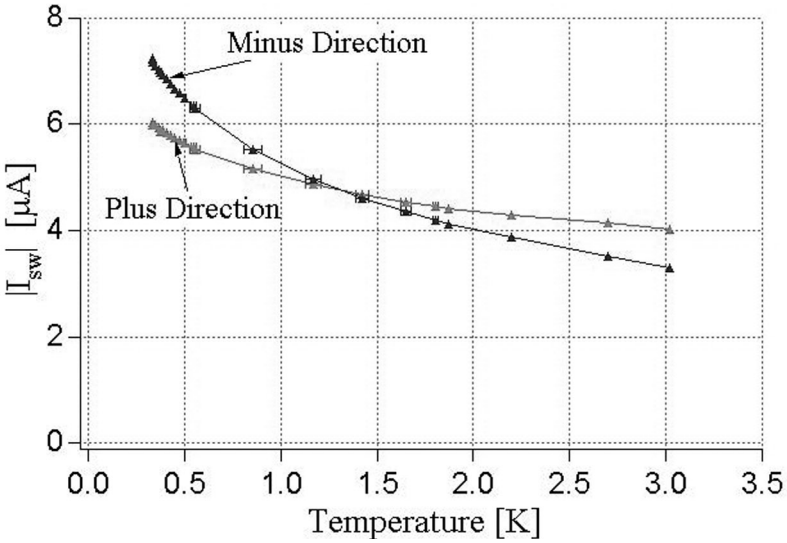

Fig. 16: Switching current for the plus and minus direction of a circular, 1-D Josephson array fabricated in the quantum regime. The switching current is a measure of the depinning rate in each direction. The crossover indicates that the preferred direction changes as a function of temperature. This is a possible signature of quantum effects.

Inorganic Quantum Dots in Organic Host Matrices for Efficient LEDs

Personnel

S. Coe, J. Steckel, and W. Woo (M. Bawendi and V. Bulovic)

Sponsorship

NSF MRSEC Program, Universal Display Corporation, and the Institute for Soldier Nanotechnology (ISN)

We recently demonstrated the first efficient hybrid organic/inorganic Light Emitting Devices (LEDs), with saturated color emission, whose performance reaches that of the all-organic LED technology (See Figure 17) [Coe *et al.*, Nature 420, 800 (2002)]. The hybrid LEDs are large-area, efficient light emitters consisting of luminescent inorganic nanocrystals (quantum dots) embedded in organic LED structures. They represent a completely new technology platform for development of the flat-panel displays and the flat-panel lighting. Their greatest benefit is in the ease of tuning their saturated emission color across the visible spectrum (by changing the size of the nanocrystal), and in their potentially longer operating lifetimes as compared to the all-organic LEDs.

(a) CdSe Quantum Dots

Nanocrystal Quantum Dots (QDs) are semiconductor nanoparticles that are chemically synthesized using simple benchtop techniques. Their sizes can be precisely controlled in a range from 1 to 10 nanometers. Electrons and holes are delocalized in QDs in states that are reminiscent of atomic wavefunctions. The energy of these states is strongly size-dependent: emission from CdSe QDs can be tuned across the entire visible spectrum by changing the size of the nanocrystals. Nanocrystal QDs can be synthesized with narrow size distributions so that the bandwidth of the emission can be < 30 nm. The dots are grown in organic solvents. Their surface is covered with a ligand shell that can be easily exchanged, giving the dots the potential for broad chemical and electronic flexibility (See Figure 17). The combination of broad spectral tunability and chemical flexibility make nanocrystal QDs ideal chromophores for opto-electronic applications in organic/inorganic hybrid structures such as QD-LEDs.

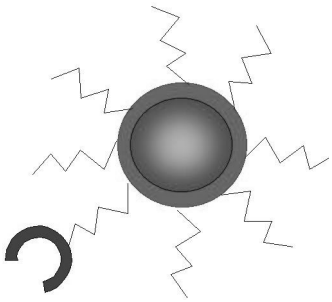

Fig. 17: Schematic of a QD showing an optically active core, a protective inorganic shell, an organic ligand shell, with one of the ligands functionalized.

QDs have unique advantages over other classes of common (small molecule or inorganic phosphor) chromophores. The emission wavelength of a QD depends on its size, and can be controlled by varying the diameter of the particle. The excitation band is very broad, requiring only that the excitation light, or energy tranfered excitations be above the band gap of the semiconductor; and it is independent of the emission, so that the same energy can be used to excite QDs with different emissions. A size series of QDs represents a family of fluorophores with different emissions that can be excited with the same light source. Furthermore, QDs are significantly less susceptible to photobleaching than dye molecules, making them ideal candidates as the chromophore in organic/inorganic hybrid structures. The energy level structure of QDs also differs substantially from most organic chromophores. The emission from QDs is from a lowest transition that is thought to be partly spin forbidden, leading to long (10-100 nsec) emission lifetimes at room temperature (and microseconds at cryogenic temperatures). The density of states above this emissive state becomes dense with both spin allowed (equivalent to singlet states of organics) and spin forbidden states (equivalent to the triplet states in organics). This high density of states should make QDs ideal in both Förster and Dexter transfer schemes of coupling excitons from organics to the QD.

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(b) Performance of Layered Structures Containing QDs
The demonstration of quantum dot LEDs (QD-LEDs) is a direct result of a cross-disciplinary merge of the nanocrystal chemistry of Prof. Bawendi's lab and Prof. Bulović's lab expertise in the development of active organic optoelectronics. The devices incorporate CdSe nanocrystals in a molecular organic host via spin-on deposition of solvated materials. Spin-casting results in the formation of an organic/nanocrystal bilayer film due to the alkyl/phenyl phase segregation, where by alkyl-coated nanocrystals form a densely packed single monolayer on top of the conjugated organic film (See Figure 17 and device cross section in Figure 20). The devices are completed by thermally evaporating thin organic films and a metal cathode on top of the organic/nanocrystal layers. These first devices operate with a quantum efficiency of 0.4%; they have a saturated color, and brightness of 1500 cd/m^2 at current density of 120 mA/cm^2, corresponding to luminescence efficiency of 1.25 cd/A, as compared to the best previous results for nanocrystal-LEDs of 600 cd/m^2 at 1 A/cm^2, corresponding to 0.06 cd/A.

The remarkable 20-fold improvement in the electroluminescence efficiency of our QD-LEDs is attributed to the optimized device structures and improved photoluminescence efficiency and chemical stability of nanocrystals. The technologically innovative step of generating the self-assembled nanocrystal monolayer through phase segregation allows us to position the nanocrystals in the recombination zone of the multilayer active organic EL device. Their confinement to the device active region maximizes the efficiency of nanocrystal usage. Furthermore, the use of alkane/phenyl phase segregation to create spin-cast heterostructures provides a new general method for the fabrication of organic or hybrid devices.

The layer design of our QD-LEDs deliberately isolates the role of QDs in the luminescence processes from their participation in charge conduction by containing only a single monolayer of QDs within the structure. The organic layers transport charge carriers to the vicinity of the QD monolayer from which the luminescence originates. This is in contrast to previous studies that utilized QD multilayer films, on the order of 10-20 layers thick, which had the dual function of both transporting electrons and serving as the emissive layer. Poor conduction through these QD multilayers lead to an injected charge imbalance, and consequently, luminescence efficiency of these early devices never exceeded 0.10 cd/A. Furthermore, a high density of pinhole defects in QD multilayers resulted in low device yields and inconsistent device performance. These technological shortcomings are avoided in our new structures that use only a single monolayer of QDs as the emissive layer. High device yields and consistent LED performance are standard for our devices.

(c) Charge Transport and Energy Transfer in Hybrid Structures
Generation of excitons on QDs in our LED structures occurs via two parallel processes: direct charge injection and exciton energy transfer from organic molecules (See Figure 20). For direct charge injection, electrons may be trapped at the QDs due to the relative energy alignment of the Lowest Unoccupied Molecular Orbital (LUMO) levels of the electron transporting organic layer (Alq_3) and the QDs (see the energy diagram in Figure 19). For these charged QDs the barrier to hole injection from the hole transporting organic (TPD) is reduced. Upon acceptance of holes from TPD, excitons form on the QDs and can subsequently recombine radiatively. Alternatively, excitons can be formed on organic molecules that are near grain boun-daries, interstitial spaces, and voids in the single QD mono-layer. These excitons can then energy transfer to the lower energy QD sites, where they recombine radiatively.

In this program, we are studying the relative importance of the direct charge injection in comparison to energy transfer

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processes for exciton generation on QDs. For example, by increasing the thickness of the shell structure of the dot, we can preferentially inhibit the short range charge tunneling processes into the dot (See Figure 19). The longer range (up to 50 Å transfer radius) Förster energy transfer is still be able to take place. Similarly, we are able to evaluate relative importance of Auger processes in quenching the emission of the QDs.

The quantum dot structure strongly affects the QD-LED performance. For example, the semi-log plot of the spectral emission intensity as a function of drive current is shown in Figure 21 for (a) ZnS coated CdSe nanodots and (b) uncoated CdSe nano-dots. Synthetic step for the coating process is indicated in the inset. In both cases, dots are surrounded by organic ligands to facilitate solvation in the organic solvent during the spin-on process. Both plots in Figure 20 show a strong luminescence peak at 570 nm corresponding to the nanodots emission, but we also observe a long luminescence tail form 700 to 950 nm. This emission is due to the luminescence form deep traps (mid-gap states) caused by dangling bonds on the surface of the nanodots. Trap luminescence is very inefficient and is more pronounced in uncoated dots. This typically results in several-fold lower efficiency of uncoated devices as has been previously observed in the PL spectra of the nanodots. The progression of luminescence as a function of device current indicates that for the coated-nanodot devices (See Figure 21) (a), luminescence of deep traps stays constant as the luminescence form the nanodots increases with current. For uncoated-dot devices, deep trap luminescence rises with current together with the dot luminescence. This is as expected: the small number of defect levels in the coated-dot devices is first populated at lower currents, and then, the luminescence form the confined states of the dot can start as the current is increased. The number of defect states on uncoated dot devices is significantly larger and cannot be filled completely even at higher device currents, so its luminescence steadily increases with the increase in current.

We are also interested in tailoring exciton generation processes and exciton energy transfer under electrical pumping conditions in the hybrid thin films.

Electrically generated excitons in organic materials can be of either singlet and triplet type, with their ratio corresponding to their spin multiplicities. In contrast, excited states of QDs mix the spin-triplet and spin-singlet exciton characteristics. In other material systems, such mixed states facilitate capture of both singlet and triplet excitons on the lumophore. Rapid exciton recombination that follows can lead to nearly 100% internally quantum efficienct LEDs. It remains an open question as to whether or not analogously efficient exciton harvesting is possible in QD-LEDs.

The fundamental limits of QD-LED performance are different than those of all organic LEDs. The discrete energy structure of QDs gives rise to a narrow emission spectrum, which in our electroluminesent devices is as small as 32 nm at full-width-half-maximum (FWHM). In contrast, molecular organic LEDs have a typical FWHM of between 50 and 100 nm, although emission of some polymers and phosphorescent molecules was shown to be as narrow as 26 nm FWHM but with long, low energy tails. The vibrational structure of structurally flexible organics typically generates broad single molecule emission spectra at room temperature. The same is not true of the rigid, covalently bonded inorganic QD, for which single QD spectroscopy shows that the fundamental FWHM linewidth at room temperature is 14 nm with a symmetrical, gaussian shape. It is the combination of spectral diffusion and size distribution of QDs in a specific sample that yields further line broadening. However, it is reasonable to expect that current techniques in QD preparation and processing could yield QD-LED line widths that

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are as narrow as 25 nm, a feat that has already been accomplished in solution. Such true color saturation would benefit applications where efficient production of narrowband light is desired. In particular, the creation of high luminous efficiency red and blue LEDs requires both high external quantum efficiency as well as narrowband emission, to prevent the bulk of emission from occurring in the infrared or ultraviolet, respectively, where our eyes have minimal response.

With the demonstrated improvement in the luminescent power efficiency of QD-LEDs, we still have not reached the fundamental limits of device performance in both quantum efficiency and color saturation. We expect that with our development of the new methods for growth of QD-films in vacuum, higher material purity will be obtained. Performance of such vacuum-grown QD-LEDs could match and potentially exceed that of conventional organic thin-film LEDs, resulting in durable, integratable, highly-efficient light sources of nano-scale thickness. By changing the diameter of the CdSe core from 22 to 65Å, the peak luminescence wavelength can be precisely tuned from l=470 nm to l=640 nm with a typical spectral full width at half of maximum of less than 35nm. Figure 22 shows the electroluminescence spectra of a series or visible and infra-red emitting QD-LEDs. Such broadly tunable, saturated color emission of quantum dots is unmatched by any class of organic chromophores. Furthermore, environmental stability of covalently bonded inorganic nanocrystals suggests that device lifetimes of hybrid-LEDs should match or exceed that of all-organic LEDs.

(d) QD Monolayer Formation via Material Phase Segregation

QD-LEDs demonstrate that sheets of single QD monolayers, square centimeters in size, can be employed in electrically active devices. This minimizes QD material use to the active device region. The material phase segregation that governs formation of the organic/QD spin-cast thin film bilayers is a general and, we expect, widely applicable fabrication process. The process is governed by the physical size and chemical character of the two solvated constituents; the organic molecules in our devices are small (~1 nm) and have aromatic character, while the QDs are large in comparison (>3 nm) and present a surface that consists of mostly alkane chains. In general, phase segregation is not limited to aromatic/aliphatic pairs, but governs the interaction between any pair of materials with disparate chemical functionality. To date, the phase segregation phenomenon has been observed in spin cast solutions of (CdSe)ZnS core-shell/TOPO capped QDs and PbSe/oleic acid capped QDs with both α-NPD and TPD in chloroform and chlorobenzene.

(e) Infra-Red QD-LEDs

We also demonstrate large area (mm^2 in size) infrared electroluminescent devices using colloidally grown PbSe quantum dots (QDs) in organic host materials (See Figure 23). By changing the QD size, the electroluminescence is tuned from 1.33 μm-1.56 μm with a full width at half maximum of <160 nm (< 0.11 eV). This represents only a portion of the accessible QD tuning range, as the lowest energy optical absorption peak of our PbSe solutions can be tuned from 1.1 eV (corresponding to wavelength λ = 1.1 μm and 2.6 nm diameter QDs) to 0.56 eV (λ = 2.2 μm, 9.5 nm diameter). Such large area emitters in the near infrared have been identified as technologically useful for chemical spectroscopy and sensing, night vision applications, and could be incorporated into an on-chip optoelectronic integrated circuit.

PbSe is a convenient choice for inorganic semiconductor QDs for NIR applications (λ > 1 μm), as the colloidal synthesis is reproducible and yields highly monodisperse nanocrystals. In addition, the exciton Bohr radius is large (46 nm), leading to strong confinement of QD excitons throughout the synthetically accessible range of 2 nm to >10 nm

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(corresponding to absorption peaks $\lambda = 1.0\ \mu m$ (1.2 eV) to >2.4 μm (<0.5 eV), respectively). Figure 23(a) shows typical absorption and emission spectra for 5.0±0.5 nm diameter PbSe QDs, while Figure 22(b) depicts an ordered layer of 4.0±0.5 nm diameter QDs imaged by high resolution transmission electron microscopy, showing their highly crystalline structure in the inset. The NIR EL spectrum of QD-LEDs closely resembles the PL spectrum of the corresponding QD solution (see Figure 23(a)). The tunability of QD-LED emission as a function of the QD diameter is shown in Figure 21(a), with EL spectral peaks at 1.33, 1.42, 1.50, and 1.56 μm. The FWHM of all four devices is <160 nm (< 0.11 eV). The devices also have an emission peak at 530 nm (not shown) due to exciton recombination within the Alq_3 ETL (or 405 nm corresponding to TPD EL when BCP is used as the ETL). We note that the InGaAs photodiode array used to record all of these spectra has low detection efficiency for λ >1.6 μm, modifying the apparent shape of the 1.56 μm emission peak.

The electrical characteristics of all the QD-LEDs of this study are similar, with a linear (J) versus voltage (V) dependence for V<3 V, and power law dependence, $J \propto V^9$, when light is emitted. This is consistent with the properties of an Alq_3/TPD device, though the operating voltage is a few volts higher, possibly due to QD charge trapping or interface dipole realignment. The PbSe QD-LED NIR external quantum efficiency is measured to be 0.001%, using a Silicon wafer to filter out visible emission from organic EL. The visible emission originates from Alq_3 and TPD and has an external EL quantum efficiency of 0.1-0.3%. These QD-LEDs demonstrate the feasibility of generating controllably tunable λ >1.3 μm EL in a large area device, and give us a starting point in the creation of higher efficiency devices in the spectral range of 1.2 $\mu m < \lambda < 2.2\ \mu m$.

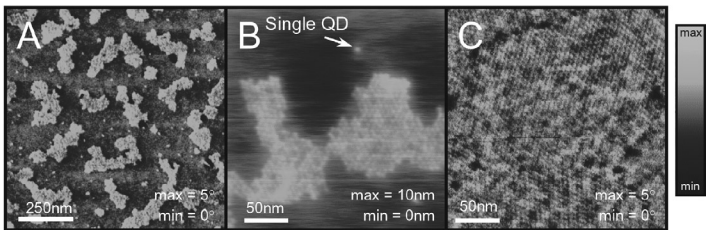

Fig. 18: AFM images showing the surface morphology of various organic/nanocrystal films. (A) Phase image of a partial monolayer of nanocrystals on top of organic thin film after phase segregation during spin-coating. Nanocrystal surface coverage is 21%. (B) Height image of a close-up of (A) showing both an island of nanocrystals as well as individual nanocrystals (QDs) on a flat organic background. (C) Phase image of a complete, hexagonally packed monolayer of nanocrystals phase segregated from the underlying organics. Grain boundaries between ordered domains of nanocrystals are observable.

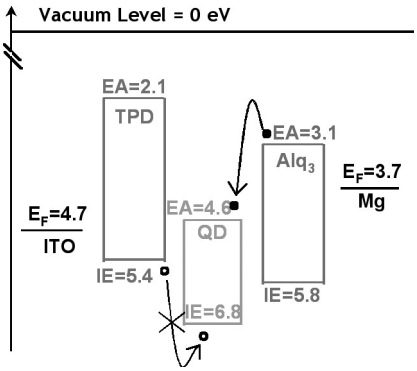

Fig. 19: Proposed energy level diagram of device in Fig. 18. Values for ionization energy (IE) of all materials except QDs are taken from photoemission spectroscopy measurements1. Electron affinity levels (EA) were then calculated using optical absorption data. QD levels shown are from calculated values

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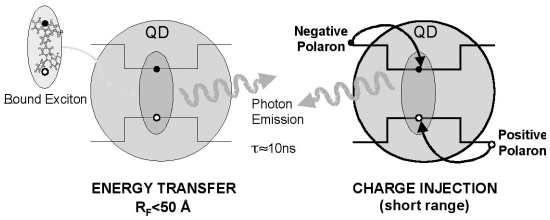

Fig. 20: Excited states of QDs can be generated by either direct charge injection or exciton transfer from an organic material. Determining the relative importance of the two processes will be essential in optimizing QD-LEDs

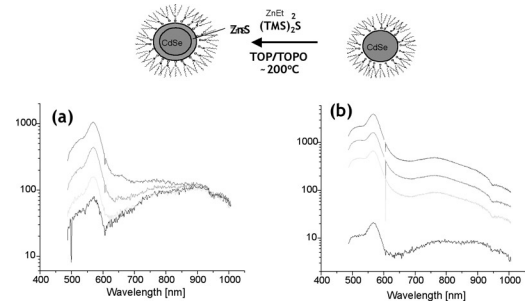

Fig. 21: Electroluminescence spectra as a function of current of HOI-LED with structure drawn in the inset of Fig. 1 and containing (a) ZnS coated CdSe nanodots and (b) uncoated CdSe nanodots. Current increases from 0.1 to 2 mA from the bottom to the top of both plots

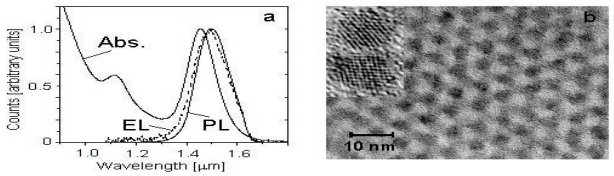

Fig. 22: Electroluminescence spectra from the visible to the near infrared of (left) CdSe and (right) PbSe based QD-LEDs.

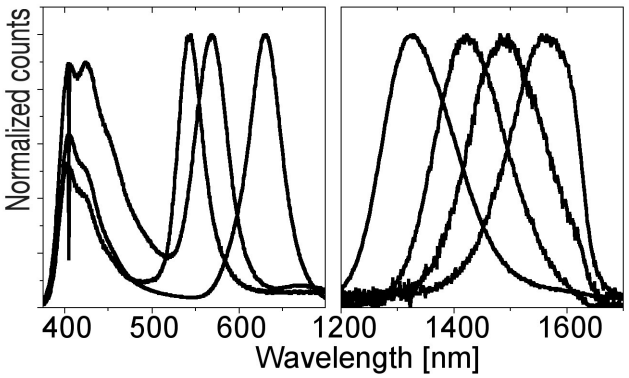

Fig. 23: (a) Typical absorption (peak at 1.456 μm), photoluminescence (peak at 1.500 μm), and electroluminescence spectra (peak at 1.495 μm) of 5.0±0.5 nm diameter PbSe particles; (b) HRTEM Image of 4.0±0.5 nm diameter PbSe particles with two enlarged images (inset).

Fast On-Chip Control Circuitry

Personnel

D. S. Crankshaw, J. Habif, and D. Nakada (T. P. Orlando, M. Feldman, M. Bocko, K. Berggren, and W. Oliver)

Sponsorship

ARO and Department of Defense University Research Initiative on Nanotechnology

RSFQ (Rapid Single Flux Quantum) electronics can provide digital circuitry which operates at speeds ranging from 1 - 100 GHz. It uses a voltage pulse to indicate a 1, and the lack of a voltage pulse within a clock cycle indicates a 0. If these electronics can be integrated onto the same chip as the qubit, complicated control with precise timing can be applied to the qubit by on-chip elements. The following design is currently in fabrication.

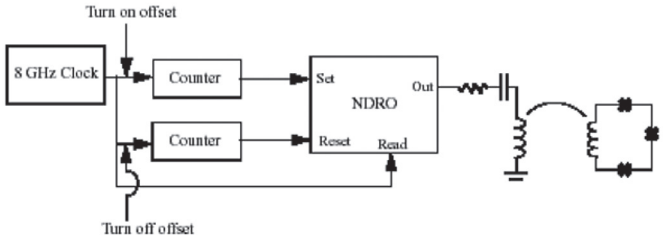

Fig. 24: An RSFQ Variable Duty Cycle Oscillator.

An RSFQ clock can be used as the oscillator to rotate the PC qubit. This oscillator has more frequency components and less tunability than a dc SQUID, but it is easier to use in conjunction with other RSFQ components. In the following design, these components can deliver a variable frequency signal (See Figure 24). An RSFQ clock is simply a Josephson Transmission Line ring. The transmission line propagates a pulse in its loop, which can be tapped off and used as a clock signal. Two counters and a Non-Destructive Read Out (NDRO) memory cell make up the digital pulse width modulator. The signal from the clock goes to both counters and to the Read input of the NDRO. The NDRO outputs a 1 for each clock input if a 1 is stored in it, but no output for each pulse if a 0 is stored in it. The output of the counters go to the Set (which sets the NDRO to 1) and the Reset (which resets the NDRO to 0) inputs of the NDRO. The counters are equal in length (13 bits), so that after 213 pulses, each one sends its output to the NDRO. By initially offsetting the counters by preloading them with the Offset inputs, one can set them out-of-phase with one another, thus controlling the duty cycle of the NDRO output. Since the NDRO signal has lots of harmonics, an RLC resonance filters the signal before delivering it to the qubit. The resonance filter converts the highly non-linear clock signal to a nearly sinusoidal signal.

The design has been fabricated, although testing is not yet complete. The most likely difficulty is easily identified given the results presented in Sections 2 and 3. Both the RSFQ circuit and the qubit have been fabricated at a current density of 500 A/cm2, where the qubit does not display the desired quantum properties. A new design is needed for 100 A/ cm2, which is where the qubit parameters are more ameliatory. This is shown in Figure 5. This design is simpler, since 100 A/cm2 requires larger junction and inductor sizes, which lessens circuit density and it operates more slowly. In this case, the timing is done off-chip, which is beneficial for synchronizing the measurement with the driving. The oscillator is once again a Josephson transmission line ring, this time operating at 3 GHz, and a signal is tapped off to drive the qubit.

This time there is no intervening circuitry, so the qubit sees an oscillating signal as long as the clock is on. The clock is interrupted by a NOT gate. Every time the clock ring sends its signal to the NOT gate, it will send a signal back into the ring unless it has received an external signal, in which case it will not output a pulse, and the clock will turn off. The signal which stops the clock comes from off the chip, using a single T-flip-flop as a divider. The first signal which comes from off-chip will be sent by the T-flip-flop to start the clock, while the second signal will be sent to stop it.

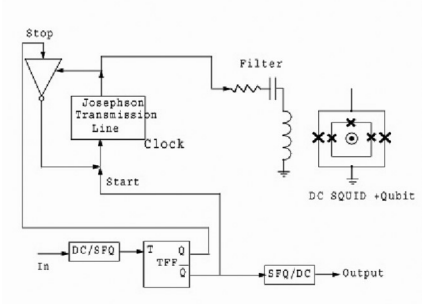

Fig. 25: An RSFQ oscillator which may be turned on and off by an external signal.

Exciton Physics in Organic Optoelectronics

Personnel
C. Madigan (V. Bulovic)

Sponsorship
National Science Foundation CAREER Award, National Defense Science and Engineering Graduate Fellowship (DOD)

Over the last decade, enormous strides have been made in the field of organic optoelectronic devices. A first generation of visible organic light emitting devices has been commercialized. Optically pumped lasers have been demonstrated at UV, visible, and IR wavelengths. Groups have fabricated photodetectors with collection efficiencies as high as 75%, and solar cells with power conversion efficiencies as high as 3% have been reported.

As a whole, these results represent an extraordinary technological achievement, but often lost in this torrential development of new devices has been a complete physical understanding of their operation. Specifically, the factors determining the properties and behavior of molecular excitons, the fundamental excitation operating in all organic optoelectronic devices, are only imprecisely understood. In this project, we study the influence of disorder in amorphous molecular organic materials on the excitonic energy structure of constituent molecules. We highlight two excitonic processes which are general to all amorphous organic thin film structures and which strongly determine organic device operation.

(a) Solid State Solvation

Emission and absorption spectra of many organic dyes in *liquid solutions* depend on the local electric fields generated by the surrounding polar solvent molecules and the response of the electronic charge on the solvent molecules to the excitation dynamics of the solute. This "solvation effect" is a result of intermolecular solute-solvent interaction forces (such as dipole-dipole or dipole-induced dipole) that tend to stretch molecular bonds and shift charge distribution on molecules, altering the energy difference between the ground and excited states of the solute. Our earlier experiments [Bulović, *et al.*, Chem. Phys. Lett. 287 (1998) 455; 308 (1999) 317] suggested that the solvation effect is also present in *molecular solids* where closely packed polar molecules can generate large local electric fields. In these first studies, we examined the Solid State Solvation (SSS) induced luminescence red shifts of amorphous organic thin films doped with the red laser dye [2-methyl-6-[2-~(2,3,6,7-tetrahydro-1H, 5H-benzo [i,j] quinolizin-9-yl)-ethenyl]-4H-pyran-4-ylidene] propane-dinitrile (DCM2). By changing the concentration of DCM2 present in a film of N,N'-diphenyl-N,N'-bis(3-methylphenyl)-[1,1'-biphenyl]-4,4'-diamine (TPD) from 0.9% to 11%, the peak electroluminescence emission wavelength shifted from λ=570 nm to λ=645 nm (see Figure 26). (In these measurements, the DCM2:TPD film comprised the active layer of an OLED.) Because DCM2 is a highly polar molecule (with μ~11 D in ground state), and TPD is nearly nonpolar (with μ~1 D in ground state), increasing the DCM2 concentration was thought to increase the strength of the local electric fields present in the film, and that this increase in the local fields was the cause of the spectral shift. The authors viewed the mechanism as a solid state realization of solvation, and so termed it "Solid State Solvation." Similar results were also observed for DCM2 in aluminum tris-(8-hydroxyquinoline) (Alq_3) and Alq_3 in TPD (see Figure 26). Further quantification of this mechanism, however, was complicated by a subsequent report which argued that as the DCM2 doping increased in these systems, the DCM2 quantum efficiency dropped, which is generally considered an indicator of dopant aggregation [Baldo *et al.*, Chem. Phys. Lett. 347 (2001) 297]. Such aggregation, by implying substantial local inhomogeneity in doping, would make it difficult to specify the environment surrounding each molecule. We, therefore, developed an alternative system in which to study the SSS phenomenon.

We prepared spun-cast films consisting of polystyrene (PS), a small concentration of the laser dye DCM2 (< 0.005% by mass), and a range of concentrations of the polar small molecule material camphoric anhydride

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(CA). This material system was chosen so that the DCM2 concentration could be kept constant (and very low), thereby fixing (and limiting) DCM2 aggregation effects, while still allowing for the modification of the strength of the local fields in the film. We modified these fields by changing the concentration of CA, which has a large dipole moment (μ~6D in ground state) relative to its molecular weight and is optically inactive over the range of wavelengths relevant for studying the properties of DCM2. The polymer host material polystyrene was selected because it provides a transparent, non-polar background for the system.

For a fixed DCM2 concentration of 0.005%, we found that the DCM2 emission spectrum shifts continuously from 2.20 eV (563 nm) to 2.05 eV (605 nm) for CA concentrations ranging from 0% to 25% (See Figure 27). We also performed the same measurements on films with DCM2 concentrations up to 0.05%, and observed no change in the results, demonstrating that aggregation does not play a role. Measurement of the electronic susceptibility of the films (See Figure 27) shows a marked increase with CA concentration, following a linear relationship given by A=2.44+0.13 (CA%).

Our results show that the DCM2 emission red shifts as the concentration of dipoles (i.e. CA molecules) increases in the film, and that this phenomenon is not related to DCM2 aggregation, but is consistent with the SSS mechanism sketched in Figure 28. By employing a system free of aggregation and then measuring the electronic susceptibility, however, we can take the model a step further and apply the theory of liquid solvation quantitatively to our films.

Using the Ooshika-Lippert-Matanga (OLM) approach [Ooshika, *J. Phys. Soc. Japan*, 9 (1954), 594; Lippert, *Z. Naturforsch.*, 10a (1955), 541; Mataga *et al.*, *Bull. Chem. Soc. Japan*, 29 (1956), 465.], we may write for the relaxation energy under the influence of solvation from a dielectric medium as,

$$E^{\downarrow} = C - A\ddot{E} \qquad (1)$$

where

$$\ddot{E} \equiv \frac{2(\breve{a}-1)}{2\breve{a}+1} \qquad (2)$$

and A and C are constants. In Figure 29, we plot three different fits to the spectral data, indicating the sensitivity of the fit to the choice of A. We find that the trend in the spectral shift is in excellent agreement with the solvation theory, with the optimal fit obtained for A = 0.57 eV.

It is difficult to determine how plausible this value is based on the definition for A because of inherent arbitrariness in the specification of the OLM parameters. However, we *can* look at solvation in solutions where the solvation mechanism is known to operate. A plot of the peak emission energy for DCM2 in different solvents is shown in Figure 29 against each solvent's value for ε. We find that the OLM theory again works quite well and obtain an optimal fit for A = 0.55 eV.

The SSS mechanism can, therefore, comprehensively describe the observed spectral shifts, and the model parameter is consistent with known values for DCM2 in solution. A priori, this result is not surprising as one could argue that dielectric relaxation in amorphous organic solids should be similar to that of liquids. Indeed, the SSS process can strongly determine the dispersion and position of molecular energy levels in organic solids. Additionally, SSS could be used as a new method for the engineering of energy structures, both for excitonic levels (as studied in this work) and for conduction levels (which are also subject to solvation).

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(b) Exciton Diffusion

The second process we have studied is Exciton Diffusion which refers to the migration of excitons between molecules. Though the presence of exciton diffusion is well-known, the details of the phenomenon have not been studied in a disordered solid. Specifically, the impact on this process of dispersion in molecular energy levels has been previously ignored, but we find plays a controlling role.

Time resolved photoluminescence measurements of disordered molecular organic thin films of Alq_3 doped with DCM2 show an emission spectrum that significantly red shifts as a function of time following excitation by a 100 fs laser pulse (See Figure 30). (The spectral measurements were performed using a Hamamatsu streak camera.) Spectral shifts of ~ 0.10 eV over a time window of ~ 10 ns are observed for doping levels ranging between 0.5% and 5% in addition to significant spectral narrowing over that same period. We show that this previously unreported phenomenon can be attributed to the diffusion of excitons through the film by means of Forster energy transfer between DCM2 molecules.

This site-to-site transfer rate is governed by the emission and absorption spectra of the exciton donating and the exciton accepting molecule. From Förster's original formulation, the rate of exciton transfer, $\tilde{A}_F$, is given as

$$\tilde{A}_F = \frac{1}{\hat{o}_{rad}} \left(\frac{R_F}{R} \right)^6 \qquad (3)$$

where R is the distance separating the donor and acceptor, $\hat{o}_{rad}$ is the intrinsic radiative lifetime of the donor, and R_F is the Förster radius, given by,

$$R_F = \frac{3\, c^4}{4\delta\, n^4}\, \acute{e}^2 \int \qquad (4)$$

where $\acute{I}^2$ reflects the relative orientation of the donor and acceptor, n is the index of refraction of the medium, S_p is the normalized donor fluorescence spectrum, and $\acute{U}_A$ is the acceptor molar absorption cross section (in units of cm^2).

As indicated by the rate expression, the Förster energy transfer occurs more readily when the acceptor molecule has lower energy spectra than the donor. In other words, the Förster mechanism preferentially transfers excitons towards lower energy sites. If we combine this observation with an assumption that the excitonic density of states, $g_{ex}(E)$, has a non-zero width (i.e. that there exists some dispersion in exciton energies in our film), we obtain a straightforward explanation of the observed time-resolved spectral shifts: diffusion by Förster energy transfer progressively drives the excitons in the film towards the lowest energy sites.

We developed a Monte Carlo simulation of this diffusion process. The simulation tracks the emission and Förster energy transfer of excitons in a large lattice of molecular sites, with each site characterized by its position and peak emission energy. The lattice spacing corresponds to the mean molecular inter-site spacing. The histogram of all the site energies reproduces the shape of the $g_{ex}(E)$ distribution. We have assumed that $g_{ex}(E)$ has a Gaussian form, with a full-width-half-max (FWHM) of w_{DOS}. Once the system of sites has been created, each site is populated with an exciton, yielding an exciton population, $n_{ex}(E,t)$, such that,

$$n_{ex}(E,t=0) \propto g_{ex}(E) \qquad (5)$$

where t=0 refers to the time immediately following the arrival of the PL excitation pulse. Then for each time step of length U_{step} each exciton has the opportunity to Förster transfer to another site or to emit.
The simulation yields results consistent with the experimentally observed shifts (See fits in Figure

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30), and through fitting of the available parameters, provides a probe of w_{DOS} and R_F. The values for w_{DOS} decrease from ~0.260 eV for 0.5% DCM2 doping to ~0.205 eV for 5% doping. In addition we find that R_F falls with increasing doping, from 38 Å for 0.5% to 20 Å for 5%. We can not turn to any published results for a direct comparison of these fitted values. However, there do exist calculations of w_{DOS} for polaron levels in amorphous organic materials, where the polaron $w_{DOS} \sim 0.1eV$. Though it is not necessary that polaron levels and excitonic levels should experience identical energy dispersion, it is reasonable to expect that they are comparably dispersed, which is what we observe.

We know of no other method for measuring the energy dispersion in exiton energies in the literature. For this reason, this technique potentially represents a major breakthrough in the analysis of energy structure in amorphous organic solids. We have also demonstrated this modeling method with neat films; we studied time-dependance of PL in films of Alq_3 and $Ir(ppy)_3$. The evolution of the peak PL for these two films is shown in Figure 31, along with fits from our simulation. Note that spectral shifts just like those observed in the DCM2:Alq_3 system are observed. In both cases, we obtain R_F ~ 12 Å and w_{DOS} ~ 0.075 eV, which, as per the arguments made above, have reasonable magnitudes. The similarity between the two systems should not be surprising as they have similar molecular ground state dipole moments and bulk spectral overlaps.

By extension, this technique should apply to any pure organic thin film material in which Förster energy transfer occurs. Experimentally, all that is required is a film with thickness of at least 20 nm and an ultrafast source operating at a wavelength for which the film is absorptive. Thus we find that this technique is not only of great value in analyzing excitonic properties in organic thin films, but its application is also straightforward and general.

(c) Conclusions

In inorganic, crystalline semiconductors, accurate physical models have been invaluable in assisting technological improvement. Currently, however, very few physical models describe electronic and excitonic behavior in organic optoelectronic devices. The larger aim of this work is the development of a practically useful model of electronic and optoelectronic processes in amorphous organic solids, which might then be used to predict the behavior of new organic device structures. The quantification of SSS helps us towards this goal in identifying one of the primary mechanisms by which solid state energy levels are altered from their gas phase values. In addition, it identifies an additional lever with which one can modify energy levels through the modification of bulk property (i.e. electronic susceptibility). The development of a more comprehensive theory of exciton diffusion aids us by providing a building block for a total model of electronic and optoelectronic processes in organic thin films. Combined with a carrier transport model and a microcavity model, one can already imagine constructing a simulation of a working OLED. And as indicated above, applying the exciton diffusion model to dynamic spectral shifts allows us to obtain previously inaccessible information about the excitonic energy level dispersion. While much work remains in developing physical models of processes in organic optoelectronic devices, these results already represent a significant step forward (See Figure 32).

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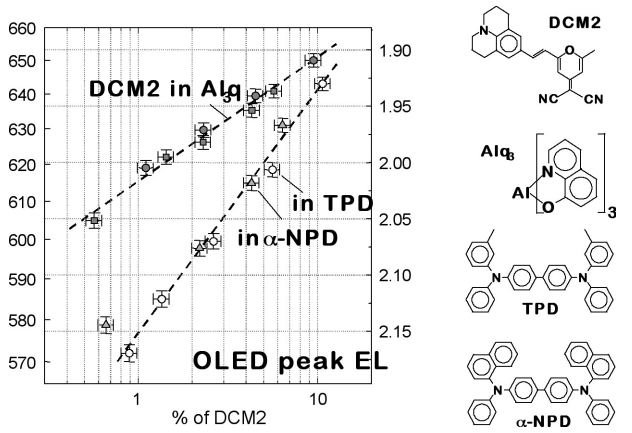

Fig. 26: (a) Evolution of peak PL spectra of DCM2 in films of Alq_3, TPD and α-NPD.; (b) chemical structures of molecules used in this work.".

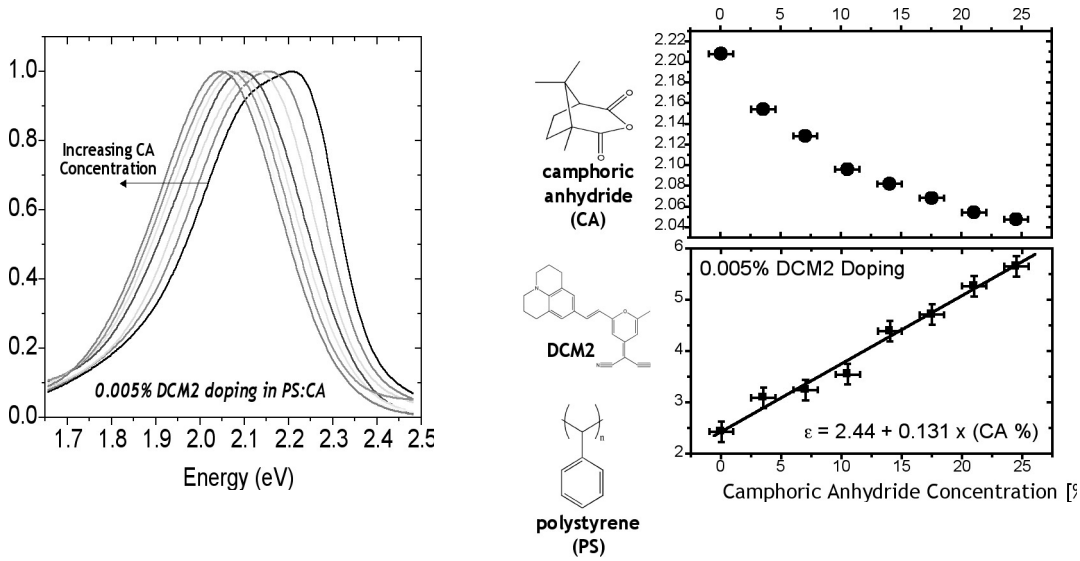

Fig. 27: (left) PL spectra of 0.005% DCM2 in PS:CA films. The spectrum red-shifts as the CA concentration is changed from 0 to 25%. (middle) Chemical structures of CA, DCM2, and PS. (right) Change of the peak luminescence energy and the dielectric constant as a function of CA doping.

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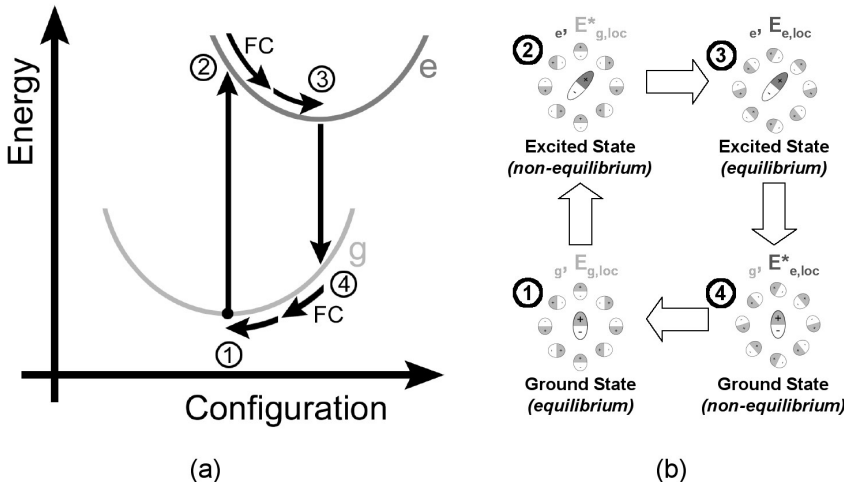

Fig. 28: Equilibrium and non-equilibrium states of the solvation process.

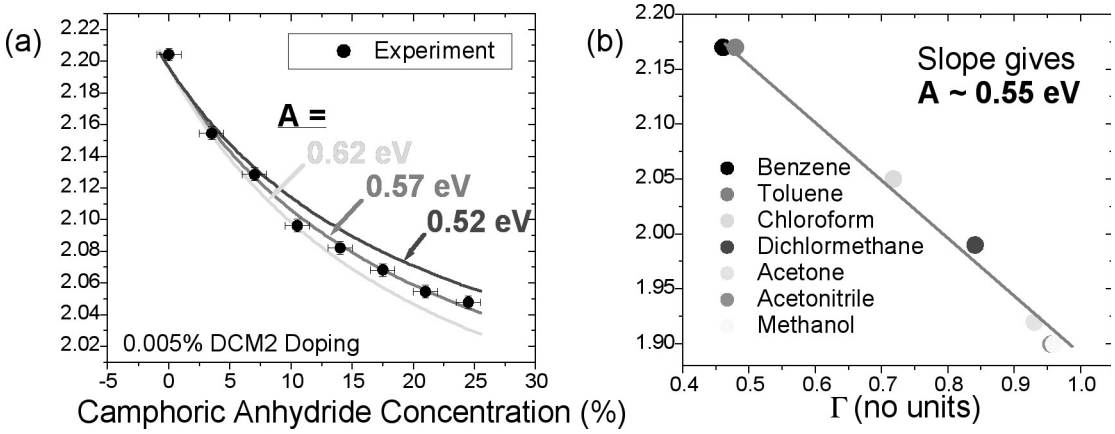

Fig. 29: (a) Fits of OLM theory to observed evolution of DCM2 peak PL energy; (b) OLM fit to DCM2 PL data in solution.

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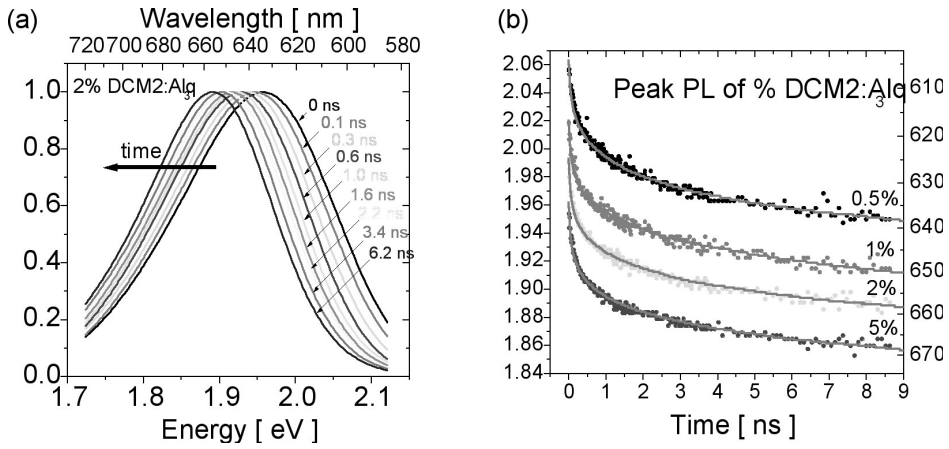

Fig. 30: (a) Normalized DCM2 PL spectra, following ultrafast excitation; (b) Evolution of peak PL of DCM2 doped in films of Alq_3. Grey lines denote simulation results optimized for each data set.

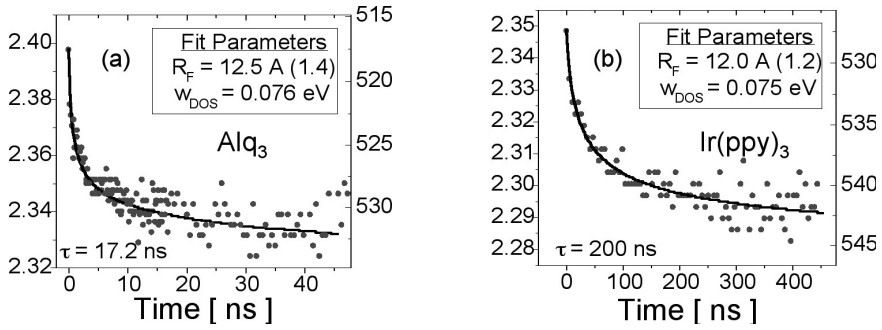

Fig. 31: (a) Evolution peak PL of Alq_3 with simulation fit; (b) evolution of peak PL of $Ir(ppy)_3$ with simulation fit.

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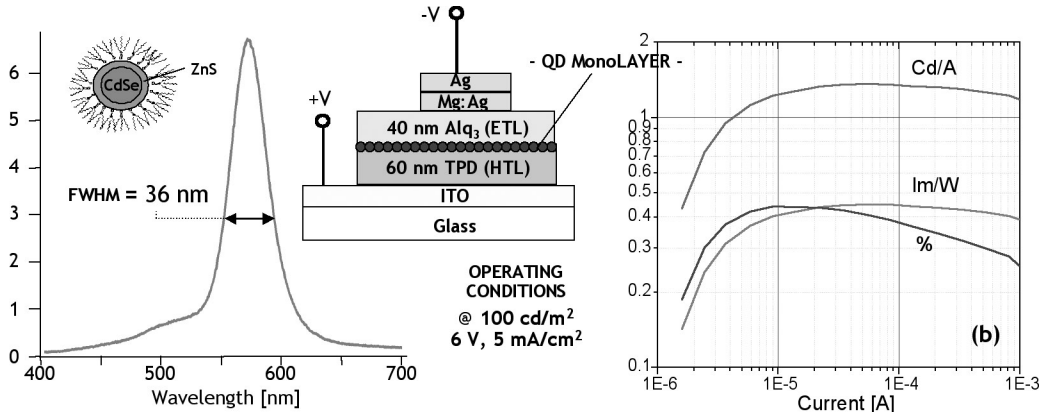

Fig. 32: Hybrid organic/inorganic light emitting device contain inorganic QDs. (Inset) QD-LED cross section. (left) Electro-luminescence spectrum at ~100 cd/m^2, with inset device cross section. (right) QD-LED quantum efficiency in percent units, and luminescence efficiency in units of Cd/A and lm/W.

Efficient Electrically Pumped Polariton Emission in a J-Aggregate OLED at Room Temperature

Personnel
J. Tischler (V. Bulovic)

Sponsorship
DARPA Optoelectronic Center for Innovative Photonic Chipscale Technologies

The goal of this project is to develop ultrafast active optoelectronic devices based on the unique physical properties of J-aggregates and their interaction with light. The essential physics of J-aggregates underpinning this project is that the excited state of a J-aggregate is a delocalized Frenkel exciton of high oscillator strength, which enables it to couple strongly to the optical field inside a resonant cavity according to the principles of semiconductor cavity QED. We are using J-aggregates because J-aggregates exhibit the strong coupling regime of Cavity QED, even at room temperature, even in an all-metal cavity, and because their lifetime is extremely short. The ultimate goal is to realize the vision of the electrically pumped polariton laser and polariton optical switches at room temperature, using J-aggregates as our material platform. The first milestone is to develop a room temperature polariton LED.

J-aggregates are ordered arrangements of highly polar cyanine dye molecules (See Figure 33) in which the transition dipole moments of the individual molecules add to form a giant dipole oscillator. When dye molecules form a J-aggregate, a new optical transition develops called a J-band. Relative to the monomer, this optical transition of the J-aggregate is red-shifted, minimally stokes shifted, and considerably narrower in energy, and the lifetime of this transition is also much faster. J-aggregates are therefore described anatomically and functionally. Anatomically, they are crystalline phase of the dye monomers, although not necessarily the lowest energy crystalline form, and functionally, they are quantum systems in which the excitons delocalize over several molecular sub-units of the aggregate, which gives rise to narrow absorption and emission spectra.

J-aggregates received their moniker in recognition of Edwin Jelly, who, while working for Kodak in the 1930's, discovered that the cyanine dye, PseudoIsoCyanine (PIC), at high concentrations became resonantly fluorescent [E. E. Jelly, Nature 138, 1009 (1936)]. This was surprising at the time because PIC at lower concentrations is not fluorescent. It is also contrary to the generally accepted rule of concentration quenching which states that the higher the concentration is, the lower the quantum yield of fluorescence. From that point forward, J-Aggregates have been studied to understand the physics of excitons, their optical properties, and their crystallographic properties; and this understanding has been fruitfully applied to the science of sensitizing photographic active silver halide crystals to narrow bands of light in regions of the visible spectrum that the silver halides would otherwise not absorb.

The genesis for our research effort has come from the recent demonstration of room temperature polariton photoluminescence from J-aggregate Frenkel excitons coupled to the cavity photon mode [Lidzey et al., Nature 395, 53 (1999)]. Because of the high oscillator strength of the Frenkel exciton, Rabi Splitting exceeding 100meV was realized, an order of magnitude larger than the splitting achieved in inorganics even at ultralow temperature. This work laid the foundation for us to start imagining how we could access the strong coupling regime using J-aggregates in active optoelectronic devices.

To make these devices, J-aggregates must be formed in a thin film process. J-aggregates can be formed in solution and in solid state. In solution, particularly in water, the dye molecules form aggregates at high concentration and in an alkaline environment; while in solid state, J-aggregates form more readily when in contact with a polymer template. In our present studies, we use PolyVinyl Alcohol (PVA) polymer layer. We have chosen JC-1 as the J-aggregate molecule (See Figure 34). JC-1 readily forms J-aggregates even at ultra low concentrations (10^{-5} M) and has been well studied

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in the photographic industry, as a membrane potential sensitive dye, and for its rich exciton dynamics. To investigate it's applicability for strong coupling devices, we sought to demonstrate Rabi Splitting and measure the polariton dispersion curve for JC-1. We prepared a series of samples, consisting of silver mirror layer (1200Å), J-Aggregate/PVA matrix and a thin silver film on top (300Å) (See Figure 35). The thickness of the J-Aggregate layer was varied so as to tune the bare cavity mode through the J-Aggregate exciton resonance. From reflectivity measurements taken from 7° - 70°, we conclude that JC-1 does in fact exhibit a strong coupling to the photon mode as illustrated by the anti-crossing in the dispersion curves. From this data and other dispersion curves we calculate a Rabi Splitting of >95 meV.

Our current objective is to develop an efficient J-Aggregate OLED that we can then fabricate within an optical cavity to demonstrate electrically pumped polarition emission. Presently, we have successfully demonstrated EL from JC-1 in an exploratory structure consisting of a mixed film of PVA doped with JC-1 (See Figure 36).

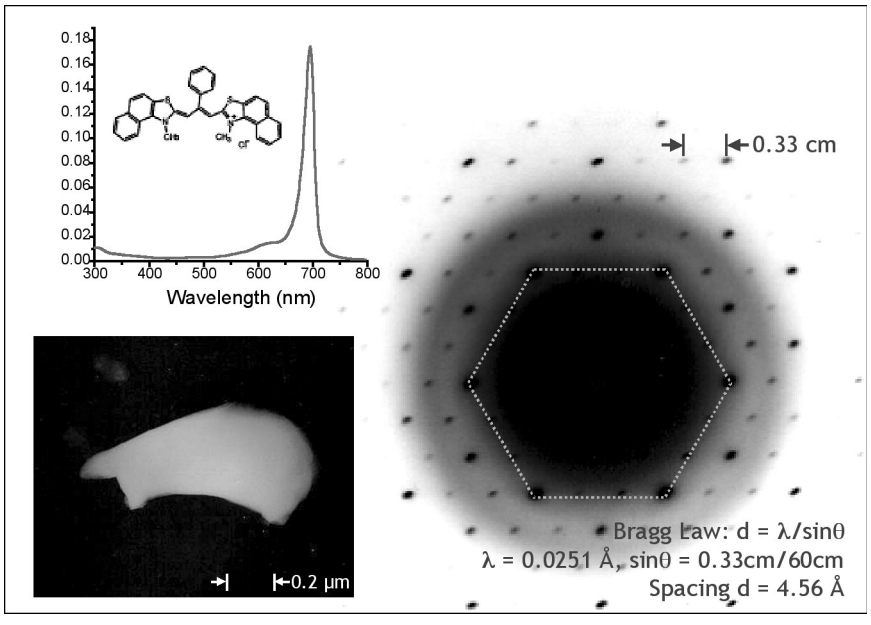

Fig. 33: Absorption spectrum, TEM Micrograph, and electron diffraction pattern of a J-aggregate dispersed in polyvinyl alcohol.

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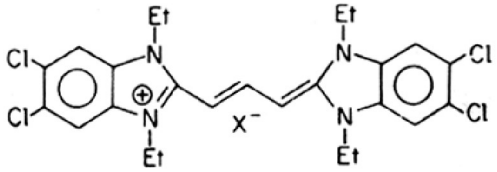

Fig. 34: JC-1, a cyanine dye that readily forms J-aggregates in solution and solid state.

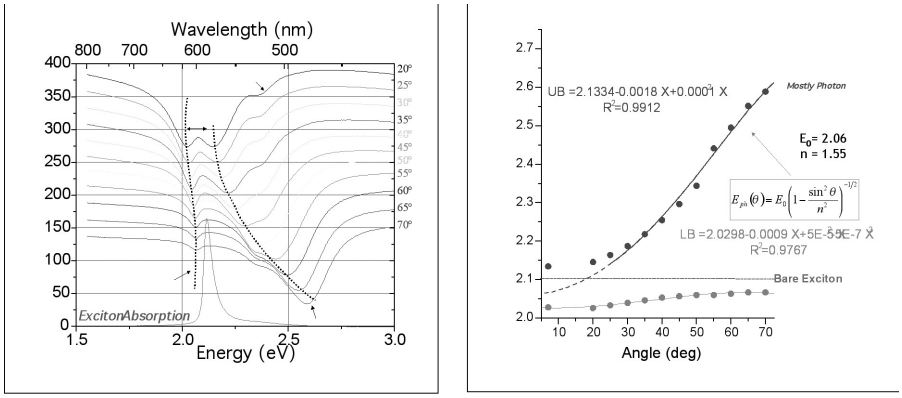

Fig. 35: Angle dependent reflectivity and dispersion curve of a silver mirror metal microcavity containing J-aggregates of JC-1 in polyvinyl alcohol.

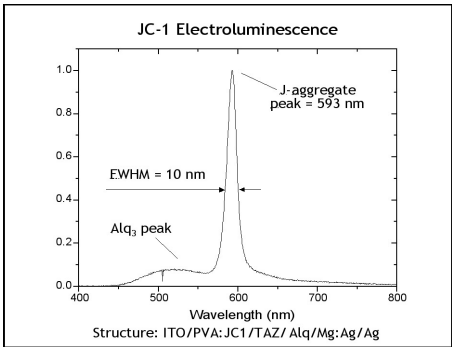

Fig. 36: Electroluminescence spectrum of a JC-1 OLED.

An On-Chip Frequency-Domain Submillimeter-Wave Spectrometer

Personnel
J. Montoya (Q. Hu)

Sponsorship
Rosenblith Fellowship

Because of the frequency limitation of semiconductor electronic devices, measurement instruments such as network analyzers can operate only below approximately 100 GHz. Thus, even if ultrahigh-frequency HBTs can be developed, they can only be directly measured up to 100 GHz, with higher-frequency performance extrapolated according to certain frequency roll-off models. Clearly, such an extrapolated measurement will not be applicable to measuring high-frequency resonance such as that shown in Figure 37. It will be very useful to develop on-chip systems that can characterize device performance up to THz frequencies. A promising component for such systems is ultrafast photoconductive switches made of Low-Temperature-Grown (LTG) GaAs materials. When pumped with two coherent laser beams, such switches can generate and detect photocurrent with a modulation frequency beyond one THz.

Furthermore, photoconductive emitters and receivers are attractive as components of sub-millimeter-wave spectroscopy systems because of their tunability, compactness, and ability to be monolithically integrated with antennas, transmission lines, and microelectronic devices. Such systems can be classified either as time-domain or frequency-domain systems. Time-domain systems, which contain a photoconductive pulse emitter and sampler excited by a mode-locked laser, are the most investigated. They have been used for free-space characterization of semiconductor materials, and on-chip characterization of ultrafast devices and circuits with 2.7 ps time resolution. The frequency resolution is the inverse of the time span over which the propagating pulse is sampled. This span is determined by the length of an optical delay line, which usually results in a frequency resolution broader than 1 GHz.

The emitter and receiver of a frequency-domain spectrometer will be pumped by two coherent cw laser beams with frequencies ω_1 and ω_2, instead of short laser pulses. If the response time is sufficiently fast, the emitter switch will generate an ac photocurrent with a frequency $|\omega_2-\omega_1|$ which can easily exceed 1 THz. Illuminated by the same two laser beams with a controlled delay, the receiver switch can be used to perform a homodyne detection of the ac photocurrent generated from the emitter. In combination with high-frequency transmission lines, they can form on-chip spectrometers with THz bandwidths. Figure 37 illustrates a schematic of such a spectrometer that can be used to characterize common-emitter performance of high-frequency HBTs.

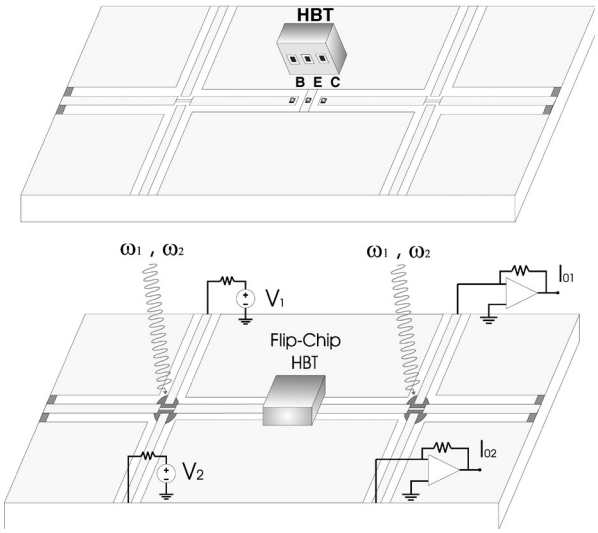

Fig. 37: Schematic of a on-chip spectrometer that uses ultrafast photoconductive switches to generate and detect ultrahigh-frequency signals.

Because of the broad bandwidth (>1 THz) and a high frequency resolution (better than 1 MHz), such a spectrometer is also adequate for molecular line spectroscopy. In combination with microchambers, the spectrometer can be part of a microfluidic, "lab on a chip"-type circuit which can be used as on-chip sensors for chemical and biological agents. As the first step

continued

in the development of an on-chip frequency-domain spectrometer, we have investigated the performance of an on-chip transceiver containing only uninterrupted CoPlanar Waveguides (CPWs).

In order to improve the coupling efficiency of the photoconductive switches and to reduce their RC time constants, we used interdigited finger electrodes fabricated using e-beam lithography. A SEM picture of such a photoconductive switch is shown in Figure 38.

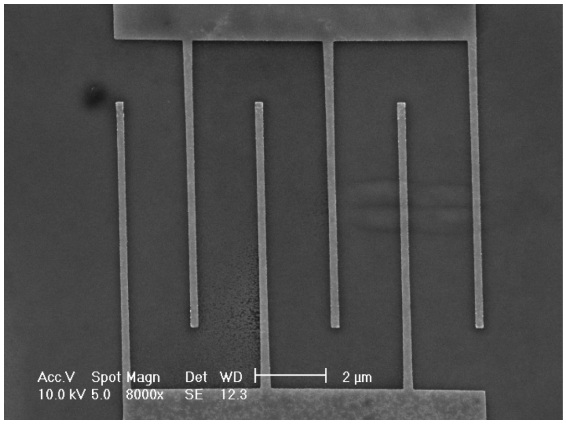

Fig. 38: SEM picture of a photoconductive switch with interdigited finger geometry and fabricated using e-beam lithography.

Previously, we have shown that LTG-GaAs photoconductive switches embedded in a transmission line can function as an intensity-intensity autocorrelator, based on the nonlinearity of a voltage divider including the photoconductive switch and the characteristic impedance of the transmission line. The time resolution of this autocorrelator, however, is limited by the response time of the LTG-GaAs photoconductive switch, which is on the order of 1 ps. In order to improve the time resolution of the autocorrelator to the degree that it can resolve the time span of femtosecond laser pulses, a more intrinsic nonlinear process must be used than the voltage divider scheme. In a recent experiment, we have developed a much faster autocorrelator by using two-photon absorption process in the photoconductive switch. The almost instantaneous nature of this nonlinear process greatly improves the time resolution of the autocorrelators. Figure 39 shows the measured time profile of fs laser pulses from a mode-locked Ti:sapphire at 900-nm wavelength. At this long wavelength, the photon energy is smaller than the energy gap of LTG-GaAs; thus, single photon absorption is suppressed. As can be seen from Figure 39, the pulse shape measured using this novel autocorrelator is in good agreement with that measured using a conventional autocorrelator with SHG crystals. This development could lead to compact, alignment free autocorrelators with femtosecond time resolutions. Furthermore, the gap energy of LTG-GaAs will make it a natural candidate for the two photon absorption measurements at ~1500-nm wavelength, which is important for fiber telecommunications.

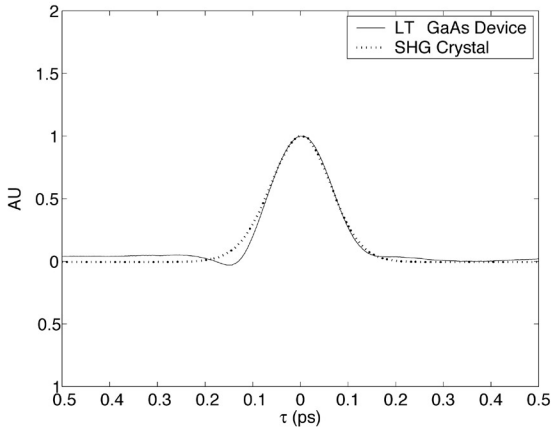

Fig. 39: Two photon absorption autocorrelation at 900-nm wavelength with an average laser power of 170 mW.

Measurement of Qubit States with SQUID Inductance

Personnel
J. C. Lee (T. P. Orlando and W. Oliver)

Sponsorship
AFOSR/DURINT, ARDA, and NSF

For the persistent current qubits, the two logical states correspond to currents circulating in opposite directions. The circulating current generates a magnetic flux that can be sensed by a SQUID magnetometer inductively coupled to the qubit. Depending on the state of the qubit which determines the direction of the persistent current, this additional flux either adds to or subtract from the background magnetic flux. Therefore, during the readout process, the two qubit states can be distinguished by a difference in magnetic flux signal, typically on the order of a thousandth of a flux quantum.

It is of great consequence that the measurement setup has minimum back-actions on the qubit. The present measurement scheme is the so-called switching current method and has some major drawbacks. It uses the property that the critical current of a SQUID is a function of the magnetic flux that it senses, and hence, will be different depending on what state the qubit is in. During the measurement, the value of the critical current is obtained directly by ramping a DC current through the SQUID and determining the point at which it switches from the superconducting state to the finite voltage state. This method requires a high current bias and introduces severe back-actions on the qubit.

The SQUID inductance measurement scheme was proposed to be an improvement over the switching current method. With this method, the current through the SQUID can now be biased significantly below the critical current level, and hence, reduces the back-actions on the qubit. The idea is to use the SQUID as a flux-sensitive inductor. Basically, the Josephson inductance across the junctions of the SQUID is also a function of the magnetic flux. To measure the inductance effectively, the SQUID is inserted in a high Q resonant circuit (See Figure 40). Note that the circuit is fed by a DC current bias as well as an AC source of a single frequency ω_b.

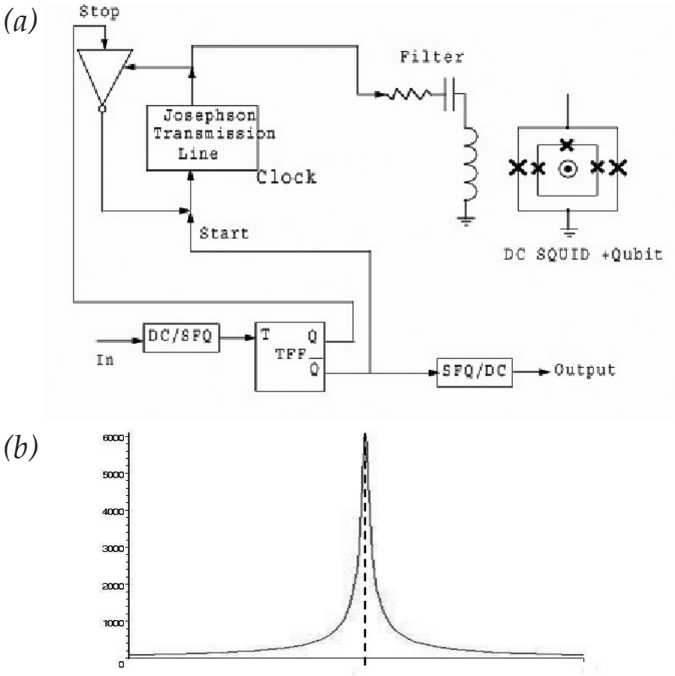

Fig. 40: (a) A resonant circuit used to measure the SQUID inductance. The 'x' represents a Josephson junction. This circuit is simplified from the actual design for illustrative purpose. (b) The corresponding plot of the magnitude of the impedance vs. frequency. The resonant frequency is denoted as ω_o.

Upon a change in the qubit state, the corresponding change in the SQUID inductance will shift the resonant frequency (See Figure 41). This is because the resonant frequency is given by $1/\sqrt{LC}$, where L is the inductance of the SQUID. If one keeps the AC current source at a bias frequency £sb, typically around 500MHz, one senses a change in the impedance ΔZ. This in turn results in a difference in the output voltage ΔV corresponding to $I_{AC} X \Delta Z$. This voltage difference will be measured to detect the state of the qubit.

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High Q resonant circuits were designed with impedance transformation and impedance matching techniques to optimize the measurement process. Detailed calculations were performed for the specific circuits currently being fabricated at the MIT Lincoln Laboratory, and the voltage corresponding to the qubit signal is expected to be about 10μV.

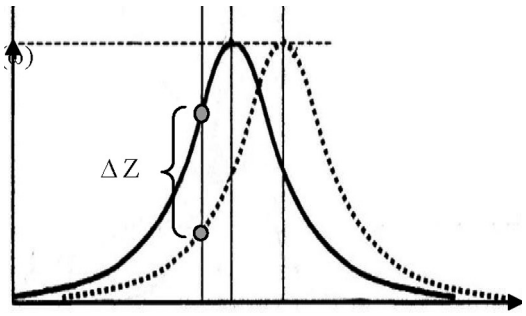


Fig. 41: Illustration of the shift in resonant frequency $\Delta\omega_0$ upon a change in the qubit state. During the measurement, one biases the operating frequency at £sb and senses a change in impedance ΔZ, which in turn can be retrieved as a voltage signal.

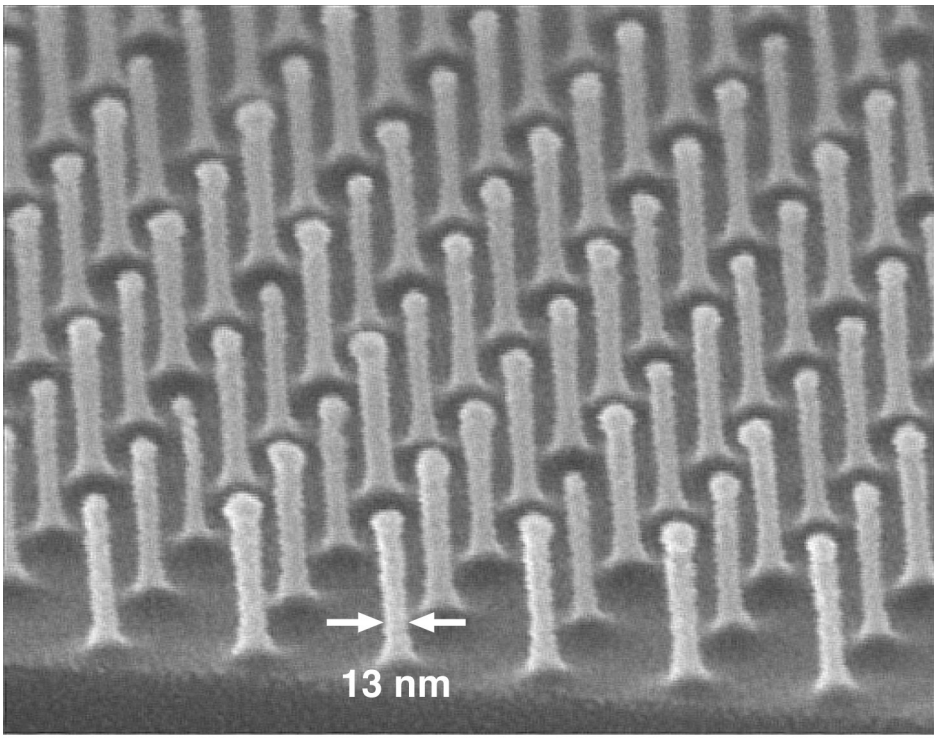
Opposite page:

Scanning electron micrograph of a 100 nm-period grid, exposed in PMMA on top of an antireflection coating, and transferred into Si by reactive ion etching.

Courtesy of J.M. Carter, R.C. Fleming, T.A. Savas, M.E. Walsh, and T.B. O'Reilly (M.L. Schattenburg and H.I. Smith)

Sponsor:
DARPA and U.S. Army Research Office

Submicron and Nanometer Structures



100nm-period posts in Si

Submicron and Nanometer Structures

- *Scanning-Electron-Beam Lithography*
- *Spatial-Phase-Locked Electron-Beam Lithograpy*
- *Zone-Plate-Array Lithography (ZPAL): The System*
- *Interference Lithography for Patterning Variable-Period Gratings*
- *Zone-Plate-Array Lithography (ZPAL): Lithographic Performance*
- *X-Ray Nanolithography*
- *Nanometer-level Feedback-Stabilized Interferometric Aligning and Gapping in an X-Ray Lithographic System*
- *Adaptive-Membrane-Mask Technology*
- *Interference Lithography*
- *The MIT Nanoruler: A Tool for Patterning Nano-Accurate Gratings*
- *Templated Self-Assembly*
- *Block Copolymer Lithography*
- *Precision Fabrication Techniques for Microphotonic Devices*
- *Nanopattern-Assisted Growth of Organic Materials for Device Applications*
- *Strain-Tunable Photonic Band Gap Microcavity Waveguides at 1.55 μm*
- *Nanopelleting of Carbon Nanotubes*
- *Nanofabricated Metal Transmission Gratings*
- *Nanofabricated Reflection Gratings*
- *Transmission Gratings for X-Ray and Atom-Beam Spectroscopy and Interferometry*
- *X-Ray Foil Optics Shaping Technology*
- *Nano-Accurate Assembly Technology for X-Ray Foil Optics*
- *Functional 3D Nanostructures Achieved via Folding of 2D Membranes*
- *Integration of Nanowires Embedded in Anodic Alumina Templates with a Large Silicon Substrate*

Scanning-Electron-Beam Lithography

Personnel

J.T. Hastings, M.K. Mondol, and F. Zhang (H.I. Smith)

Sponsorship

NSF, DARPA, and U.S. Army Research Office

Figure 1 is a photograph of the Scanning-Electron-Beam Lithography system (VS-26) located in the Scanning-Electron-Beam Lithography (SEBL) facility, Room 38-165. This instrument was put together at MIT from two systems (VS-2A and VS-6) obtained as gifts from IBM in the mid 1990's. It has a minimum beam diameter of about 12 nm and is capable of creating large-area patterns composed of multiple stitched fields. Conversion software has been developed which allows a CAD data file to be fractured and translated prior to exposure by the electron-beam tool. Substrates up to 20 cm diameter can be exposed at linewidths down to 30 nm. In order to write concentric circular patterns, such as Freznel zone plates, software was developed to generate arbitrary arcs of an annulus with user-specified start and finish radii and angles.

The SEBL facility also houses a Raith Turnkey 150 system as shown in Figure 2. Its electron-optical column is essentially identical to that of a Gemini SEM, and provides a beam diameter as fine as 5 nm. Linewidths of 17 nm have been written with the system, as illustrated in Figure 3.

The goals of the SEBL facility are to: (1) provide the MIT research community with an in-house SEBL capability for writing directly on experimental device substrates; (2) advance the state-of-the-art in SEBL, particularly with regards to pattern placement accuracy and long-range spatial-phase coherence; and (3) pattern photomasks and X-ray nanolithography masks for in-house use.

The VS-26 and Raith 150 are heavily used in a variety of projects, both mask making and direct write. These have included: 3-D, 2-D, and 1-D photonic bandgap structures; optical-communication filters; arrays of Fresnel zone plates; electrical contacts to bismuth nanowires; high-density magnetic nanodots and rings for information storage; distributed-feedback lasers; sub-100 nm electronic devices; double-gate sub-100nm MOSFETs; diffractive optical elements; and magnetic random access memory devices. Masks have been made for X-ray nanolithography and conformable-contact photolithography.

The Raith 150 is used in a program to develop spatial-phase-locked e-beam lithography. The objectives of this program are (1) to achieve sub-1 nm pattern-placement accuracy, and (2) to reduce the cost and complexity of SEBL. In a conventional SEBL system costing several million dollars, pattern placement accuracy is typically much worse than 10 nm.

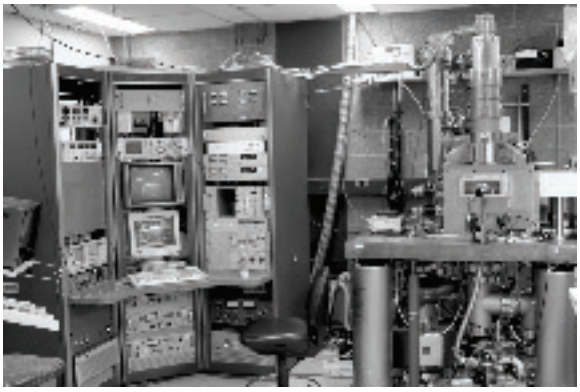


Fig. 1: Photograph of the VS-26 scanning-electron-beam lithography system.

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Fig. 2: The Raith-150 electron-beam lithography system. This tool provides sub-20-nm patterning resolution, and pattern-placement accuracy ~ 1nm via spatial phase locking. The operator is graduate student J. Todd Hastings.

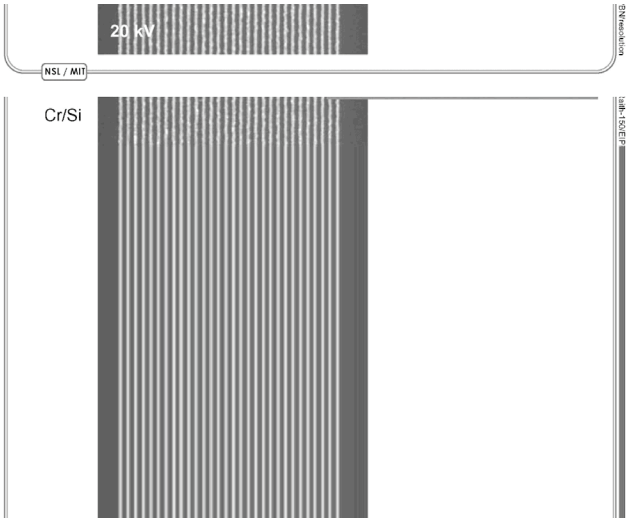

Fig. 3: Scanning electron micrograph illustrating the resolution of the Raith 150 SEBL system.

Spatial-Phase-Locked Electron-Beam Lithography

Personnel

C. Caramana, Dr. J. Goodberlet, J.T. Hastings, M.K. Mondol, and F. Zhang (H. I. Smith)

Sponsorship

DARPA and U.S. Army Research Office

Our research in Spatial-Phase-Locked Electron-Beam Lithography (SPLEBL) is aimed at reducing pattern-placement errors in electron-beam-lithography systems to the nanometer level. Such high precision is essential for a variety of future lithographic applications. SPLEBL is currently the only approach capable of achieving such accuracy. As shown in Figure 4, SPLEBL uses a periodic signal, derived from the interaction of the scanning e-beam with a fiducial grid on the substrate, to continuously track the position of the beam while patterns are being written. Any deviation of the beam from its intended location on the substrate is sensed, and corrections are fed back to the beam-control electronics to cancel errors in the beam's position. In this manner, the locations of patterns are directly registered to the fiducial grid on the substrate.

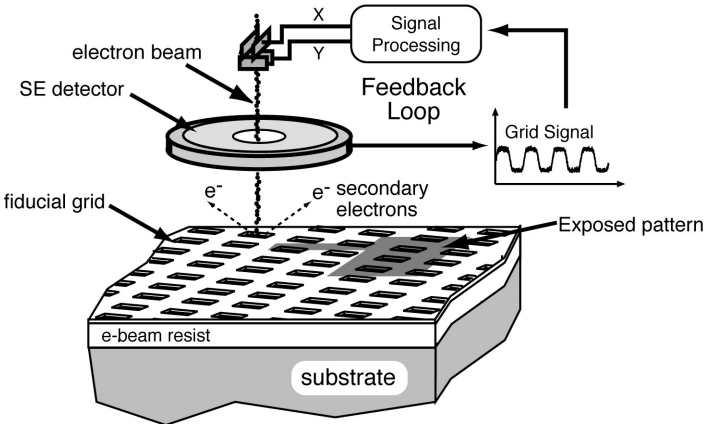

Fig. 4: Schematic of the global-fiducial-grid mode of spatial-phase-locked electron-beam lithography. The periodic signal detected from the fiducial grid is used to measure placement error, and feed a correction signal back to the beam deflection system.

We have implemented two modes of spatial-phase locking on a Raith 150 scanning e-beam lithography system. The Raith 150 is an inexpensive system that provides high resolution (sub-20-nm) patterning. It has little shielding from environmental disturbances and has a number of shortcomings with respect to pattern fidelity. Because the system can only reliably deflect the e-beam over a small area (~100 x 100 mm), patterns must be built up by stitching together an array of these fields. The best field-to-field stitching errors observed without spatial-phase locking have a standard deviation of ~8 nm.

continued

In the first mode of spatial-phase locking, the fiducial grid is segmented into small areas of the substrate that will not be patterned. Before exposing each stitched field, the electron beam scans over these areas and detects the spatial-phase of the grid. As a result, the field's shift, scaling, and rotation can be corrected before writing the pattern. This technique achieved field stitching errors with a standard deviation of 2.6 nm and has been used to expose 225-nm-period Bragg-grating filters in silicon-on-insulator waveguides.

To achieve maximum pattern-placement accuracy, it is desirable to constantly correct the beam position during exposure; to do so requires that the grid cover the entire substrate, but not perturb the electron-beam. Toward this end, we place a thin (<10 nm) metallic fiducial grid on top of PMMA e-beam resist. This grid produces a secondary-electron signal, while the primary electron-beam passes easily through to expose the resist below. Because the grid is conductive, it opens the possibility of obtaining higher signal-to-noise ratios through voltage contrast.

In order to implement the continuous-feedback mode, it was necessary to add raster-scan capability to the Raith 150. We added the required hardware and software to switch the beam on and off at desired times as the system raster-scans the beam across the field. In addition, we implemented hardware and software to measure the residual field distortion relative to the fiducial grid and to apply 3rd order corrections during the raster-scan exposures.

To provide continuous feedback control for beam positioning, we developed a phase-locking algorithm. The e-beam is scanned at an angle to the fiducial grid axes. This produces a signal with two fundamental frequency components whose phases are used to calculate the x- and y- beam-placement errors. To implement this algorithm, we added analog-to-digital conversion for the secondary electron signal, digital-signal processing with custom software for correction calculations, and digital-to-analog conversion for the x- and y- correction signals.

To evaluate the effectiveness of this algorithm, we exposed test patterns with a 10 keV electron beam using an 8-nm thick, 250-nm period, Al fiducial grid. Figure 5 shows stitching measurements of the resulting pattern with standard deviations at or below 1.3 nm. Locking to the fiducial grid ensures a comparable level of global pattern-placement accuracy. These experiments were conducted with patterns that do not require beam-current modulation to continuously track the grid. Developing appropriate current-modulating electron optics remains a high priority to enable patterning of arbitrary patterns. Another high priority for future research is to develop a means of putting down the fiducial grid that does require multi-step lithography.

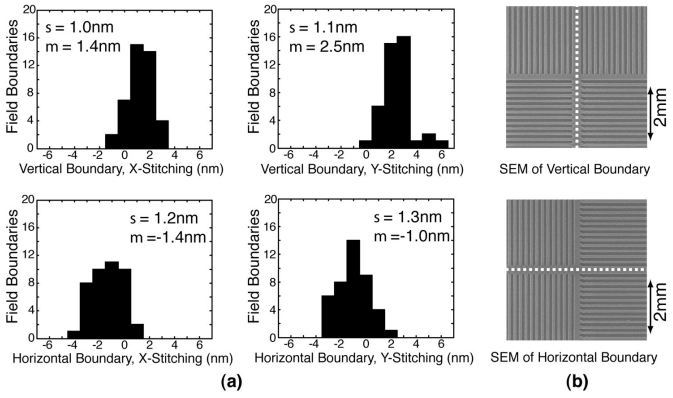

Fig. 5: (a) Histograms showing x- and y-stitching measurements at all 84 field boundaries of 49 stitched fields. Spatial-phase locking has reduced the standard deviation of the stitching errors to below 1.3 nm. (b) Sample 200-nm period stitched grating patterns. The dashed line indicates the field boundary.

Zone-Plate-Array Lithography (ZPAL): The System

Personnel
D. Gil, R. Menon, and A. Patel (H.I. Smith)

Sponsorship
DARPA and Army Research Office

In semiconductor lithography, glass masks are illuminated with deep UV laser light, and their image is reduced through a lens onto the substrate to define circuitry. As feature sizes are pushed towards 100 nm and smaller, lithography systems and masks are becoming increasingly complex and costly (~$1 million per mask set). In addition, the delay in obtaining a mask set, with complex optical-proximity correction and phase-shifting features can be months. This presents a huge hurdle to continuing progress in semiconductor technology.

At the MIT NanoStructures Laboratory, we are pursuing a radically new schem, which requires no mask called Zone-Plate-Array Lithography (ZPAL), made possible by inexpensive, high-speed computation and micromechanics. ZPAL replaces the "printing press" of traditional lithography with a technology more akin to that of a laser printer. Although it will not have the throughput of an optical stepper, ZPAL is ideal for prototyping and also for semiconductor products requiring only a few wafers, e.g., application-specific IC's.

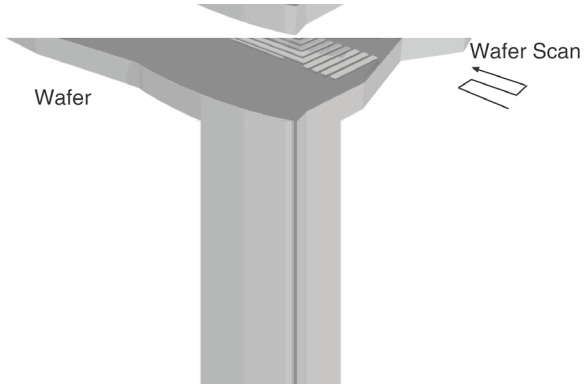

Fig. 6: Schematic of Zone-Plate-Array Lithography (ZPAL). An array of Fresnel zone plates focuses radiation beamlets onto a substrate. The individual beamlets are turned on and off by upstream micromechanics as the substrate is scanned under the array. In this way, patterns of arbitrary geometry can be created in a dot-matrix fashion. The minimum linewidth is equal to the minimum width of the outermost zone of the zone plates.

Instead of a single, massive lens, an array of hundreds or thousands of microfabricated Fresnel-zone-plate lenses is used, each focusing a beam of light onto the substrate. A computer-controlled array of micromechanical mirrors turns the light to each lens on or off as the stage is scanned under the array, thereby printing the desired pattern in a dot-matrix fashion. No mask is required, enabling designers to rapidly change circuit designs. A schematic of ZPAL is shown in Figure 6.

ZPAL leverages advances in nanofabrication, micromechanics, laser-controlled stages, and high-speed, low-cost computation to create a new form of lithography.

Recent research efforts have primarily concentrated on developing planar processes for fabrication of zone-plate arrays, proving the lithographic capabilities of zone plates, developing robust system-simulation tools and building a fast data-delivery system.

Fabrication of Phase-Zone-Plate Arrays

Phase-zone-plate arrays are fabricated using a process consisting of electron-beam lithography and self-aligned electrochemical etching. We use the negative e-beam resist HSQ (hydrogen silsesquioxane, by Dow Corning). HSQ's extraordinarily high resolution (~10nm) and its glass-like properties make it an optimal choice for fabricating diffractive-optical elements that operate in the UV and DUV regimes (See Figure 7). HSQ has an index of refraction very close to that of fused silica, and negligible absorption down to 157nm. The resist is first spun to the thickness corresponding to the desired phase step for the zone plate, patterned with e-beam lithography, and then the unexposed regions are developed away. It is also necessary to prevent the light from transmitting through those areas on the substrate not occupied by the zone plate. This is achieved by evaporating metal (chrome in this case) onto the substrate. Since the metal within the zones of the zone plate is electrically isolated from the metal outside,

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the metal within the zone plate can be removed by an electrochemical etching process (Fulton/Dolan Process).

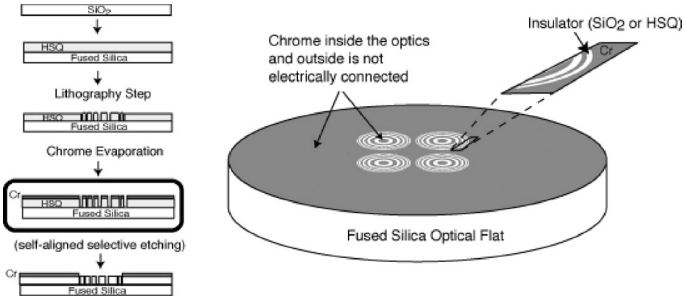

Fig. 7: Left: Typical sequence of the self-aligned process requiring a single-lithography step. Starting with a transparent blank material, HSQ is spun on it. The thickness of the HSQ is chosen to provide the appropriate phase step for the zone plate. After patterning the elements in HSQ, the absorber metal is evaporated. Right: Detail of the process after the absorber has been evaporated. Note that the absorber (chrome in this case) inside the zone plate and outside is not electrically connected. The lack of electrical connectivity will allow for the absorber within the diffractive elements to be removed by means of a wet-etch Fulton/Dolan technique.

Zone-plate arrays can be manufactured in a highly reliable manner. We have fabricated zone plates that perform very close to their theoretical limit (as shown in another section), and have manufactured arrays containing over 1,000 zone plates (See Figure 8). We believe much larger arrays, of ~1M zone plates, are possible.

System Simulation Tools

We have developed simulation tools to design zone plates as well as other diffractive focusing elements and to study the effect of various system parameters on the lithographic performance of ZPAL.

The simulation begins with modeling the diffraction of light by a zone plate using the finite-difference time-domain method. Calculated fields are further propagated to the focal plane of the zone plate using a vector

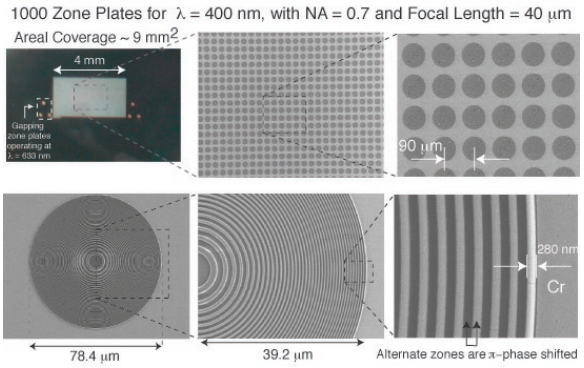

Fig. 8: Large zone plate arrays can be readily fabricated with our novel process that requires a single lithography exposure and no etching, even for the case of phase zone plates. Top-left: Optical micrograph showing an array containing over 1,000 zone plates with an aerial coverage of 9 mm². Bottom-right: Detail of the outermost zones. The duty-cycle is very close to 50%, and the phase shift between alternate zones was controlled to about 1%.

plane-wave spectrum method. Since this is a full-vector model of electromagnetic theory, it gives extremely accurate predictions about the spatial structure of the Point-Spread Function (PSF). This is illustrated in Figure 9, where the PSF of the zone plate was experimentally determined by exposing single spots at a large number of doses in photoresist. The photoresist, being highly nonlinear, acts as a sampler to obtain points on the PSF. The excellent agreement between the model and experiment attests to the model's accuracy as well as the reliable fabrication of the zone plates.

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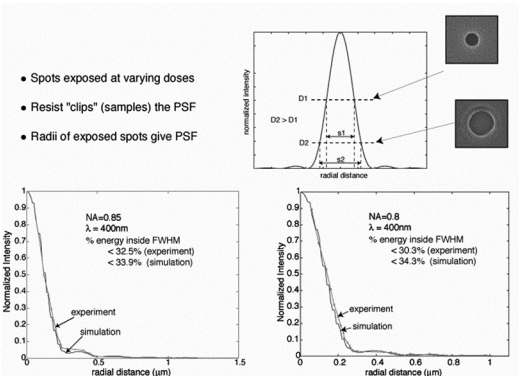

Fig. 9: Top: Experimental process for quantifying the PSF. Spots of several exposure times were patterned in photoresist, which acts as a sampler of the PSF. The radii of the exposed spots can be assembled to form the PSF. Bottom: PSFs for zone plates of NA=0.85 (left) and NA=0.8(right) were determined experimentally using the simulation tools. The results show excellent agreement.

Since ZPAL results in an incoherent addition of spots in photoresist, by convolving the PSF with a desired pattern, we can simulate exposed patterns. This is important to understand various component-tolerances in the system.

Micromechanics & Data Delivery System

We have switched from the previously reported method of multiplexing the light for ZPAL, the Texas Instruments DMD™ micromirror array, to the Silicon Light Machines Grating Light Valve™ (GLV™) linear array. Although the GLV™ has a smaller number of pixels (1,088) compared to the DMD™ micromirror array (~1 million or more), the higher speed of operation of the GLV™ (20ns rise time as opposed to 20 ms for the DMD™), the fact that gray-scaling is built in, and its diffractive mode of operation (making it compatible with shorter wavelengths, possibly even down to 157nm) made it a superior choice for ZPAL.

The GLV™ is a micromechanical phase grating consisting of parallel rows of reflective Al ribbons. Alternate rows of ribbons can be pulled down electrostatically in a controlled manner to create diffraction effects on incident light. When no force is applied, all the ribbons lie in the same plane. If illuminated, incident light will be reflected from their surfaces at the same angle at which it is incident. When alternate ribbons are pulled down, a grating structure is created. In this state diffraction will produce light at an angle different from that of the incident light. By alternating between these two states (i.e. from flat ribbons to a grating structure), the GLV™ can switch light ON and OFF. Furthermore, by tuning the applied electrostatic force, the depth to which the ribbons are pulled down can be controlled, impacting the amount of light diffracted into the first order. Grayscaling of the incident light can be achieved in this manner. Each of the 1088 pixels present in the linear array can accept 8-bits of grayscaling (256 levels). Since the motion involved in switching the pixels of the GLV™ is small (one-quarter wavelength), the GLV™ is capable of very high switching speeds, with a rise time from the ON to the OFF position of only 20ns. One pixel of the linear array is depicted schematically in Figure 10, along with the intended implementation in ZPAL.

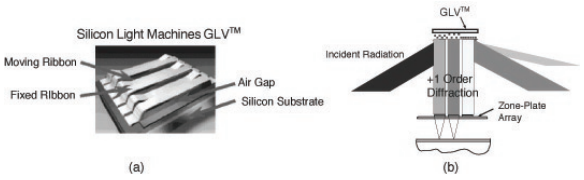

Fig. 10: Schematics of the Silicon Light Machines Grating Light Valve (GLV) device. (a): Fixed and electrostatically-deflected moving ribbons create a variable-height grating. (b): Incident light will be diffracted from the grating at a known angle, with varying intensity depending on the height of the grating. Each pixel, a small patch of the grating, diffracts onto a single zone plate, thus turning on and off (or grayscaling) each pixel written onto the substrate in ZPAL.

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We have built a custom system to deliver the pattern data from the ZPAL control computer to the 1,088 pixels of the GLV™ array at very high speeds. Data is first transferred from the computer through the PCI bus to a National Instruments digital I/O board (Model#: 6601). The data is then sent from the I/O board to the GLV™ through a custom-made Printed Circuit Board (PCB) which performs the data routing and interpretation as required by the GLV™ electronics. The I/O board, equipped with an 80 Mhz clock to enable clocking the data at very high speeds, has the capability of both reading data from the control computer and sending data to the GLV™ simultaneously. In practice, two I/O boards are used in parallel to achieve high data rates. All the software was written in LabView on a Dell windows workstation.

In order to test the data delivery system, we have built an experimental setup as shown in Figure 11(a). Light from a Helium-Neon laser is collimated and directed onto the GLV™. A lens is used to focus the 1st order diffracted beam onto a detector. We send data to the GLV™ and measure the modulation of the light on the detector. Figure 11(b) shows the detector signal as a function of time when the GLV™ was driven with "ON-OFF" data at a frequency of 7.5 kHz (the specification required for our prototype system), corresponding to an average data transfer rate of 130 Mbits/s. The vertical axis is the detector voltage, but it was not calibrated and hence, is not labeled in the figure.

Since the GLV™ is capable of operating at much higher frequencies (~500 kHz), we tested our system to determine the limits of the data delivery architecture, even though our requirements had been successfully met. Figure 11(c) shows the GLV™ operating at a frequency of 66.67 kHz, corresponding to a data transfer rate of about 1Gbit/s. At present, we were limited by the response time of our detector, but data from our logic analyzer indicates that we can successfully send rates in excess of 100 kHz with our current

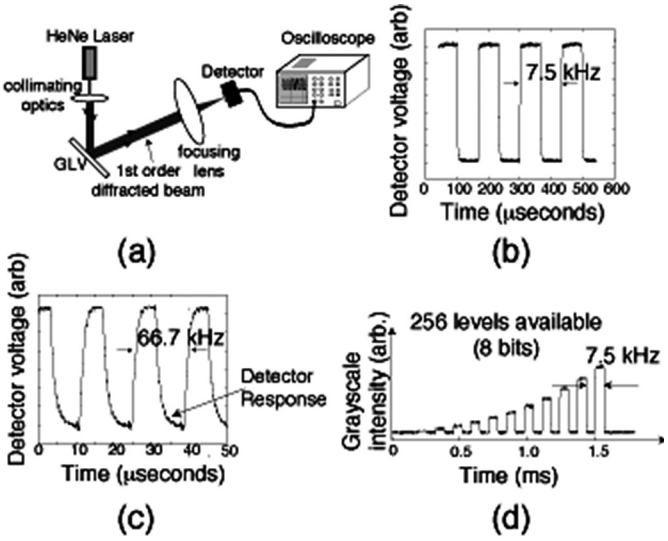

Fig. 11(a): Schematic of the experimental setup for testing the data delivery system for ZPAL. (b) The GLV operating at 7.5 kHz, the required speed for our prototype system. (c) The GLV operating at 66.67 kHz, corresponding to a 1Gbit/sec data rate. (d) Grayscaling at 7.5 kHz

implementation. Since dose control is an important requirement for good lithographic performance, the ability to grayscale is paramount in any multiplexing device to be employed in a ZPAL system. The GLV™ offers 8-bits of grayscaling (256 levels), 3 bits more than what is needed for our writing strategy, which requires 5-bits. As shown in Figure 11(d), our data-delivery system is capable of achieving all 8-bits of grayscaling without sacrificing switching speed.

Interference Lithography for Patterning Variable-Period Gratings

Personnel
C. Chen, C.-H. Chang, C. Joo, P. Konkola, J. Montoya, and R. Heilmann (M.L. Schattenburg)

Sponsorship
NASA

Scanning-Beam-Interference Lithography (SBIL) patterns large-area, linear, low-phase-distortion gratings with a pair of small diameter (millimeter size) phase-locked laser beams. We are developing a prototype system that generalizes the concept of phase-locked scanning beams for patterning continuously varying (chirped or quasi-periodic) patterns. These structures can subsequently be used to fabricate chirped X-ray reflection gratings for astronomical imaging applications, chirped fiber Bragg gratings for time-delay or spectral filtering applications, and/or diffractive optical elements.

Figure 12 shows the experimental diagram of the Variable-Period Scanning-Beam Interference-Lithography (VP-SBIL) system. For controlling the grating period and orientation, the system employs dual-axis picomotor-driven gimbal mirrors to produce symmetric deflections of a pair of interfering beams around the optical axis without translation. Two objective plano-convex lenses (f# = 4.25, 2.12) are used in a 4-f optical configuration. Such a lens system allows the conjugate points of beam deflection (on mirrors) to overlap at the focal plane of the second objective lens. The spot size of image overlap is reduced to half the beam diameter as the ratio of focal lengths f_2/f_1=0.5. This relaxes the maximum period variation ($\Delta\Lambda$) constraint over the image diameter (D) that requires $\Delta\Lambda/\Lambda << \Lambda/D$ where Λ is the grating period.

To attain phase stability during grating patterning, homodyne fringe locking is adopted using an imaging detector, analog fringe-locker and a piezo-actuated mirror in closed-loop. In the present experimental configuration, two-axis beam rotation can generate any fringe orientation. However, variation in grating period (~1000 to 2 μm) is limited by the range of deflection produced by the gimbal mirrors (± 10°) and by the numerical aperture (NA) of the lens system. Using position-sensitive detectors with an appropriate imaging and Fourier lens configuration, closed-loop beam steering is implemented to vary the grating period and orientation in a predetermined fashion. Typical requirements for x-ray reflection grating fabrication are Λ_{ave}~ 2 μm and chirp factor $\Delta\Lambda/\Lambda$ ~ 5%.

Figure 13 shows two grating images of period 2.0 μm and 4.0 μm obtained on a static substrate by changing the angle between the beams using the picomotor-controlled gimbal mirrors. Line uniformity in the images indicates minimal fringe distortion over the entire beam overlap. The picomotors can be constantly driven to write large-area gratings with continuously varying period and orientation on a substrate mounted to a precision X-Y stage. The Piezo-actuated picomotors (which produce displacement jitter and exhibit low bandwidth operation) will be subsequently replaced by voice coil-actuated fast steering mirrors.

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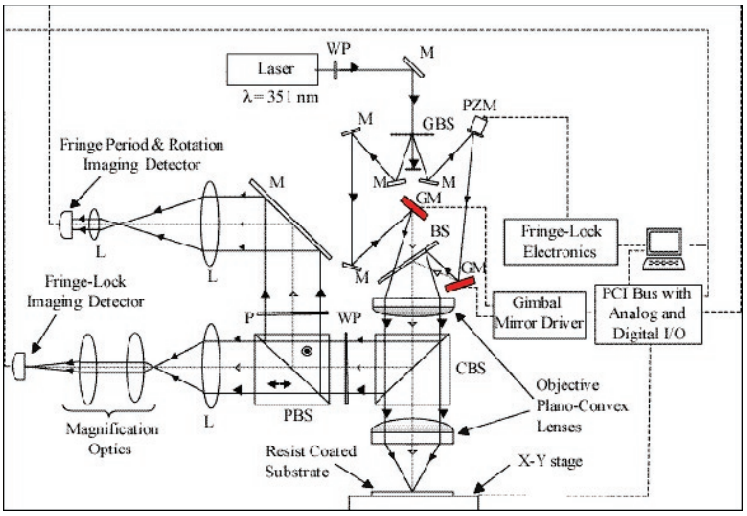

Fig. 12: Experimental diagram of variable-period scanning-beam interference-lithography system. M: mirror, L: lens, P: polarizer, GM: gimbal mirror, WP: wave plate, BS: beam splitter, PZM piezo-actuated mirror, GBS: grating BS, CBS: cubic BS, PBS: polarizing BS.

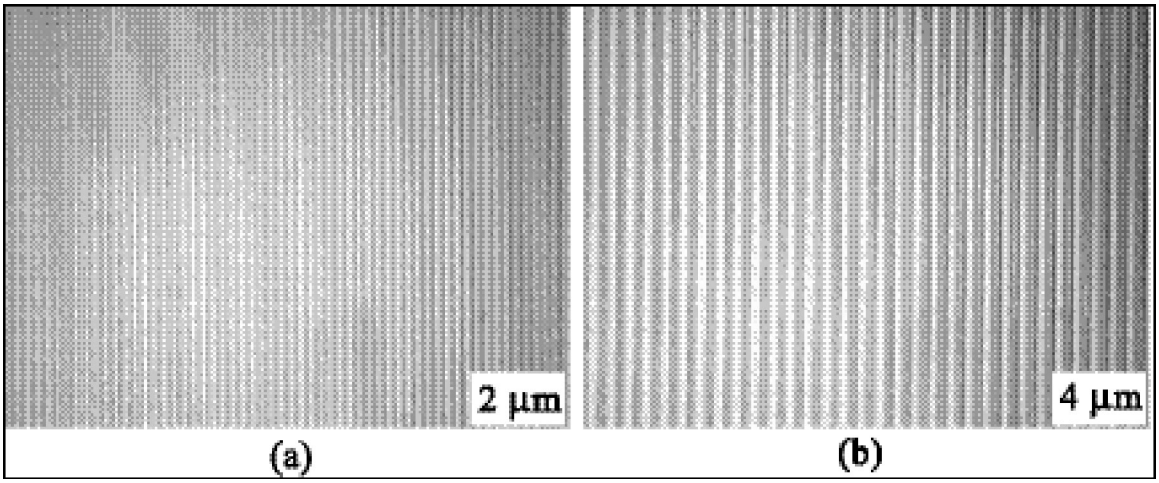

Fig. 13: Grating images written by VP-SBIL with period (a) 2.0 mm and (b) 4.0 mm.

Zone-Plate-Array Lithography (ZPAL): Lithographic Performance

Personnel
D. Gil, R. Menon, and A. Patel (H.I. Smith)

Sponsorship
DARPA and Army Research Office

In a direct-write system such as ZPAL, the major figures-of-merit are resolution and contrast. The resolution is quantified by the following equation:

(1) $$W_{min}=\lambda/NA$$

where Wmin is the minimum feature size, NA is the numerical aperture of the zone plate, lambda is the exposure wavelength, and k1 is a proportionality factor that, in effect, indicates how close to theoretical limits one operates.

In order to reduce the minimum feature size, one can increase the NA of the zone plates. The results presented in Figure 14, using NA=0.9, are the highest quality lithographic patterns ever produced with ZPAL, showing good fidelity, low edge roughness, and the ability to pattern very dense features down to the minimum spot size. It is worth noting that since all exposed pixels received the same dose, proximity effects are minimal in the exposures.

The ability to pattern curved structures and non-manhattan geometries is important for a number of applications, and our ZPAL system, by employing sub-pixel stepping, can satisfy these needs, as illustrated in Figure 15.

The minimum feature size can be further reduced by reducing k1. This corresponds to decreasing the size of the address grid, as illustrated in Figure 16.

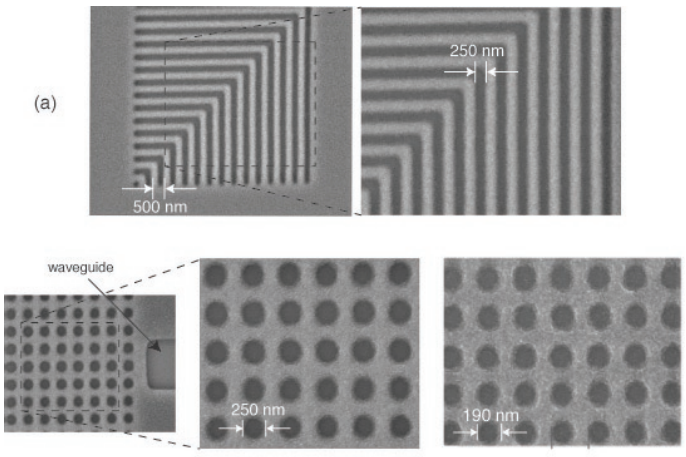

Fig. 14: Scanning electron micrographs of patterns exposed with our continuous-scan 0.9 NA UV-ZPAL system operating at λ = 400nm. (a) Dense nested Ls, (b) 2D photonic bandgap structures with 500 nm period, (c) 2D photonic bandgap structures with 360 nm period.

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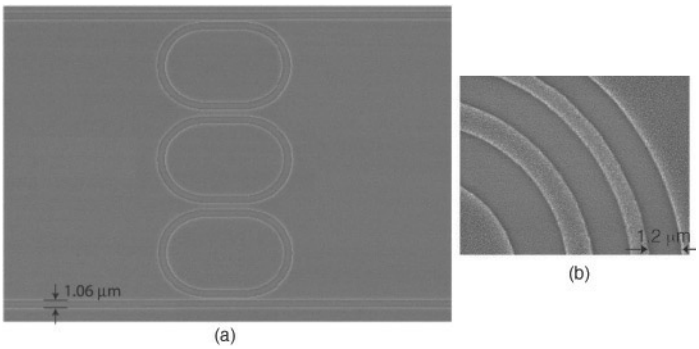

Fig. 15: Scanning electron micrographs of patterns exposed with our continuous-scan 0.9 NA UV-ZPAL system operating at λ = 400nm. Sub-pixel stepping enables patterning of curved structures with smooth edges. (a) waveguides with ring resonators, (b) one quadrant of a zone plate.

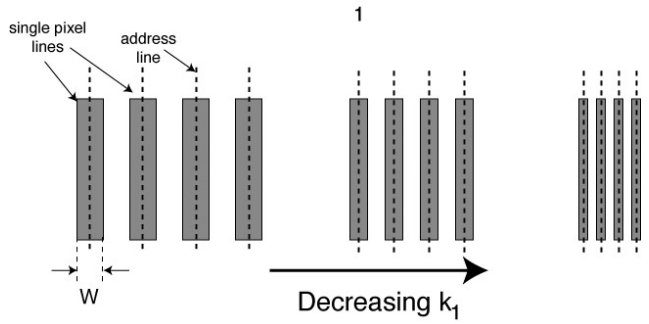

Fig. 16: k1 in ZPAL. Decreasing k1 decreases the minimum feature size. This is done by decreasing the address grid of the system, i.e., the scan lines of the focused spot are brought closer together as shown. At some point, the final image will not have sufficient contrast to be resolved by the photoresist. That point determines the limiting k1 factor.

Figure 17 shows a set of scanning electron micrographs of dense lines and spaces with varying k1's, from 0.56 to 0.38. We are currently exploring the limits of how much lower we can go, since even at k1 = 0.38 the quality of the patterning remains remarkable. Systematic characterization of lithographic exposures has also allowed us to determine that the process latitude for our current system is around 13% (even when operating at k1 = 0.38). We believe the superior lithographic performance of ZPAL is connected with the fact that there is no phase relationship between sequentially exposed spots (i.e., incoherent imaging).

Image contrast is an important lithographic-figure-of-merit. This is particularly important since phase zone plates have higher (odd) diffraction orders which contribute to the background. Here, we show that large area patterning is indeed possible with zone plates, even without order-sorting apertures, and at very high numerical apertures.

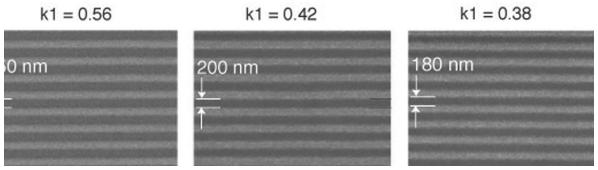

Fig. 17: Exploring the limits of k1 with ZPAL. High-numerical-aperture zone plates (0.85 and 0.9) can operate at low k1 factors (below 0.4). Sub-70 nm patterning should be possible, by operating at the demonstrated k1=0.39, with 0.9NA zone plates and λ = 157nm.

For evaluating contrast, it is sufficient to pattern full fields at the maximum resolution. Figure 16 demonstrates that full fields of dense lines and spaces can be written with high-NA zone plates. The top of the figure provides a schematic of ZPAL (without the micromechanics), illustrating the concept of parallel writing by stitching multiple fields. The bottom of the figure contains an experimental result in which we exposed fields of 125µm x 125µm (currently the scanning limit of our stage) with a 0.9 NA zone plate operating at λ=400nm and a focal length of 40 µm. A field of 125µm x 125µm corresponds to the area under a 0.85 NA zone plate, as indicated in the figure. The exposed pattern consists of 1:1 dense lines and spaces

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with a period of 440nm. The zoomed in scanning-electron micrograph of the bottom-right of Figure 18 provides a clear view of what the pattern looks like, namely a 440nm-period dense 1:1 grating.

In summary, our results provide hard evidence that high-numerical-aperture zone plates are capable of providing sufficient contrast for state-of-the-art lithography. Although multiple diffracted orders exist, the background exposure that they produce is not deleterious. Moreover, the background can be further reduced by the utilization of order-sorting apertures.

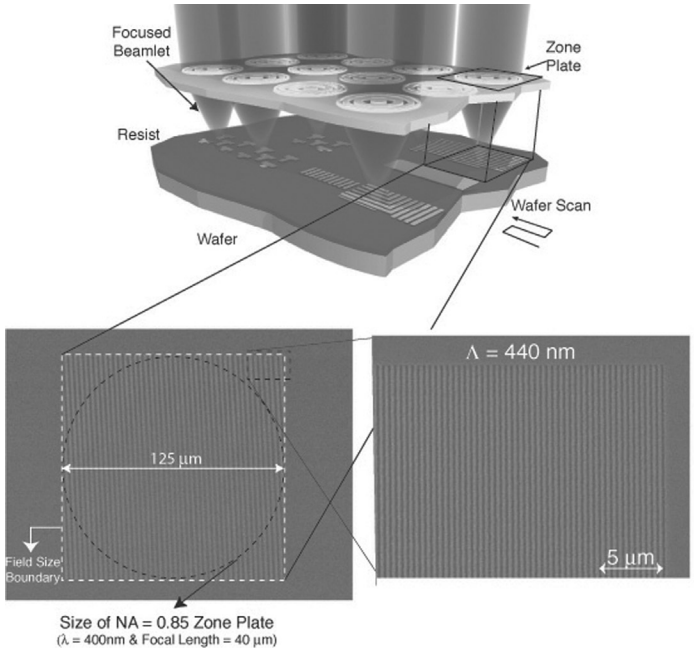

Fig. 18: Top: Schematic of the ZPAL system without the micromechanics. Large-area patterns are created by stitching adjacent fields, with a field defined as the square area located underneath any given zone plate. Bottom-left: Proof that full-field patterning is possible with ZPAL despite the existence of multiple orders. A dense 1:1, 440nm-period grating was exposed (with 400nm wavelength) covering the area of a 0.85 NA zone plate. Note that the inclined periodicity (~3μm period) observed in the left scanning-electron micrograph is the result of a moiré effect (resulting from the beating of the periodic sampling of the SEM with which the picture was acquired and the periodicity of the exposed grating. Bottom-right: Zoomed in SEM of the top-right corner of the large area grating.

X-Ray Nanolithography

Personnel
L. Chen, J.M. Daley, and E.E. Moon (H. I. Smith)

Sponsorship
DARPA and University of Wisconsin

For several years, we have been developing the tools and methods of X-ray nanolithography. We have explored the theoretical and practical limitations and have endeavored to make its various components (e.g. mask-making, resists, electroplating, sources, alignment, etc.) reliable and "user-friendly." Because of the critical importance of X-ray mask technology, we discuss this in a separate section.

X-ray NanoLithography (XNL) is a reliable and simple means of replicating patterns with feature sizes down to about 20 nm. Typically, the X-ray mask is made with Scanning-Electron-Beam Lithography (SEBL), although we very often employ a combination of interference lithography, photolithography, SEBL, and XNL to fabricate the mask. Once the mask is fabricated, it can be replicated an unlimited number of times. The simplicity and process latitude of XNL make it ideally suited for nanostructures research. In fact, at the present time, XNL is the only technique available for replicating sub-100 nm patterns of arbitrary geometry.

In the NanoStructures Lab (NSL), X-ray lithography is used in the fabrication of a large variety of structures and devices, including: photonic bandgap devices, short-channel MOSFETs, and optical channel-dropping filters.

Our sources for X-ray nanolithography are simple, low-cost electron-bombardment targets. We utilize the L line of copper at $\lambda = 1.32$ nm. The sources are separated by a 1.5 μm-thick SiN_x vacuum window from a helium-filled exposure chamber.

We have submitted a proposal to DARPA for the purchase of a laser-plasma source from JMAR, Inc. Their source operates at a wavelength of 1.1 nm which is very close to the wavelength we currently use. Figure 19 is an example of some lithography done with the JMAR source using an MIT mask. Acquisition of a JMAR laser-plasma source should enable us to reduce our exposure times from hours to minutes.

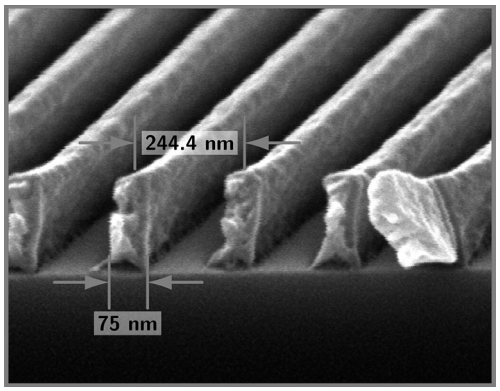

Fig. 19: Example of X-ray lithography done with the JMAR laser plasma X-ray source.

Although the wavelength used is very short (1.32 nm) compared to the minimum feature sizes of interest (e.g., 20 nm), diffraction in the gap between the mask and the substrate can be detrimental. For example, with a Cu_L source, a 50 nm feature must be exposed at a mask-to-substrate gap of less than about 4 μm in order to maintain good process latitude. A 25 nm feature would require a gap of 1 μm. For very small features, we eliminate the gap and use contact between the substrate

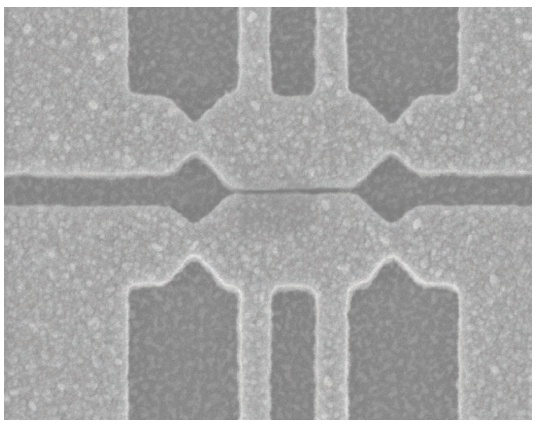

Fig. 20: Scanning electron micrographs of device pattern with feature size ~ 20 nm achieved by X-ray nanolithography.

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and the flexible membrane mask. This technique has enabled us to replicate features as small as 20 nm in a practical, reproducible way. Figure 20 shows scanning electron micrographs of device patterns with feature sizes less than 40 nm.

We are currently investigating if gaps below 4 μm can be reliably measured and controlled. For this, the substrate will have to be much flatter than 1 μm, something that is easily achieved with an appropriate pin chuck such as those used in optical projection lithography steppers. In fact, for the same minimum linewidth, the control of substrate flatness in X-ray lithography is less critical than in optical projection lithography by a factor 13. For a linewidth control of 10%, the control of gap in X-ray lithography is given by $\Delta G=0.2\ G$.

At linewidths of 25 nm and 50 nm, the allowable gap variation is 680 nm and 170 nm, respectively. Since the mask, if made properly, can be optically flat, the only contributor to gap variation is non flatness of the wafer or tilt of the mask relative to the wafer. We believe these can be controlled to meet the above requirements. For measuring gaps below 4 μm, we will use the "transverse chirp gapping" scheme described elsewhere in this report.

Another approach to achieving extremely fine linewidths is to use a much shorter wavelength, around 0.5 nm. At this wavelength, the high-atomic-number materials such as gold, tungsten and tantalum, and their alloys have X-ray attenuation comparable to that at a wavelength of 1 nm. The shorter wavelength enables one to use a larger gap between mask and substrate for the same resolution. The penalty one pays is that the attenuation of resist is significantly reduced, necessitating the doping of the resists with materials such as chlorine or bromine. Another issue is the energetic photoelectrons emanating from the substrate. Their deleterious effect can be eliminated by using a trilayer resist, with the bottom buffer layer absorbing the energetic photoelectrons. We are collaborating with F. Cerrina at U. Wisconsin and T. Kitayama of Mitsubishi in the development of this shorter wavelength approach.

Nanometer-level Feedback-Stabilized Interferometric Aligning and Gapping in an X-ray Lithographic System

Personnel
E. E. Moon, L. Chen, and P. N. Everett (H. I. Smith)

Sponsorship
JMAR/SAL Incorporated and University of Wisconsin

An experimental X-ray exposure system has been constructed that employs Interferometric-Spatial-Phase Imaging (ISPI) for high-precision aligning and gapping. The ISPI scheme utilizes grating and checkerboard marks on mask and substrate. When illuminated with oblique-incidence spatially-coherent light, interference patterns are formed, which are imaged by f/10 optics at a 22 degree angle from the X-ray beam at a 110 mm working distance. Since the microscopes and illumination are removed from the path of the x-ray beam, alignment and gap are detected and feedback-controlled during, as well as before, exposure.

As shown in Figure 21, each alignment mark consists of three gratings (or checkerboards), of slightly different periods, p_1 and p_2, arranged so that the two outer gratings with p_1 (on the mask) are superimposed over p_2 checkerboards (on the substrate). In the middle of the three-part mark, a p_2 grating is superimposed over a p_1 checkerboard. In this arrangement, when the mask is moved relative to the substrate, interference fringes from the middle part of the mark move in the opposite direction of the fringes from the outer parts. Alignment is determined from the relative spatial phase between the middle and outer fringe sets, measured with a sub-nanometer sensitivity frequency-domain algorithm. Phase bias due to rotation of the camera with respect to the mark is removed by examining the spatial phase difference between the two outer fringe sets.

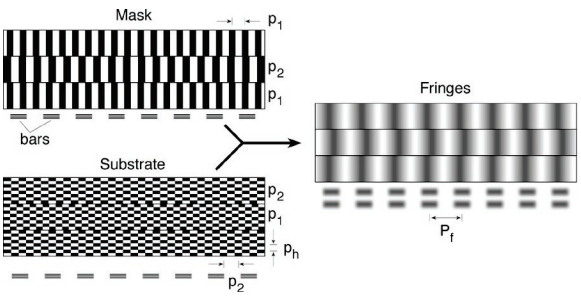

Fig. 21: Schematic of ISPI aligning marks. Fine alignment is detected using the spatial phase relation of middle to outer fringe sets. Errors from camera-mark rotation are removed by phase comparison of outer fringe sets. Spatial-phase ambiguity is eliminated by comparing the phase between bar arrays on the mask and wafer, as well as between bars and fringes.

Gap is measured from checkerboards on the mask, which have a constant period in the plane of illumination, but a varying, or chirped, period in the transverse plane. Three chirped gratings are used, with the middle chirp in the opposite direction from the outer chirps. Constant-period fringes can be obtained by design of the chirp rate. In a manner similar to that for alignment, the spatial phase of the fringes encodes gap information. In addition to phase, average intensity and fringe frequency also vary with gap. Fringe frequency variation is indicated in Figure 22, where a middle and outer fringe pair are shown at gaps of (a) 4.3 mm and (b) 19.3 mm. Fringe frequency can be used to resolve gaps to +/- 1 mm.

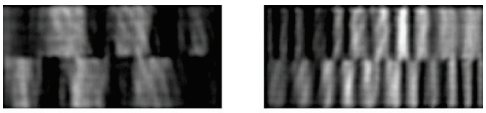

Fig. 22: Illustration of fringe variation with gap. Between (a) 4.3 mm and (b) 19.3 mm gaps the number of fringes increases by 0.51 fringe/mm.

To increase gap resolution, frequency, phase and average intensity of the transverse chip fringes are used simultaneously. The data from a gap scan between 6 and 8 μm (with 5 nm gap steps) is plotted in Figure 23(a). The same three quantities are plotted in three dimensions in Figure 23(b). The curve in Figure 23(b) traces out a highly repeatable, pseudo-helical path that indicates a unique gap within the 2-mm range. The observed gap detectivity of <20 nm is more than adequate for linewidth control of sub-50 nm features in proximity X-ray lithography.

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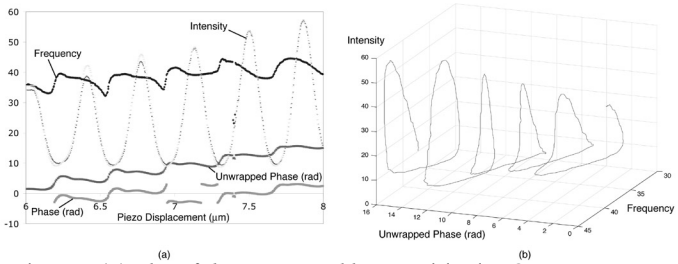

Fig. 23: (a) Plot of three measurable quantities in ISPI transverse chirp gapping fringes: frequency, phase, and average intensity as a function of gap. (b) Within the +/- 1 range of fringe frequency resolution, a unique correspondence to gap is found from a combination of all three fringe quantities. (Note that in both plots frequency is upshifted by ~4x due to zero padding.)

The same ISPI microscopes are used to detect both alignment and gap, however, alignment and gap have distinct (and conflicting) illumination requirements. Aligning is fundamentally achromatic, so any wavelength within a wide range can be used. In practice, it is advantageous to use multiple laser lines to avoid thin-film interference effects that could cause signal extinction at certain resist thicknesses. Gapping, on the other hand, is intrinsically dependent upon wavelength. Indeed, phase, frequency, and intensity in the gap marks all vary with illumination wavelength. Multiple wavelengths, if used simultaneously, would cause confusion from several sets of gap fringes. To meet both requirements, a Closed-Loop Variable Bandwidth light source (See Figure 24) is used to provide a narrow bandwidth for gapping or a broad band for aligning. The CLVB source consists of four diode lasers in the range between 635 and 690 nm, four fiber-coupled beamsplitters, and a compact spectrometer with USB computer link, which permits equalization of the power in the spectral lines during aligning, or measurement of the exact wavelength of a single laser line for gapping.

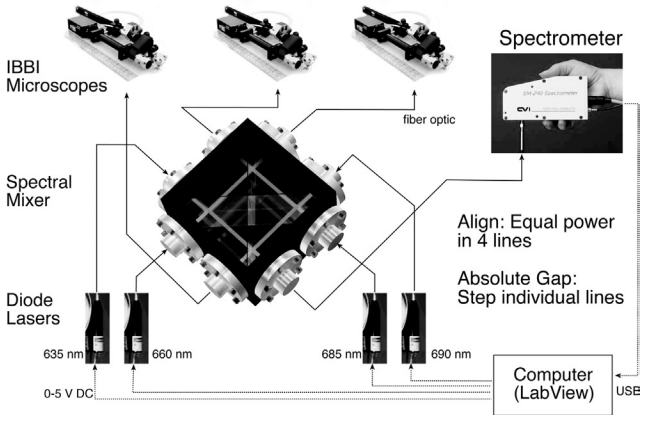

Fig. 24: A Closed-Loop Variable Bandwidth (CLVB) light source provides optimum illumination for both aligning and gapping. A single laser line is used for gapping, but a broad spectrum using multiple lasers is ideal for aligning. The spectrometer monitors wavelength when gapping, and relative intensities when aligning.

The unique collection of capabilities inherent to ISPI aligning and gapping is being employed in the fabrication of a variety of electronic and optical devices.

Adaptive-Membrane-Mask Technology

Personnel

J.M. Daley and T.B. O'Reilly (G. Barbastathis and H. I. Smith in collaboration with M. Feldman, LSU)

Sponsorship

DARPA/Naval Air Systems Command and Louisiana State University

The conventional approach to maintaining pattern fidelity and overlay in lithography is to minimize distortion in pattern generation and transfer, and to make masks as rigid as possible. Since July 2000, we have been pursuing a radically new approach that seeks to exploit the flexibility of membrane masks. This approach, which we call the Adaptive Membrane Mask (AMM), seeks to actively measure and control mask distortion, making it possible to eliminate or compensate for many types of distortion common in lithography. This approach is similar in spirit to adaptive optics where optical surfaces are actively deformed to compensate for system or media distortions.

Our approach to distortion measurement is based on holographic interferometry. A reference grid is fabricated on the back of a membrane mask using Interference Lithography (IL). Mask distortion is measured using the Holographic-Phase-Shifting Interferometer (HPSI), shown in Figure 25, essentially an IL system modified to measure in-plane distortion of the reference grid on the membrane. We believe that HPSI will be able to measure in-plane distortion of the mask with resolution of the order of 1 nm.

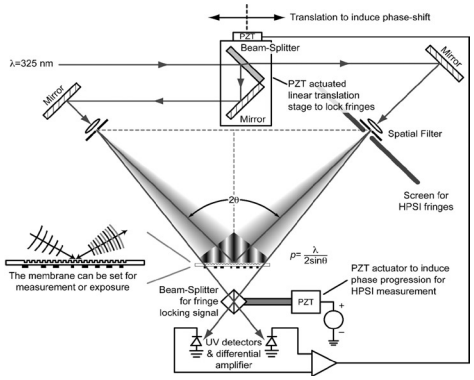

Fig: 25: Schematic of the Holographic-Phase-Shifting Interferometer(HPSI). This setup can be used as an interference lithography system to write reference grids as well as a holographic interferometer to measure grid distortion.

Once the distortion is measured, an algorithm developed at MIT is used to calculate the temperature distribution that will generate thermal stresses to eliminate the measured distortion. The membrane mask is heated using a computer-controlled illumination source, based on either a spatial light modulator, such as the Texas Instruments digital micromirror array, or a scanned laser system. The distortion is measured again, and the process is repeated iteratively until the distortion is eliminated. The final temperature distribution is measured using an infrared camera. The

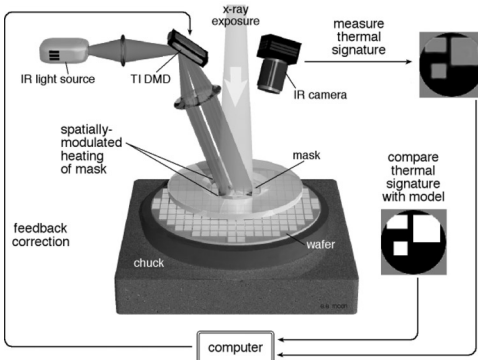

Fig. 26: Proposed implementation of Adaptive-Membrane-Mask Distortion Correction

proposed implementation is outlined in Figure 26. Because membrane distortion is directly related to temperature, it can be eliminated by maintaining this final temperature distribution.

The AMM approach is ideally matched to X-Ray Lithography (XRL). The primary sources of distortion in XRL are distortion of the mask due to stresses in the absorber layer and by radiation damage. XRL membrane masks used in industry are typically 2 microns thick silicon carbide, which is not subject to radiation damage at exposure levels seen in industry. The ability to measure and correct distortion may allow

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the use of a wider range of materials for both membrane and absorber, and relax some process constraints currently needed to minimize absorber stress. For instance, masks can be made from silicon nitride, which is less expensive and easier to make than silicon carbide, but is subject to radiation-damage-related distortion. The use of thinner membranes has the additional advantage of reducing exposure times and increasing optical transmission for mask alignment.

An AMM can be used to provide magnification correction. AMM can also be used to correct for wafer distortion, which can arise from a number of causes: high temperature processing, stress in grown overlayers, stress due to ion implantation, etc. As long as these distortions are measurable and repeatable, an adaptive mask can compensate for them, allowing more flexibility in wafer processing. For example, high temperature processes that induce wafer distortion can be used since the AMM can compensate for them. The advantages described above also apply to the use of AMM with types of lithography other than XRL that use membrane or stencil masks, including electron, ion- and neutral-atom lithography. In addition, we believe that adaptive masks may be applicable to Optical-Projection Lithography (OPL), by far the dominant technique for fabricating semiconductor chips. Although rigid masks are currently used in OPL, reducing the importance of distortion in the mask, OPL is subject to all of the other types of distortion described above. In addition, the projection lens system introduces distortion in the image produced on the substrate. Application of AMM to OPL should allow control of this distortion and may allow the use of simpler projection lens systems.

Preliminary work has shown good agreement between experiment and model. Figure 27 compares experimental and analytical results for a simple case where the left half of the membrane is heated. Here, displacements are plotted along a horizontal line in the middle of the membrane.

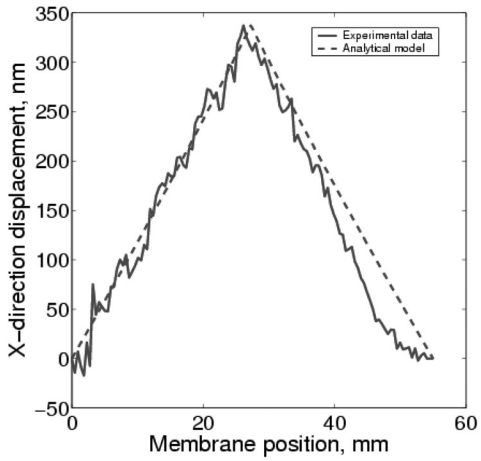

Fig. 27: Comparison of experimental and analytical results

Interference Lithography

Personnel

J.M. Carter, R.C. Fleming, T.A. Savas, M.E. Walsh, and T.B. O'Reilly (M.L. Schattenburg and H.I. Smith)

Sponsorship

DARPA and U.S. Army Research Office

Interference Lithography (IL) is the preferred method for fabricating periodic and quasi-periodic patterns that must be spatially coherent over large areas. IL is a conceptually simple process where two coherent beams interfere to produce a standing wave, which can be recorded in a photoresist. The spatial-period of the grating can be as low as half the wavelength of the interfering light, allowing for structures of the order of 100nm from UV wavelengths; features as small as 30-40 nm are also possible using a DUV ArF laser.

The NanoStructures Lab has been developing IL technology for close to 20 years, and we currently operate 4 different IL systems for a wide variety of applications. One system, shown schematically in Figure 28, is run in cooperation with the Space Nanotechnology Lab. This system is specially designed for high stability and repeatability and is capable of producing metrological quality gratings and grids up to 10 cm in diameter at spatial periods down to 200nm. Used primarily for satellite applications, gratings produced with this tool have flown on numerous missions, most notably, the Chandra X-ray astronomy satellite launched in August of 1999, which included hundreds of matched, high-precision gratings.

We operate another system similar to the one shown in Figure 28 based around the 325 nm line of a HeCd laser. This system functions both as an exposure tool with capabilities comparable to those described above as well as an analysis tool. Using a technique known as Holographic Phase-Shifting Interferometry (HPSI), the linearity and spatial phase of gratings produced in this system can be quantitatively measured and mapped with an accuracy on the order of parts per million. Known hyperbolic distortions in the spatial-phase of gratings printed using IL are responsible for changes in periodicity of a few angstroms (for a 200nm period grating) over a 10 cm wafer. Although seemingly small, distortions of this scale can be highly

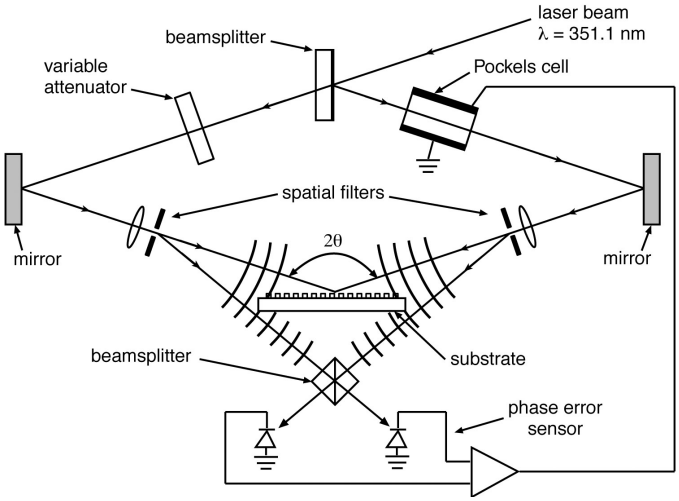

Fig. 28: Schematic of one of the MIT interferometric lithography systems. This system occupies a 2x3m optical bench in a class 100 clean environment. The beamsplitter directs portions of the two interfering spherical beams to photodiodes. A feedback locking is achieved by differentially amplifying the photodiode signals and applying a correction to the Pockels cell which phase shifts one of the beams in order to stabilize the standing wave pattern at the substrate.

significant, especially in metrological applications such as the fiducial grids for spatial-phase locked electron beam lithography. Using the HPSI, we have been able to investigate innovative techniques for reducing these distortion levels. One method, based on the controlled bending of the substrate during exposure, has demonstrated a reduction of the distortion pattern from 2 dimensions to 1 dimension as well as reducing the magnitude of the distortions by about a factor of 5.

Also utilizing a 325 nm HeCd laser is the Lloyds-mirror interferometer, shown schematically in Figure 29. The primary advantage of the Lloyds-mirror is that the spatial-period of the exposed gratings can be easily and continuously varied from many microns down to ~170 nm simply by rotating the stage without realigning the

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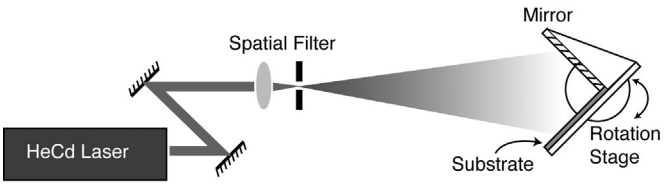

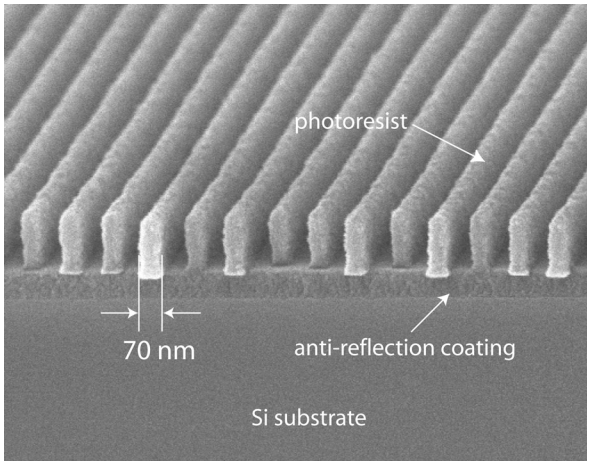

Fig. 29: Schematic of a Lloyds-mirror interferometer. The substrate and mirror are fixed at a 90˚ angle to one another, and centered in a single incident beam. Rotating the substrate/mirror assembly about its center point varies the spatial-period of the exposed grating. The micrograph shows a grating with 70 nm lines on a 170 nm pitch exposed using the Lloyds-mirror.

optical path. This has opened the door to new possibilities such as varied aspect-ratio grids (different periodicities in the two axes of the grid) for patterned magnetic media and MRAM (Magnetic Random Access Memory) devices. Among the many other applications of IL supported by the Lloyds-mirror are alignment templates for organic crystals and block co-polymers, semiconductor quantum dots, and other self-assembling structures.

Distributed FeedBack (DFB) structures for quantum dot lasers and photonic bandgap devices have also been made using the Lloyds-mirror.

For spatial periods of the order of 100 nm, we use a 193 nm ArF laser. To compensate for the limited temporal coherence of the source, we utilize an achromatic scheme shown in Figure 30. In this configuration the spatial period of the printed grating is dependent only on the period of the parent gratings used in the interferometer, regardless of the optical path or the wavelength and coherence of the source. Thus, gratings and grids produced with this tool are extremely repeatable. Figure 31 shows a 100 nm-period grid of 13 nm-diameter posts etched into Si, produced using Achromatic Interferometric Lithography (AIL) and a sequence of etching steps. Other applications AIL include patterned magnetic media, gratings for atom-beam interferometry UV polarizers, and templated self-assembly.

A new generation of achromatic interference lithography tools is currently being developed to produce 50 nm period gratings and grids, or 25 nm lines and spaces. Because of the limited availability of sub-100nm wavelength sources, all of the possible implementations for making 50 nm period gratings are based around the achromatic scheme described for 100 nm period gratings. Among the possibilities are free-standing gratings etched in a thin membrane for use with soft X-rays, or use of reflection gratings in an analogous AIL scheme with a 58.4 nm helium discharge.

The fourth type of interference lithography is Scanning-Beam Interference Lithography (SBIL). Such a system, which is also called the Nanoruler, has been constructed in the Space Nanotechnology Laboratory, and is described in another section.

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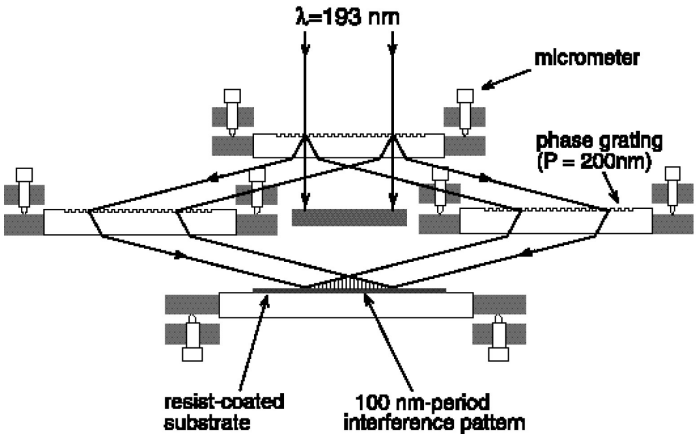
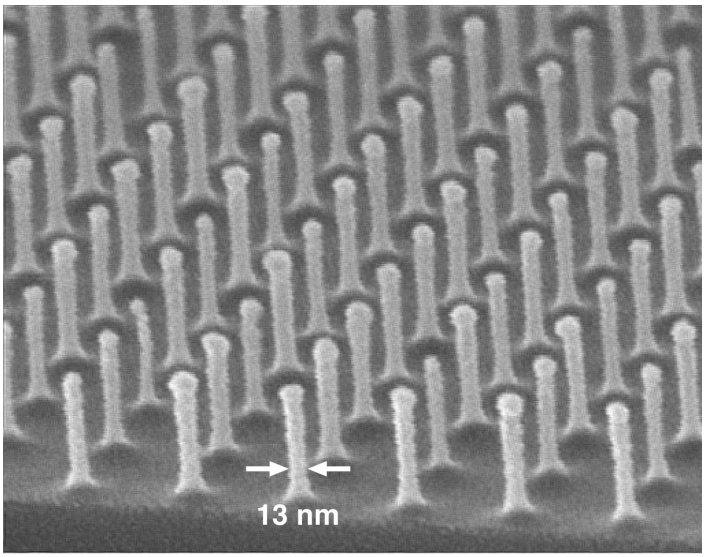


Fig. 30: Achromatic interferometric lithography (AIL) configuration employed to produce 100 nm-period gratings and grids.



100nm-period posts in Si

Fig. 31: Scanning electron micrograph of a 100 nm-period grid, exposed in PMMA on top of an antireflection coating, and transferred into Si by reactive ion etching.

The MIT Nanoruler:
A Tool for Patterning Nano-Accurate Gratings

Personnel
C. Chen, C.-H. Chang, C. Joo, P. Konkola, J. Montoya, and Dr. R. Heilmann
(M. L. Schattenburg and H.I. Smith)

Sponsorship
DARPA, Army Research Office, and NASA

Historically, the ability to observe and measure the results of processes has been critical to advancing fabrication technology. Thus, improvements in optical microscopy (e.g., Nomarski differential interference contrast) were a key enabler of the microelectronics revolution. In turn, the scanning-electron and atomic-force microscopes are essential tools as we move into the nanotechnology era. While the ability to print or resolve a particular feature size is a necessary condition for the successful lithographic manufacturing of nanosystems, it is, by no means, the only requirement. Equally important is the ability to measure and control the size and placement of lithographic features with very high accuracy

All modern lithographic production and inspection tools, and all precision tools for that matter, are based on the notion of a metrology frame. Such a frame is composed of three components: (1) a rigid mechanical structure, (2) means to measure the motion of a workpiece with respect to the metrology frame, and (3) means to project, image or detect patterns on the workpiece, such as by use of an optical or electron lens. The preferred means for measuring workpiece motion has been the laser interferometer. The accuracy of a lithographic tool is critically dependant on the accuracy of its metrology frame, which, in turn, is dependant on the accuracy of the interferometer. Due to a number of complex factors, however, interferometer accuracy is not keeping pace with the shrinking tolerances as called for by the semiconductor industry roadmap (See Figure 32) and the future nanotechnology revolution.

To address this problem, we are developing a lithographic tool called the Nanoruler that is designed to pattern gratings of such high accuracy that they may serve as the means for detecting workpiece motion in precision tools, using a method known as optical encoding, with an accuracy that is some 10-100X better than laser interferometers. The Nanoruler utilizes a patterning method called Scanning-Beam-Interference Lithography (SBIL), developed in the Space Nanotechnology Laboratory (SNL), that is capable of rapidly patterning large gratings (>300 mm diameter) in only a few minutes with unprecedented accuracy (see Figure 33). Such super-accurate gratings can serve as optical encoder plates, as mentioned. Another important application for the Nanoruler is the patterning of nano-accurate gratings necessary for locking an electron beam using a novel technique called Spatial-Phase Locked Electron Beam Lithography (SPLEBL) that is under development in the NanoStructures Laboratory (NSL) and described elsewhere.

High fidelity gratings are also critical for advanced instrumentation and optics such as laboratory and astronomical spectrographs, high-bandwidth optical communications and fusion energy research. Conventional means of fabricating gratings, such as diamond ruling, holography, or beam writing, can take many hours or weeks to complete, and typically produce gratings of poor spatial-phase fidelity.

The concept of SBIL is to combine the sub-1 nm displacement-measuring capability of laser interferometry to control a high-performance air-bearing stage, with the interference of narrow coherent beams, to produce coherent, large-area, linear gratings and grids. Our ultimate goal is to produce gratings with sub-nm distortion over areas many tens of centimeters in diameter. SBIL requires sophisticated environmental controls to mitigate the effects of disturbances such as acoustics, vibration, and air turbulence, and variations of temperature, pressure, and humidity. The system also features real-time measurement and control of optical phase using heterodyne fringe detection, acousto-optic modulator phase locking (See Figure 34), and a high-speed Digital Signal Processor (DSP) controller (See Figure 35).

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An important feature of SBIL is the ability to both write and read gratings with nanometer control of grating phase. Figure 36 is a map of phase error for a grating that was first written in the Nanoruler, developed, and then placed back into the tool and read. The data demonstrates ~2 nm 3s repeatability of the writing/reading process, which includes errors due to substrate chucking/unchucking.

YEAR	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
CD (nm)	130	115	100	90	80	70	65	45	32	22
OVERLAY (nm, mean+3 sigma)	45	40	35	32	28	25	23	18	13	9
MASK IMAGE PLACEMENT (nm)	27	24	21	19	17	15	14	11	8	6
	Solutions Exist			Solutions Being Pursued			No Known Solutions			
METROLOGY FRAME ERROR (nm)	11	10	8.8	8.0	7.0	6.3	5.8	4.5	3.3	2.3
LENGTH SCALE ERROR (nm)	2.8	2.5	2.2	2.0	1.8	1.6	1.4	1.1	0.8	0.6
	MIT Effort									

Fig. 32: Semiconductor Industry Association (SIA) roadmap tracking Critical Dimension (CD) or minimum feature size, overlay error, mask image placement error, and metrology tool error. The MIT effort seeks to produce grating metrology standards with sub-nm errors, which would be used as planar metrology length scales or optical encoders in lithographic and other equipment, eliminating the laser interferometer.

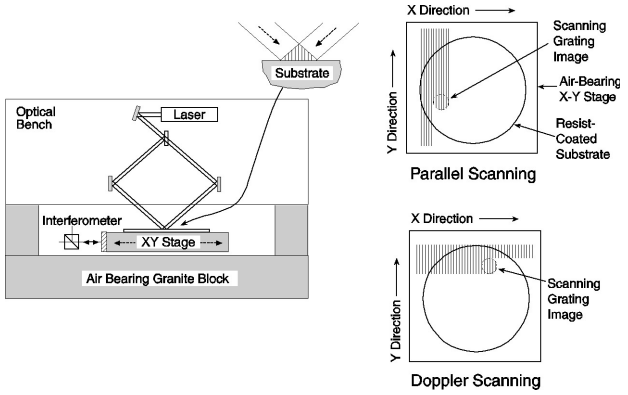

Fig. 33: Schematic of the Scanning-Beam-Interference-Lithography (SBIL) system under development in the SNL. A pair of narrow, low-distortion beams overlap and interfere at the substrate, producing a small grating "image." The substrate is moved under the beams, writing a large area grating. Tightly overlapped scans ensure a uniform dose.

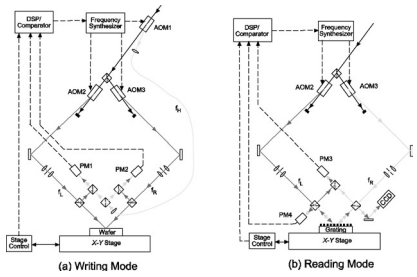

Fig. 34: Schematic of SBIL Acousto-Optic (AO) modulator phase locking system. Both writing and reading modes are depicted. The phase of the grating image is measured by a small interferometer close to the writing surface. The AO modulators Doppler shift the beams into the megaHertz range, providing high-accuracy heterodyne measurement of phase. This information is processed by a digital signal processor and used to control RF frequency synthesizers which drive the AO modulators, thus locking the image phase to the moving substrate.

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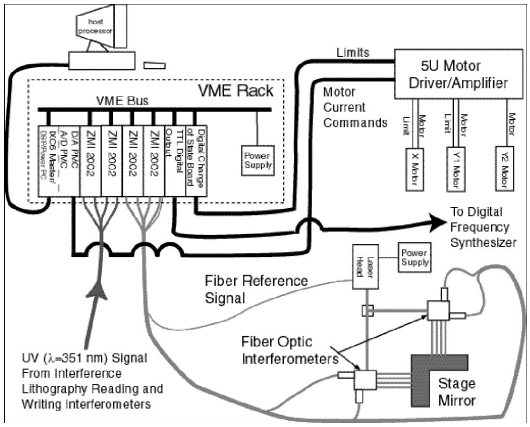

Fig. 35: Schematic of SBIL system control architecture. The system utilizes a frequency stabilized HeNe laser (l=632.8 nm) and heterodyne interferometry to measure substrate position, and argon ion laser (l=351.1) heterodyne interferometery to measure image fringe phase. Phase error signals are processed by an IXTHOS 4x167 MHz DSP board which then drives the stage DC motors and the RF digital frequency synthesizer controlling the fringe-locking AO modulators.

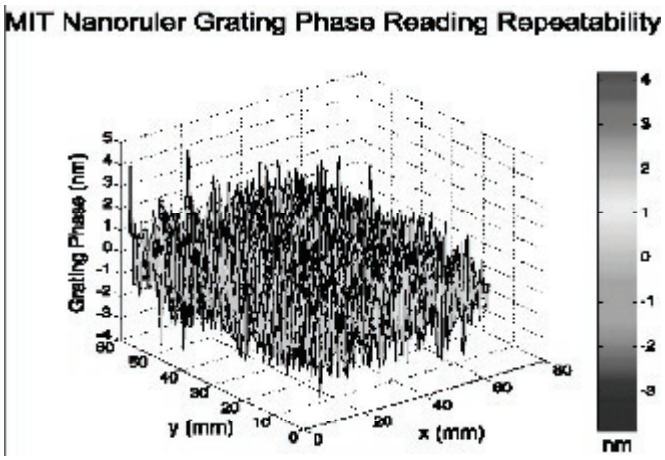

Fig. 36: Wafer phase mapping repeatability (nm), for a 400 nm-period grating that was written and then read by the Nanoruler.

Templated Self-Assembly

Personnel

K. Nielsch, M. Walsh, and A. L. Giermann (C. A. Ross, H. I. Smith, C. V. Thompson in collaboration with F. Ross, IBM, and F. Frankel, MIT)

Sponsorship

NSF

Self-organizing systems can be used to create fine-scale periodic patterns with good short-range order. However, the long-range order of such patterns is typically poor, limiting their usefulness in nanoscale structures or devices. In this new project, methods are being developed to induce long-range order in self-assembled systems patterning the substrate with a lithographically defined periodic structure. This approach is called 'templated self-assembly'. Patterning is carried out by topographically or chemically modulating a substrate, using interference lithography which can pattern large areas of a substrate with periodic features of ~100 nm dimension. The periodically-modulated substrate then provides long-range order to the self-organized system. The overall goal of the project is to develop methods by which nanoscale patterns can be created using a combination of 'conventional' lithography and self-assembly. Of particular interest is how the quality of the assembly is affected by the relative length-scales of the template and the natural period of the self-assembled system.

This approach is being applied to several different physical systems in order to understand how different types of substrate modulation can be used to create nanostructures with long-range order. Examples include the phase-separation of block copolymers (see under 'Block Copolymer Lithography'), the formation of pores in alumina during anodization, the growth of strained SiGe quantum dots on Si substrates by chemical vapor deposition, and the agglomeration ('dewetting') of metal films on oxide surfaces. An example is shown in Figure 37 which illustrates how the pores in anodized alumina, which typically form with a hexagonally-close-packed arrangement, can be formed instead in a square array. This is achieved by depositing an aluminum film over a substrate that has been patterned with a square array of pyramidal indentations, created by interference lithography and anisotropic etching.

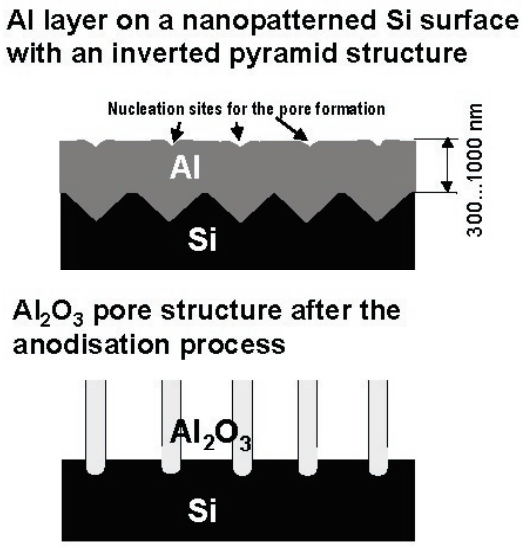

Fig. 37: To make a film of anodized alumina containing a regular arrangement of pores, we start by patterning a silicon substrate with a square array of inverted pyramids, using interference lithography. The substrate is then coated with Al, which conforms to the surface topography. The aluminum film is then anodized (at 80V in this case), and the indentations in the aluminum act as nucleation sites for pores. A film of porous alumina grows containing a square array of pores.

Block Copolymer Lithography

Personnel

J. Cheng and G. J. Vancso (C. A. Ross, H. I. Smith, and E. L. Thomas)

Sponsorship

NSF through the MIT Center for Materials Science and Engineering

Fabrication of large-area periodic nanoscale structures using self-organizing systems is of great interest because of the simplicity and low cost of the process. Block copolymers consist of polymer chains made from two chemically distinct polymer materials. These can self-assemble to form small-scale domains whose size and geometry depend on the molecular weights of the two types of polymer and their interaction. The domains have a very uniform distribution of sizes and shapes. We have been using block copolymers as templates for the formation of structures such as magnetic particles by selectively removing one type of domain and using the resulting template to pattern a nanostructured magnetic film. An example is shown in Figure 38, where Co dots have been made using ion milling to pattern a Co film. The structure has a center-to-center spacing of 50 nm.

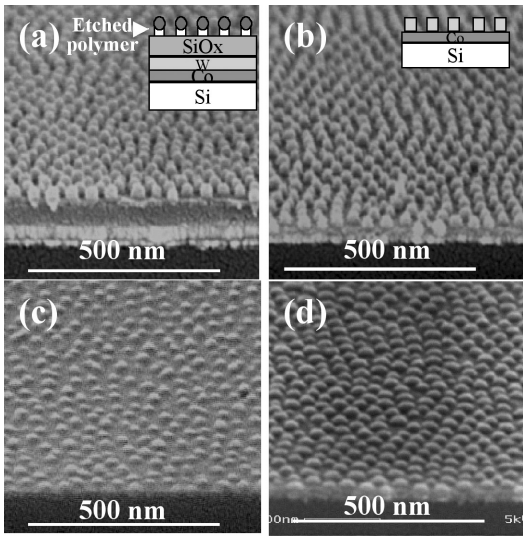

Fig. 38: Cross-section SEM micrographs of (a) Block copolymer lithographic template on the multilayer film. (b) W hard mask (dots) on continuous Co film. (c) Co dots after Ar ion milling. (d) Co dots after Ne ion milling.

However, the self-assembled block copolymer lacks long-range order (See Figure 39(a)). Graphoepitaxy is used here to induce orientation and positional ordering of the block copolymer through an artificial surface patterning. Block copolymers have been spin-cast on silica grating substrates made by interference lithography. For block copolymer PS/PFS 50/12, well-ordered structures form in the grooves of the gratings with all the close-packed rows aligned within the grooves (See Figure 39(b)), provided the groove width is comparable to the 'grain size' of the block copolymers. We have found that the number of rows within the groove, the spacing of the rows, and the deliberate introduction of defects such as vacancies and dislocations can be controlled by adjusting the groove dimensions. These ordered nanostructures may be useful as templates for various applications.

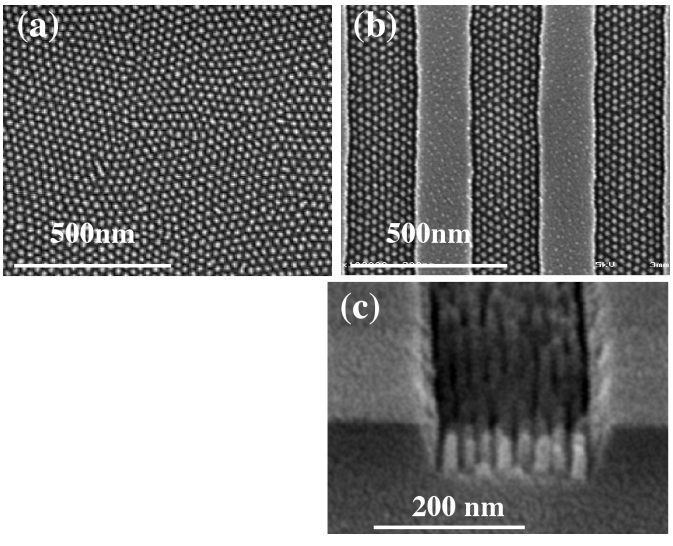

Fig. 39: (a) PS/PFS block copolymer 50/12 on the flat silica substrate. (b) PS/PFS 50/12 forms an ordered structure in 260nm wide silica grooves fabricated by interference lithography. (c) Ordered array of silica pillars, formed by etching using the ordered block copolymer as a template.

Precision Fabrication Techniques for Microphotonic Devices

Personnel

T. Barwicz, J.T. Hastings, J. Huang, M.J. Khan, and M.H. Lim (H. Haus and H.I. Smith)

Sponsorship

DARPA and U.S. Army Research Office and Pirelli Lab S.p.A.

Microphotonic devices seek to miniaturize and integrate the components needed for optical networking. These devices have exacting fabrication tolerances for feature size, pattern-placement, and surface roughness. Careful control of feature size is critical for resonant structures and phase-matching between coupled waveguides, while pattern-placement is essential for devices that rely on long-range interference effects. Surface roughness often dominates optical loss in a device. As a result, only careful control of the fabrication process can maximize device performance. This project focuses on Bragg-grating-based devices and high- index-contrast devices; both of which require precision fabrication.

Grating-Based Devices

Bragg-gratings have widespread application in the field of optical telecommunications. A Bragg-grating is formed by creating a periodic corrugation or refractive index modulation in an optical waveguide. Such a structure behaves as a wavelength-selective filter, reflecting a narrow band of wavelengths while transmitting all other wavelengths. Although Bragg-gratings are commonly imprinted in photosensitive optical fiber, physically-patterned gratings in planar waveguides, shown in Figure 40, offer a number of advantages. For example, one can build Bragg-gratings in non-photosensitive materials such as indium phosphide or silicon. In addition, integrated gratings can contain precise phase-shifts and variations in grating strength to achieve a desired filter response. Finally, the planar-fabrication process can integrate multiple gratings with splitters, couplers, and other optoelectronic components on a single, readily manufacturable chip.

We use a combination of several different types of lithography to generate Bragg-grating devices. In interference lithography, two coherent laser beams are crossed, generating a standing-wave interference pattern. This standing-wave pattern is used to expose photoresist, yielding a coherent submicron-period grating. This grating can be used directly as the device grating or it can serve as a precision reference for later electron-beam lithography steps.

For devices that require long Bragg-gratings with engineered phase shifts or variations in grating strength, we use a technique called Spatially-Phase-Locked E-Beam Lithography (SPLEBL), which combines the long-range spatial coherence of interference lithography with the flexibility of scanning e-beam lithography. Inherent pattern-placement errors in gratings written by standard e-beam lithography limit device performance. SPLEBL references the interference-generated grating during the e-beam exposure to minimize these placement errors.

In many cases, the techniques mentioned above are not applied directly to a device, but instead to an X-ray lithography mask. Once the mask is generated, with the appropriate gratings and alignment marks, the patterns can be repeatedly transferred to substrates using X-ray lithography.

One of the critical challenges facing integrated Bragg-gratings is that they often require submicron grating structures patterned over relatively tall optical waveguides. In order to address this topography problem, we have developed a dual-hardmask process, depicted in Figure 44. This process allows both lithography steps to be performed over essentially planar surfaces. Figure 43 shows devices fabricated by the dual-hardmask process in the indium-phosphide and silicon-on-insulator materials systems.

In many cases it is desirable to place Bragg gratings in the sidewalls of optical waveguides as shown in Figure 43 (b). This technique allows the grating and waveguide to be patterned in the same lithographic step. As a result, the grating depth can be easily varied along the waveguide to introduce apodization. Apodization, the process of gradually increasing and

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then decreasing the grating strength, reduces side-lobe levels in the reflection and transmission spectra of the device, thus reducing cross-talk between neighboring channels in wavelength-division multiplexing. Figure 43 (a) shows an apodized-sidewall grating in a SOI ridge waveguide along with measured transmission spectra. The waveguide-grating structures were patterned using Spatial-Phase-Locked E-Beam Lithography (SPLEBL) and chlorine reactive ion etching. The silicon-on-insulator substrates were provided by Canon.

High Index-Contrast Devices

High-refractive-index-contrast-material systems enable very small bending radii in microphotonic devices. In low-index-contrast waveguides (such as optical fibers), the bending radii must be on the order of centimeters. On the other hand, integrated-optical waveguides exploiting the high index contrast between Silicon Nitride and Silicon Oxide may have bending radii on the order of 10um. This is 1000 times smaller. Consequently, device size shrinks considerably, and large-scale integrated optical circuits become possible. Unfortunately, fabrication of high-index-contrast microphotonic devices is much more demanding than fabrication of low-index-contrast ones. The main challenges reside in precisely and accurately controlling dimensions of submicron features as well as in achieving the required smoothness of waveguide sidewalls. High-index-contrast microphotonic devices are much more sensitive to feature size variations. Moreover, scattering losses due to sidewall roughness become increasingly important when index contrast goes up and may even render devices unusable. In the NanoStructures Laboratory, dimensional control is addressed by using direct-write scanning-electron-beam lithography. The higher resolution allows for much better control of submicron features than photolithography. Sidewall roughness is addressed by optimizing reactive-ion etching for minimal mask erosion (See Figure 44). Additionally, quantitative sidewall roughness measurement techniques are developed for efficient optimization and monitoring of fabrication processes.

An add-drop filter based on optical racetrack resonators is shown on Figure 46. Light is evanescently coupled from a bus waveguide to an adjacent racetrack. If the optical path in a racetrack is equal to an integer number of wavelengths, one will have resonance. In this case, power will be entirely transferred from one bus waveguide to the racetracks and then to the other bus waveguide. The resonance has a Lorentzian profile for a single racetrack and becomes sharper if multiple racetracks are used. The whole device occupies about 20 by 50 μm while low-index-contrast add-drop filters require millimeters or even centimeters.

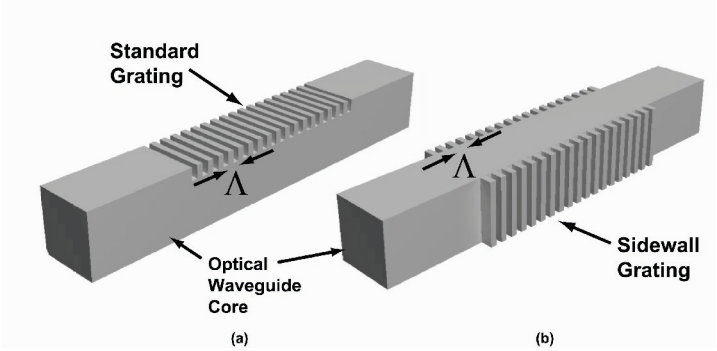

Fig. 40: Two possible configurations for physically patterned Bragg gratings in optical waveguides. (a) Bragg grating patterned in the top of the high-index core. (b) Bragg grating patterned in the sides

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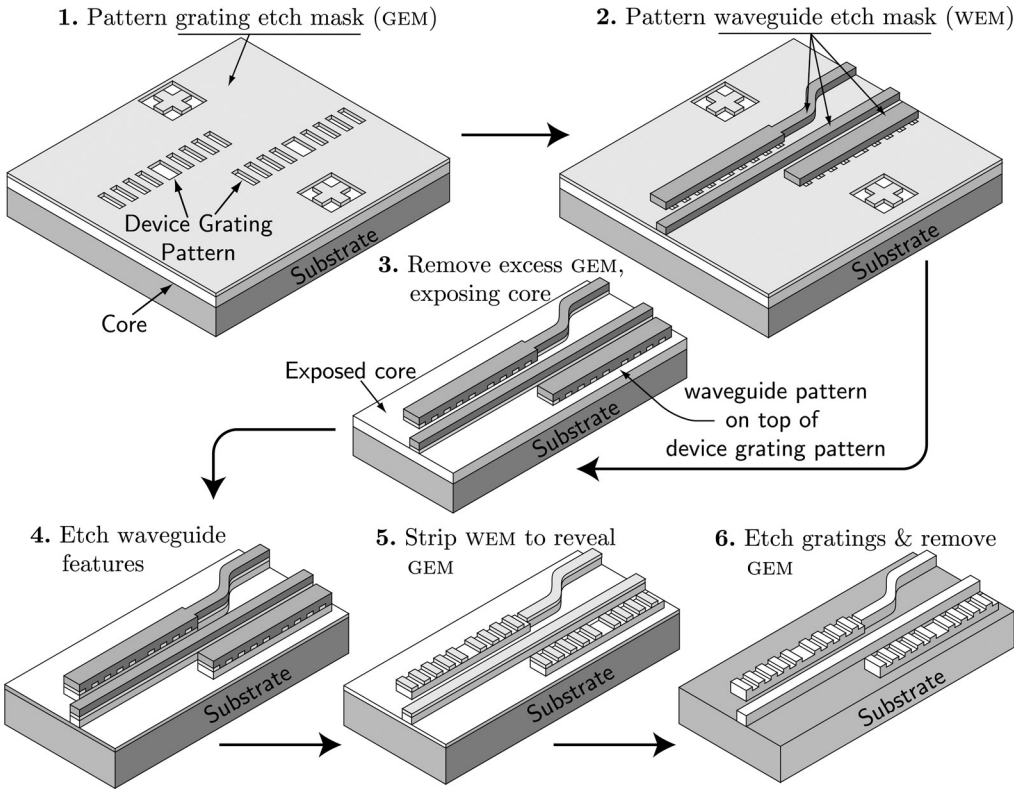

of the high-index core.

Fig. 41: Dual-hardmask process used to pattern fine-period Bragg gratings atop relatively tall waveguide structures. The process is designed such that all lithography steps are performed over essentially planar topography.

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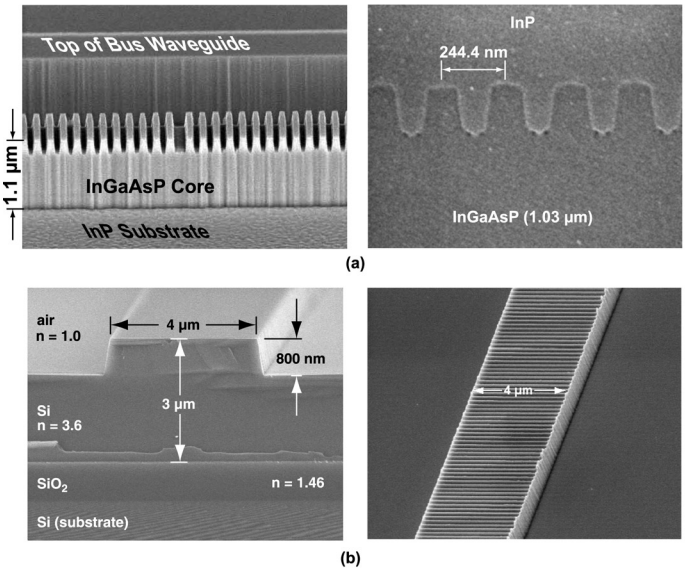

Fig. 42: Examples of the dual-hardmask process applied to two different materials systems. (a) Scanning-electron micrograph depicting a quarter-wave-shifted, 244.4 nm period Bragg grating etched into the top surface of an InGaAsP waveguide, and the subsequent InP overgrowth. (b) Silicon-on-insulator (SOI) ridge waveguide cross-section and SOI waveguide with Bragg grating in the top.

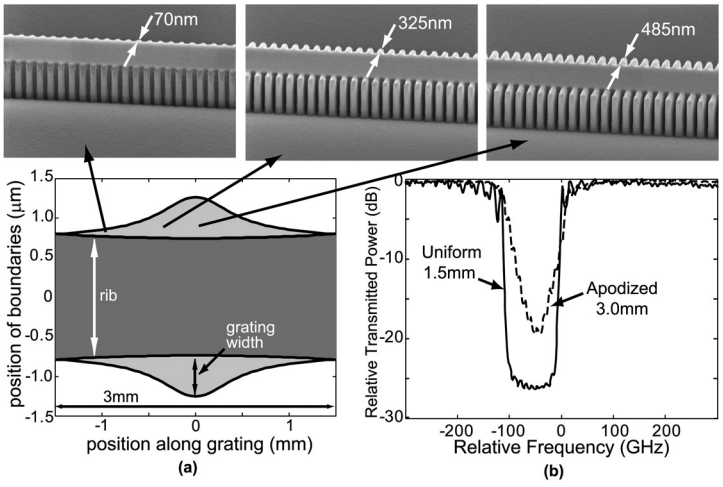

Fig. 43: (a) Apodized Bragg gratings fabricated in the side-walls of a SOI ridge waveguide. (b) Transmission specta for the TE- mode of uniform and apodized waveguide-grating devices. The reduction of side-lobe levels for the apodized devices is readily apparent.

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Fig. 44: Cross-section of a high-index-contrast waveguide with smooth sidewalls. Light is guided by the 330nm thick Silicon-rich Silicon Nitride (SiN) layer with an index of refraction of 2.20. The Silicon Oxide layer is about 3 microns thick and acts as optical isolation from the Silicon wafer.

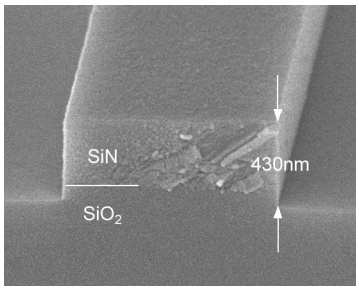
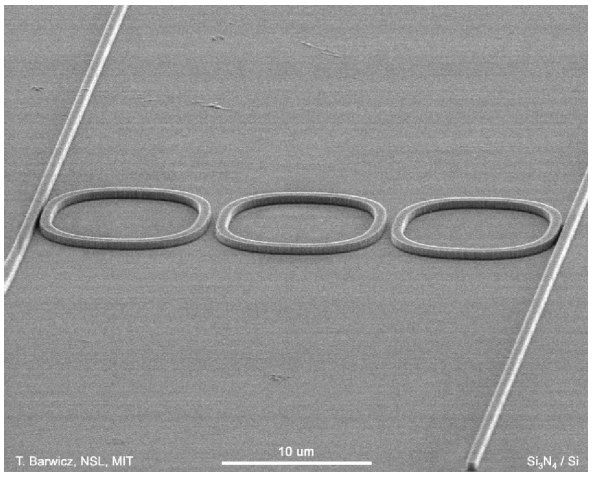


Fig. 45: Add-drop filter based on optical racetrack resonators. This structure was fabricated using scanning-electron-beam lithography. For high-volume manufacturing, a high-resolution replication technique such as X-ray lithography could be used.



Nanopattern-Assisted Growth of Organic Materials for Device Applications

Personnel

D. Mascaro and J. Zartman (V. Bulovic)

Sponsorship

MARCO Focused Research Center on Materials, Structures, and Devices (MARCO/DARPA)

While optoelectronic devices based on organic small molecules have recently become commercially available, electronic devices such as field-effect transistors are less well developed. Typical Organic Field-Effect Transistors (OFET) utilize polycrystalline thin films of evaporated organic materials such as pentacene as the semiconducting layer. The charge carrier mobility, and hence performance, in pentacene OFETs is primarily determined by the molecular ordering within the thin film, where the best OFET (with highest mobility) are made from single crystals of organic materials. As previous research shows that growing large single crystals of molecular organic materials directly on a substrate is a difficult task, we developed a new approach to the formation of such crystals.

Our work to date has focused on tris-(8-hydroxyquinoline) aluminum (Alq_3), which is commonly used as the emitting layer in organic LEDs. The crystal structures of the Alq_3 α-phase and β-phase [from Brinkmann, et al., J. Am. Chem. Soc., 122, 5147 (2000)] is shown in Figure 46. The widespread use of Alq_3 in OLEDs—including products on the market—results from the amorphous nature of as-deposited films and the high glass transition temperature (T_g=175 °C) of Alq_3. These properties yield efficient and durable devices, yet several studies suggest that device failure can result from crystallization of the Alq_3 film during device operation. Indeed, it has been demonstrated that needle-like crystals form when Alq_3 thin films are thermally annealed at temperatures above T_g. The formation of crystals upon exposure to organic solvent vapors has also been observed. This is likely due to the reduction of T_g by the permeation of solvent molecules into the film, which is a well-known effect—that of plasticization—in the field of polymers.

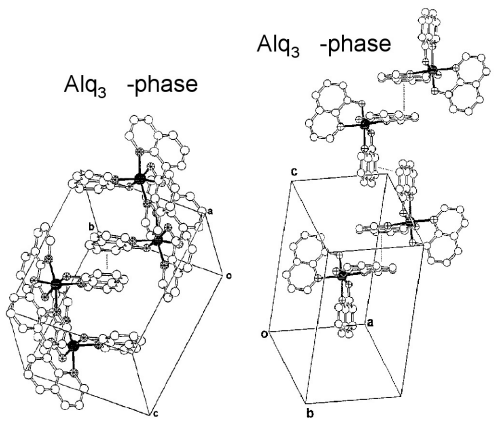


Fig. 46: α and β crystal forms of Alq3. (from Brinkmann, et al., J. Am. Chem. Soc., 122, 5147 (2000).

The crystallization of Alq_3 thin films is detrimental to OLED performance, but it suggests that generating large thin single crystals of organic materials in the plane of the substrate could be possible. A technique that could form such crystals and also direct them along pre-determined substrate directions would be especially useful for OFET use and also for forming single crystals of organic non-linear materials for optoelectronic applications.

We recently demonstrated that nano-patterned substrates can, indeed, be used to direct the flow of solvent-rich thin films of Alq_3 and thereby, generate such oriented needle crystals in the plane of the substrate. The optical micrograph in Figure 47 shows a portion of a nano-patterned substrate with Alq_3 crystals that are predominantly aligned with the underlying nano-grooves.

To generate the crystal needles, Alq_3 is deposited onto nano-patterned Si or SiO_2 substrates by thermal evaporation in vacuum (<10^{-6} Torr). The Alq_3 films are typically 10-20 nm thick and are deposited at rates of 1-3 Å/s (as measured by a quartz crystal thickness monitor) onto room temperature substrates. Prior to Alq_3 deposition, the nano-patterned substrates are cleaned via a sequence of steps involving either sonication in

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a solution/solvent or immersion in a boiling solvent. Following the final boiling 2-propanol step, the substrates are dried in a stream of nitrogen and further cleaned by UV-ozone treatment for 5 to 30 minutes. In the case of chemical surface modification, the substrates are placed in a vessel together with a crucible containing n-octadecyltrichlorosilane (OTS). The vessel is evacuated to a pressure of <1 Torr and heated to 120 °C for ~2 hours. Substrates treated in this manner are hydrophobic. Following the evaporation of Alq_3, the substrates are placed in a glass jar together with a beaker of chloroform, and the jar is sealed with a Teflon-lined cap. Exposure of the Alq_3 films to chloroform vapor for times ranging from a few hours to two days results in the formation of elongated Alq_3 crystals that are oriented parallel to the underlying nano-grating. The crystals are characterized by a variety of techniques, including optical microscopy, fluorescence microscopy, Atomic Force Microscopy (AFM), and Scanning Electron Microscopy (SEM).

The nano-patterned substrates are fabricated via interference lithography in the NanoStructures Laboratory (NSL) at MIT. Interference lithography is a maskless lithography in which photoresist is exposed by the optical standing wave generated by the interference of two coherent beams of light. Using the Lloyd's Mirror setup in the NSL, we can generate periodic patterns over square centimeters with feature sizes ranging from 100 to 500 nm. The patterns are transferred to Si or SiO_2 via etching, resulting in surface relief gratings with depths up to 150 nm. After etching, the wafers are cleaned in 5:1:1 H_2O:H_2O_2:NH_4OH at 80 °C for ~10 minutes to remove any remaining anti-reflection coating, SiO_x interlayer, or photoresist. After the wafers are diced into ~cm^2 pieces, these pieces are further cleaned and processed as described above. Figure 48 summarizes all of the fabrication steps, beginning with the nano-lithography, necessary to form oriented crystals of Alq_3. The final step depicted is the evaporation of metal electrodes to enable electrical characterization.

The Alq_3 crystal needles formed in this process vary in size from experiment to experiment, with thicknesses and widths ranging from hundreds of nanometers to a few microns and lengths ranging from a few hundred microns up to one centimeter (the size of the substrate). The needle length can exceed the needle thicknesss and needle width by a factor of 1000 or more. Needle thicknesses exceed the initial Alq_3 amorphous film thickness (typically 10-20 nm) by as much as 200 times. The total volume of a 10 nm thick film on a centimeter square substrate is 10^{-12} m^3. A needle with dimensions 1 μm by 1 μm by 1 cm has a volume of 10^{-14} m^3. Hence, 100 such needles could be formed from the initial thin film, and these needles would be separated by approximately 100 microns. Such a perfect sample has never been produced, but the sizes of the needles formed are consistent with this simple volume analysis. With respect to the nano-pattern dimensions, the needles can be as narrow as one nano-groove or as wide as tens of grooves, and the needle thickness can exceed the groove depth by a factor of 50 or more.

Preliminary electron diffraction data indicates that the needles are single crystals. Other characterization of the needles supports this as well. Figure 49 shows two SEM micrographs of different Alq_3 needles. Micrograph A is a top view of one end of a several micron wide needle, and micrograph B shows the cross section of a smaller needle (the substrate was cleaved in the middle of the needle). Both micrographs show that the needles have distinct crystal facets and tend to be diamond-shaped in cross section. In addition, the fluorescence of the Alq_3 needles is polarized, which is expected if the Alq_3 is crystalline. The graph in Figure 50 plots normalized photoluminescence intensity as a function of polarizer angle, while the fluorescence micrographs shown below the plot correspond to the brightest and dimmest data

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points. The discrepancy between the 0° and 180° data points is a result of photobleaching of the needle during the course of the measurements.

The formation of the Alq_3 crystals, such as that in Figure 51, is traced to the exposure of the evaporated thin films to the chloroform vapor. We observe that formed Alq_3 crystals are surrounded by what appear to be amorphous and flowing organic films. The flowing segments are confined by the substrate grooves and are characterized by menisci at both ends in the plane of the substrate and also in cross section. Several of these segments can be seen in the middle of the SEM micrograph of Figure 51 and also surrounding the AFM image inset in the same figure. The menisci of the amorphous segments lend evidence towards a fluid-like state of the Alq_3 thin film in the presence of chloroform. This fluidity can be understood in terms of a plasticization effect, whereby the T_g of a glassy material (typically a polymer) is reduced by the presence of low molecular weight additives. The effect of plasticization on T_g can be roughly estimated by the following semi-empirical equations:

$$T_g \approx \frac{T_{gp}}{1+(X-1)(1-\Phi_p)} \tag{6}$$

$$X \approx \frac{T_{gp}}{T_{gs}} \tag{7}$$

$$T_{gs} \approx \frac{2}{3} T_{ms} \tag{8}$$

These equations are based on free-volume considerations. T_{gp} and T_{gs} are the glass transition temperatures of the pure polymer and pure solvent, respectively, and T_{ms} is the melting temperature of the solvent. Equation 8 is used to estimate T_{gs} based on T_{ms} because T_{gs} has been measured for only a few solvents. Φ_p is the volume fraction of the polymer. Using T_{gp}=175 °C for Alq_3 and T_{ms}=-63 °C for chloroform in the above equations, the predicted effect of chloroform permeation on the T_g of Alq_3 is plotted in Figure 52. As can be seen from the plot, the T_g of Alq_3 is significantly reduced by the presence of the chloroform, dropping to 40 °C when the film is 20% chloroform and falling below room temperature when the film is 25% chloroform by volume. Hence, it is reasonable to suggest that the Alq_3 is able to incorporate enough chloroform to become fluid at room temperature.

It is curious, however, that the amorphous segments, which are the signature of fluid Alq_3, are only observed adjacent to Alq_3 crystals, suggesting that there is a higher concentration of chloroform in the vicinity of the crystals. This could result from a rapid exclusion of chloroform in liquid form as Alq_3 molecules are incorporated into the growing crystal. Another possible explanation is based on the apparent affinity between chloroform and Alq_3, and assumes that the surface of each crystal is coated with a thin layer of fluid, chloroform-rich Alq_3. The large surface area of the crystal relative to that of the crystallite clusters would, therefore, result in a higher concentration of chloroform near the crystal. Indeed, a correlation exists between the size of the crystal and the width of the surrounding region that has experienced flow of chloroform-rich Alq_3. The crystal in Figure 51 is ~300 nm thick and ~600 nm wide, and nano-films are observed in a strip that extends ~2.5 microns to the right of the crystal (similarly on the other side of the crystal). In comparison, for a smaller needle that is ~130 nm thick and ~400 nm wide, the width of the strip containing nano-films is only one to two grating periods (300-600 nm). Therefore, as a crystal grows, an increasing concentration of chloroform at the crystal surface (due to increasing surface area) causes the surrounding region of flowing Alq_3 to widen. In some cases, extended nano-films (exceeding several microns in length) are present in the grooves immediately adjacent to an Alq_3 crystal. This implies that the crystal was in a very active stage of growth—

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having a plentiful supply of fluid Alq_3 close by—when the vapor treatment was terminated. In fact, the crystals likely grow up out of the Alq_3 that flows in the nano-grooves as evidenced by the nano-films that are protruding out from underneath the crystal tip in the AFM micrograph of Figure 51.

Although the individual amorphous segments and crystallite clusters are too small to be resolved by optical microscopy, the regions of the substrate with clusters can be distinguished from amorphous flow regions in optical micrographs. For example, the darker, speckled region of the substrate on the left in Figure 47 is a region with crystallite clusters. The rest of the substrate surrounding the crystals has experienced flow of chloroform-rich Alq_3.

What is astonishing about the flow regions of Figure 47 is the extent to which they extend beyond the ends of the crystals in the direction parallel to the underlying nano-grooves. This sheds light on the critical role played by the substrate nano-pattern in the formation of the Alq_3 crystals. What has been emphasized up to this point is that the incorporation of enough (~25% by volume) chloroform can cause Alq_3 to become fluid at room temperature, but this seems to happen only near crystals. As was mentioned before, this suggests that there is extra chloroform associated with the crystals, possibly due to a thin fluid layer of chloroform-rich Alq_3 on the crystal surface. It is also likely that chloroform is excluded as Alq_3 molecules are incorporated into a crystal. Since the atmosphere in the vapor treatment jar is already saturated with chloroform vapor, it is reasonable to assume that the excluded chloroform will remain on the substrate as a liquid. The chloroform can then flow on the substrate, but due to capillary effects, it prefers to flow down the nano-grooves of the patterned substrate. As it flows down the grooves, it encounters and permeates Alq_3, reducing its T_g, and allowing it to flow down the grooves as well. It is in this way that the nano-grooves aid the transport of Alq_3 to the forming crystals, and this also explains the elongation of the flow regions parallel to the nano-grooves.

A transport ratio can also be calculated from substrates with much more extensive Alq_3 flow and crystal formation, such as the substrate shown in Figure 47. The distance traveled by Alq_3 perpendicular to the nano-grooves can be ascertained by the gap between the (speckled) crystallite cluster region on the left side of the micrograph and the leftmost crystal. This gap is ~200 microns wide. In contrast, the typical distance parallel to the nano-grooves separating the cross needles from the oriented needles is ~2 mm, indicating that the Alq_3 was able to flow at least 1 mm down the nano-grooves to reach a crystal. The calculated transport ratio in this case is only 1:5, but this is likely a conservative estimate since the flow is so widespread and may even have been limited by the size of the substrate. The large size of the cross crystals can be understood in terms of the large number of nano-grooves intersected by these crystals relative to the number of grooves that directly feed the oriented crystals.

While the proposed mechanism for crystal growth via capillary flow of chloroform-rich Alq_3 down substrate nano-grooves in the vicinity of pre-existing crystals seems well-supported, the question remains as to how the crystals are formed initially. It is possible that crystallites present in the as-deposited films seed the growth, or that crystallite clusters (formed during exposure to chloroform vapor) of a certain size can act as a seed. Whatever the case may be, it seems that the requirement for crystal formation is a large enough concentration of chloroform to initiate significant flow of Alq_3. Although the exact mechanism for the nucleation of the crystals is not fully understood at this time, the ease of formation of crystals of such large dimensions in the plane of a substrate is a technological breakthrough in the field of organic electronics.

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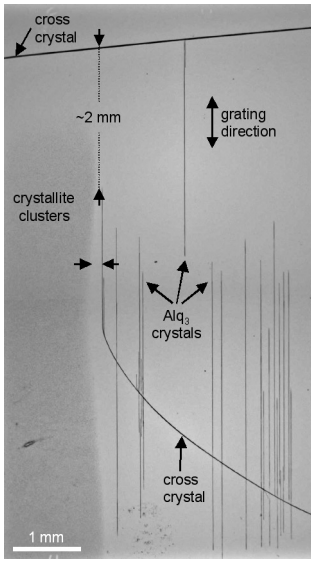

Fig. 47: Macroscopic Alq_3 crystals on a nanopatterned substrate.

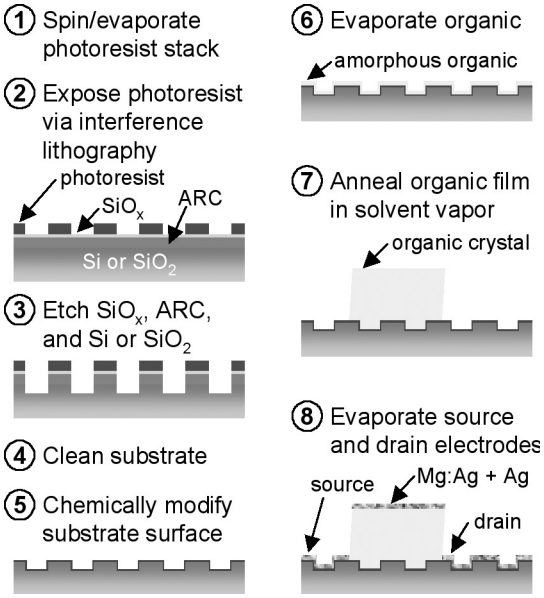

Fig. 48: Fabrication steps, beginning with the nano-lithography, necessary to form oriented crystals of Alq_3.

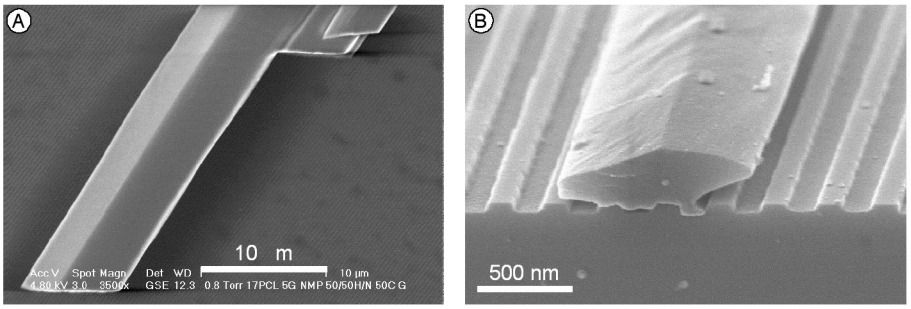

Fig. 49: SEM micrograph of two Alq_3 crystals. (A) is a top view of one end of a several micron wide needle, and (B) shows the cross section of a smaller needle (the substrate was cleaved in the middle of the needle).

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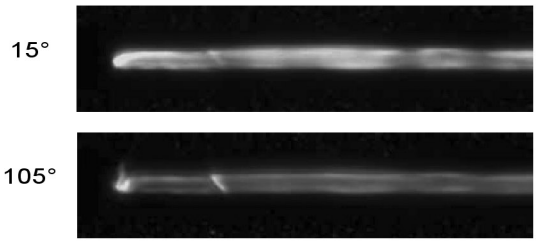


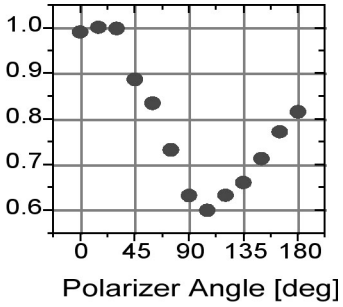
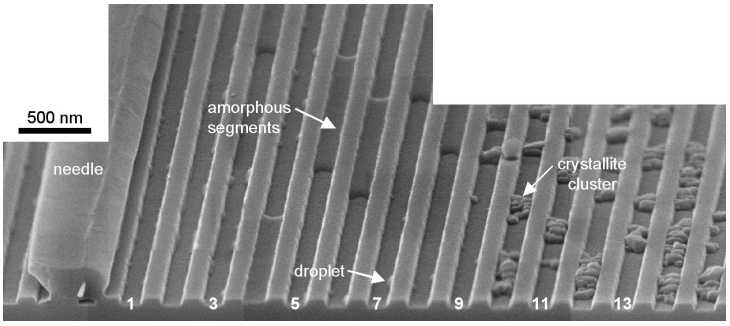
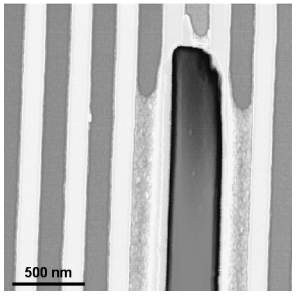


Fig. 50: (left) Polarized fluorescence micrographs (UV excitation at 449 nm) for two orthogonal polarizer angles. (right) The graph plots the normalized photoluminescence intensity as a function of polarizer angle.

Fig. 51: (left) SEM and (right) AFM micrograph of a Alq_3 crystal and vicinity.





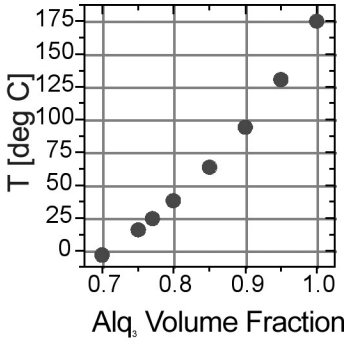


Fig. 52: Change in the glass transition temperature of Alq_3 upon incorporation of chloroform.

Strain-Tunable Photonic Band Gap Microcavity Waveguides at 1.55 μm

Personnel
C. W. Wong, M. Qi, P. Rakich, S. G. Johnson and Y. B. Jeon (G. Barbastathis, S-G. Kim and H. I. Smith)

Sponsorship
MIT Microphotonics Center

We have designed and fabricated tunable photonic-bandgap microcavities in optical waveguides, with strain modulation via thin-film piezoelectric actuators on deformable membranes. Cavity resonance tunability, with nanometer lattice control, is designed through perturbation on Finite-Difference Time-Domain FDTD computations. Device fabrication integrates X-ray nanolithography, piezoelectric micro-actuators and bulk micromachining.

Photonic-bandgap microcavities in optical waveguides have demonstrated cavity resonances at wavelengths near the 1.55 μm band, quality factors on the order of 300, and modal volume at 0.055 μm^3 in high-index contrast Si/SiO_2 waveguides and GaAs air-bridge waveguides. Applications include zero-threshold microlasers, filters, and signal routers. For tunability in Si microphotonic platforms, thermal actuation is often utilized. Compared to thermo-optics, strain-tuning via thin-film piezoelectric micro-actuators provides a significantly faster response, lower power consumption, and better localization of tunability. This level of integration permits dynamic reconfiguration of the cavity resonance and band-edges, fine-tuning for fabrication mismatches, and active compensation of device arrays to external disturbances.

The conceptual design is illustrated in Figure 53. The Si microcavity waveguide is located on a deformable double-anchored SiO_2/Si membrane. The thin-film piezoelectric actuators provide sufficient driving force, under 5 V actuation, for the sub-nanometer strain control of the geometric lattice in the microcavity. Comparative designs of the double-anchored membrane have been demonstrated for analog tunable diffractive gratings. Experimental effects of static strain on coupled vertical microcavity resonators and theoretical designs for shear-modulated 2D photonic crystals on bulk piezoelectric substrates have also been reported.

We employ first-order perturbation theory to obtain a semi-analytical result for the strain-induced shift in the cavity resonance; such methods ease the study of small modulations such as the 0.3% strain considered here. First, a closed-form solution for the hole boundary displacements is derived following classical mechanics. The material boundary displacements are then numerically meshed and employed in a perturbation-theory formulation, which involves surface integrals of the unperturbed fields (obtained by FDTD simulation) over the perturbed material boundaries. The result predicts a 0.8% shift in resonant wavelength (12.7 nm in the C-band) for a 0.3% mechanical strain from a 3D computation. This is illustrated in Figure 54a. While a 2D computation suggests similar final results in the resonant shift, the 3D computation highlights differences from the individual contributions – hole ellipticity, defect cavity length, and hole diameters – in the strain perturbation. Other effects such as photoelasticity and waveguide out-of-plane bending were found to be secondary.

For resonance wavelength at 1.55 μm, the minimum feature size, located between the waveguide edges and the hole edges, is 130 nm. X-ray lithography is employed with a Cu_L source at 1.3 nm to transfer the pattern from the mask to a PMMA resist. The mask is a thin SiN_x membrane with 200 nm Au patterned with e-beam lithography. The resist image is then transferred to 50 nm of Cr, via lift-off, and etched into a 212 nm single-crystal Si layer to form our waveguide. The microfabricated piezoelectric film has an excellent dielectric constant of 1200 and a d_{31} coefficient of ~ -100 pC/N. A fiber lens assembly is used to couple a 1.430 μm to 1.610 μm tunable laser diode source, with TE polarization and lock-in amplification, into the prepared input/output waveguide facets. For a static microcavity waveguide, resonance is detected at 1555.4 nm with a Q of 159, as shown in Figure 54b. Experimental measurements of the tunable cavity resonance, band-edges, and other cavity responses are currently underway.

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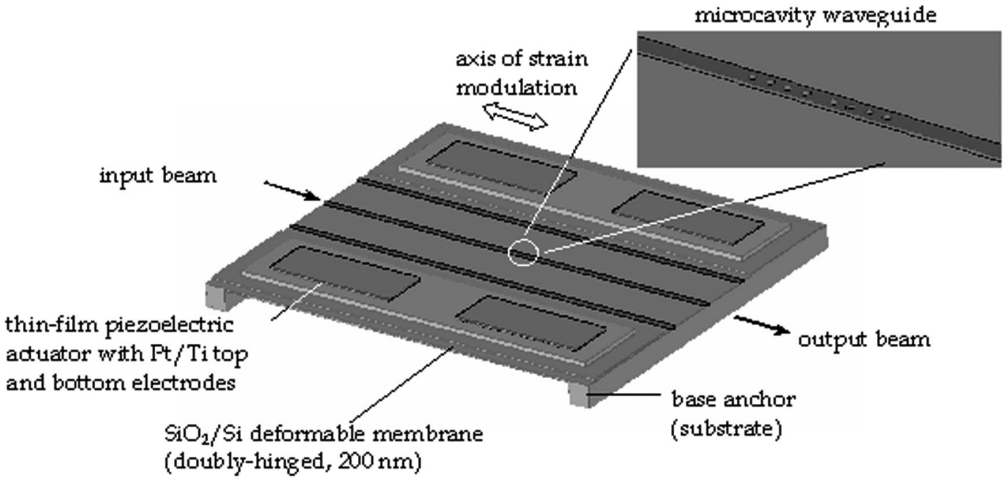

Fig. 53: Device schematic of the tunable photonic-bandgap microcavity waveguide, with strain modulation via thin-film piezoelectric actuators on the deformable membrane.

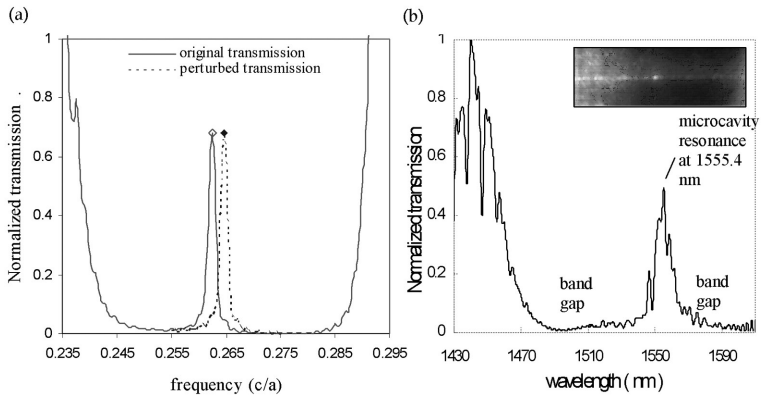

Fig. 54: (a) Computed transmission shift through perturbation theory in the photonic band gap, (b) Measured static microcavity resonance with Q of 159. Inset: top view of microcavity waveguide in transmission.

Nanopelleting of Carbon Nanotubes

Personnel

T. El-Aguizy, Y. Jeon, and J.-H. Jeong (S.-G. Kim)

Sponsorship

Deshpande Center Ignition Grant

A novel method of decoupling the growth and the assembly of Carbon NanoTubes (CNT) has been invented. The objective of this project is to make a long range ordered CNTs on a large area, which has not been possible with the existing nanotube growing processes. Nanopelleting is the technology to transform carbon nanotubes into the handleable and manufacturable form with which the existing micro-scale manufacturing processes can be utilized, such as fluidic self assembly or MEMS manupulators. To achieve this, small blocks (nanopellets) of material encapsulating CNTs with known length and alignment are going to be made (See Figure 55). The CVD growth of individual free-standing nanotubes in arrays of Silicon trenches followed by the encapsulation and CMP will form nanotube-embedded nanopellets. Various self-assembly methods can then be utilized to locate the individual nanopellets at points of use. The nanopelleting material must allow for selective release from the substrate material as well as selective removal of the nanopellet material without affecting the CNTs.

Fabrication of the silicon trenches can be achieved utilizing anisotropic wet etching of (100) wafers to allow for well-defined sloping sidewalls that facilitate self-assembly. The desired geometry and periodicity can be achieved by tailoring the mask pattern and etch parameters to achieve the desired geometry and periodicity in the resulting trenches. Nickel nanodots with diameters of several microns are currently used as the catalyst patches in CNT growth. Interference lithography and X-ray lithography are well suited for patterning periodic patterns in the sub-micron regime, and we investigate their potential for patterning sub-micron (200nm) nanodots aligned with the etched trench patterns.

Several methods exist for growing single or multi-walled CNTs, including arc discharge and CVD methods. Plasma Enhanced (PE) CVD methods provide a reliable, low-cost option for growing well-ordered, aligned CNT over large areas. We have established a collaboration with Z.F. Ren of Boston College to utilize their PE-CVD device for growth of aligned CNTs. Advantages of this approach include: the lower temperatures required for nanotube formation, the flexibility in the range of catalytic materials used, and the inherent e-field that assists in growth of aligned CNTs.

We are investigating various materials for filling the nanopellets to satisfy the functional requirements (See Figure 56). Spin-coated M-Bond epoxy is found to allow selective release of the nanopellets from a silicon substrate utilizing xenon di-fluoride (XeF_2) as well as the selective removal of the M-Bond without attacking the CNT utilizing oxygen plasma etching. We are also investigating the possibility for utilizing conventional chemical-mechanical planarization methods to eliminate any excess filler material, leaving independent nanopellets with well-defined geometry encapsulating aligned CNTs with well-defined lengths and diameters.

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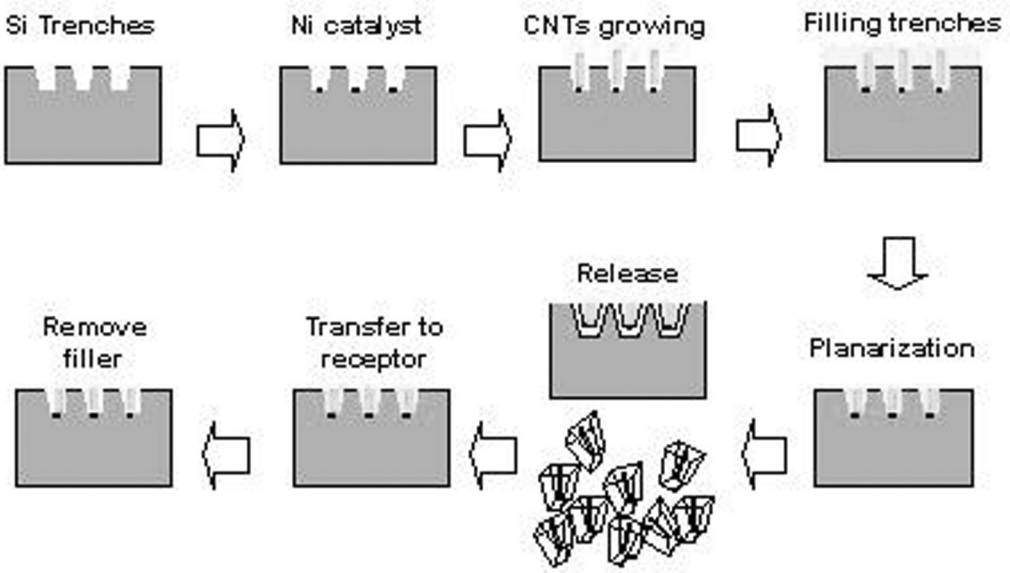

Fig 55: *Nanopelleting of CNTs*

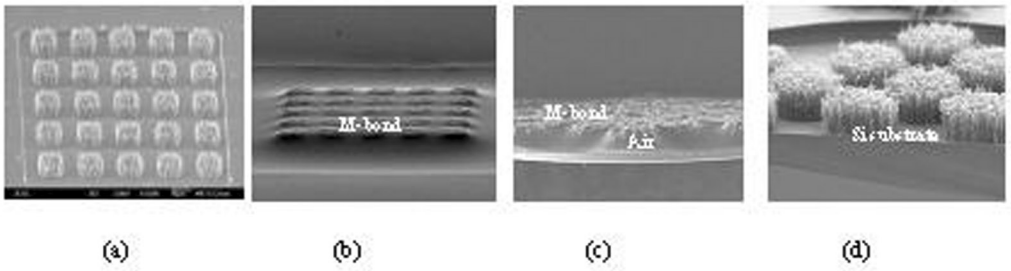

Fig. 56: SEM images of the CNTs (a) Grown CNTs, (b) Filled with M-bond, (c) Released M-bond pellet by XeF_2 (not planarized) and (d) CNTs after filler removal by O_2 plasma (not planarized)

Nanofabricated Reflection Gratings

Personnel

J. Carter, C.-H. Chang, R.C. Fleming, R. Heilmann, and E. Murphy
(M.L. Schattenburg, C.R. Canizares and H.I. Smith)

Sponsorship

NASA and Chromaplex Corp.

Grazing-incidence X-ray reflection gratings are an important component of advanced high-resolution spectrometers and other X-ray optics. These have traditionally been fabricated by diamond scribing with a ruling engine or by interference lithography followed by ion etching. These methods result in gratings which suffer from a number of deficiencies, including high surface roughness and poor groove profile control, leading to poor diffraction efficiency and large amounts of scattered light.

We are developing improved methods for fabricating blazed X-ray reflection gratings which utilize special (111) silicon wafers, cut ~1 degree off the (111) plane. Silicon anisotropic etching solutions, such as potassium hydroxide (KOH), etch the (111) planes very slow compared to other crystallographic directions, resulting in the desired super-smooth blaze surface. Previous work used similar off-cut (111) silicon substrates to fabricate blazed diffraction gratings, but utilized a second KOH etch step that compromised the grating facet flatness and proved unsuitable for small grazing-angle X-ray diffraction.

Gratings are patterned using interference lithography with the l=351.1 nm wavelength, and transferred into the substrate using tri-level resist processing, Reactive-Ion Etching (RIE), and silicon-nitride masking during the KOH etch. The narrow (~100 nm) ridge of silicon which supports the nitride mask is removed using a novel chromium lift-off step followed by a CF_4 RIE. The result is extremely-smooth sawtooth patterns, which, after applying a thin evaporative coating of Cr/Au, are suitable for X-ray reflection (See Figure 57).

We have recently begun a new effort to replicate sawtooth gratings using nano-imprint lithography with a UV-curable polymer (See Figure 58). If successful, this new method promises to significantly reduce the cost of grating fabrication.

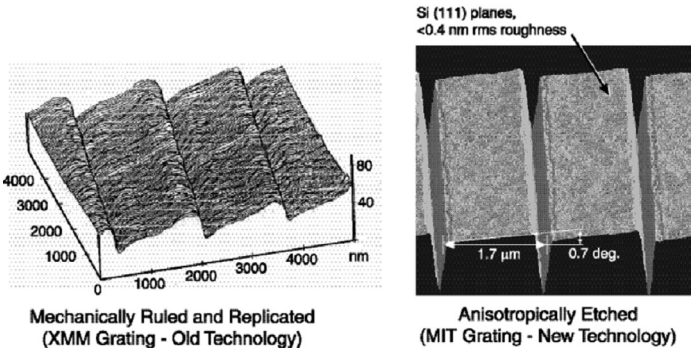

*Fig. 57: (a) An AFM image of a traditional mechanically-ruled and replicated X-ray reflection grating (Bixler et al., Proc. SPIE **1549**, 420-428 [1991]). Note the rough, wavy grating surfaces that lead to poor diffraction performance. (b) An AFM image of a blazed X-ray reflection grating fabricated by anisotropic etching of special off-cut (111) silicon wafers. Note the improvement of grating surface flatness and smoothness, leading to significantly improved performance.*

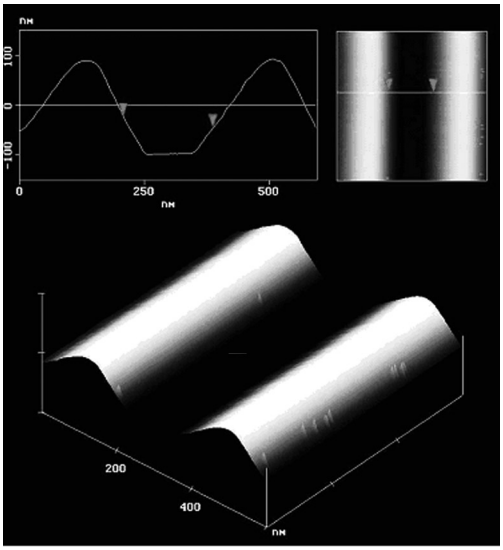

Fig. 58: AFM image of nano-imprinted grating. Profile is far from ideal at this stage.

Transmission Gratings for X-ray and Atom-Beam Spectroscopy and Interferometry

Personnel

J.M. Carter, T.A. Savas, and E. Murphy (H.I. Smith and M.L. Schattenburg)

Sponsorship

X-OPT, Inc.

Transmission gratings with periods of 100 to 1000 nm are widely used in applications such as X-ray, vacuum-ultraviolet, and atom-beam spectroscopy and interferometry. Over 30 laboratories around the world depend on MIT-supplied gratings in their work. For X-ray and VUV spectroscopy, gratings are made of gold and have periods of 100 to 1000 nm, and thicknesses ranging from 100 to 1000 nm. The gratings are most commonly used for spectroscopy of the X-ray emission from high-temperature plasmas. Transmission gratings are supported on thin (1 micron) polyimide membranes, or made self supporting ("free standing") by the addition of crossing struts (mesh). (For short X-ray wavelengths, membrane support is desired, while for the long wavelengths, a mesh support is preferred in order to increase efficiency.) Fabrication is performed by interference lithography combined with reactive-ion etching and electroplating. Progress in this area tends to focus on improving the yield and flexibility of the fabrication procedures.

Another application is the diffraction of neutral-atom and molecular beams by mesh-supported gratings. Lithographic and etching procedures have been developed for fabricationg free-standing gratings and grids in thin silicon nitride (SiNx) membranes supported in a Si frame. Figure 59 shows a free-standing 100 nm-period grating in 100 nm-thick silicon nitride. Figure 60 shows a 100 nm-period grid in a 100 nm-thick SiNx membrane. Such a grid is used in experiments as a "molecular sieve."

We have established a collaboration with the Max-Planck Institute in Göttingen, Germany, in which they utilize our gratings of 100 nm period in diffraction experiments using atomic, molecular, and helium-cluster beams. As shown in Figure 61, the diffraction of atomic and molecular beams reveals striking deviations from Kirchhoff's optical diffraction theory. The analysis of the diffraction intensities enabled a quantitative determination of the attractive van der Waals interaction between the silicon nitride surface and various atomic and molecular species, including He, Ne, Ar, Kr, He*, Ne*, D_2, and CH_3F. The diffraction of cluster beams by a transmission grating has been established as a unique technique for the non-destructive mass selection and detection of small and weakly bound van der Waals clusters. Recently, the Göttingen group discovered bound states in mixed-isotope helium clusters, e.g. $^3He^4He_2$, $^3He^4He_3$, etc., by diffraction from one of our 100-nm-period gratings as shown in Figure 62. In addition, they employed the grating to measure the bond length of the helium dimer, $^4He_2$, which is assumed to be the weakest molecular bond. Future experiments based on the transmission gratings include the study of cluster formation dynamics and the search for the Efimov effect in the helium trimer.

Data obtained by helium-atom-beam diffraction at large incident angles showed Lyman ghosts in the spectrum. This data led to the development of new fabrication techniques to improve the quality of the free-standing gratings in silicon nitride. Diffraction spectra from gratings made with the improved process show no Lyman ghosts, illustrating the important synergy between applications and nanofabrication.

Successful diffraction experiments with beams of buckyballs (C60) have been carried out with our 100 nm-period, free-standing SiNx gratings by Dr. Markus Arndt of the University of Vienna. In addition, our 100 nm-period, free-standing SiNx gratings can be lightly coated with metal. Prof. Herman Batelaan of the University of Nebraska-Lincoln has used such gratings in highly-successful diffraction experiments with beams of 500 eV electrons.

Our 100 nm-period free-standing SiNx gratings are also used for atom interferometry by two groups: those of Prof. Alexander Cronin of the University of Arizona

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and Prof. Bruce Doak of the State University of Arizona. Cronin's group interferes neutral beams of sodium atoms, while Doak's group interferes helium beams (performed at the Max Planck Institute in Göttingen, Germany in collaboration with P. Toennies).

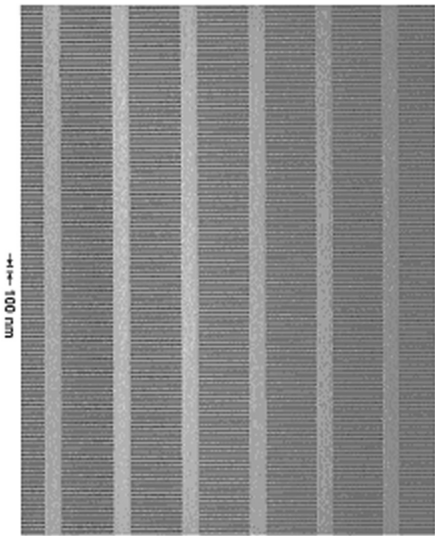

Fig. 59: Scanning electron micrograph of a free-standing 100 nm-period grating (50 nm-wide bars) in a silicon nitride membrane of area 500 microns by 5 mm.

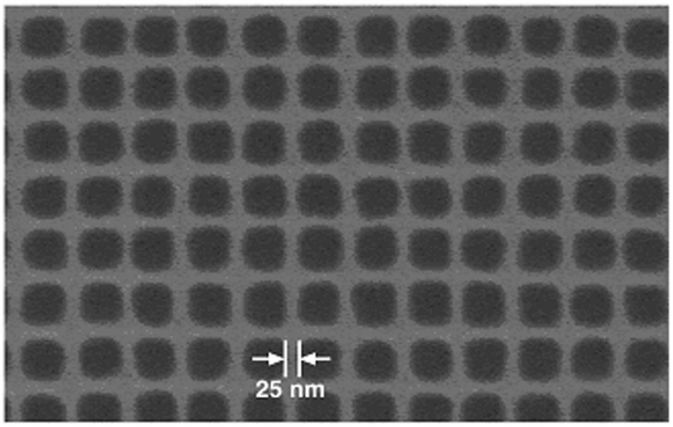

Fig. 60: Scanning electron micrograph of a free-standing 100 nm period grid in a silicon nitride membrane of area 500 micron by 5 mm. Such grids are used in experiments to separate out Helium trimers from other clusters.

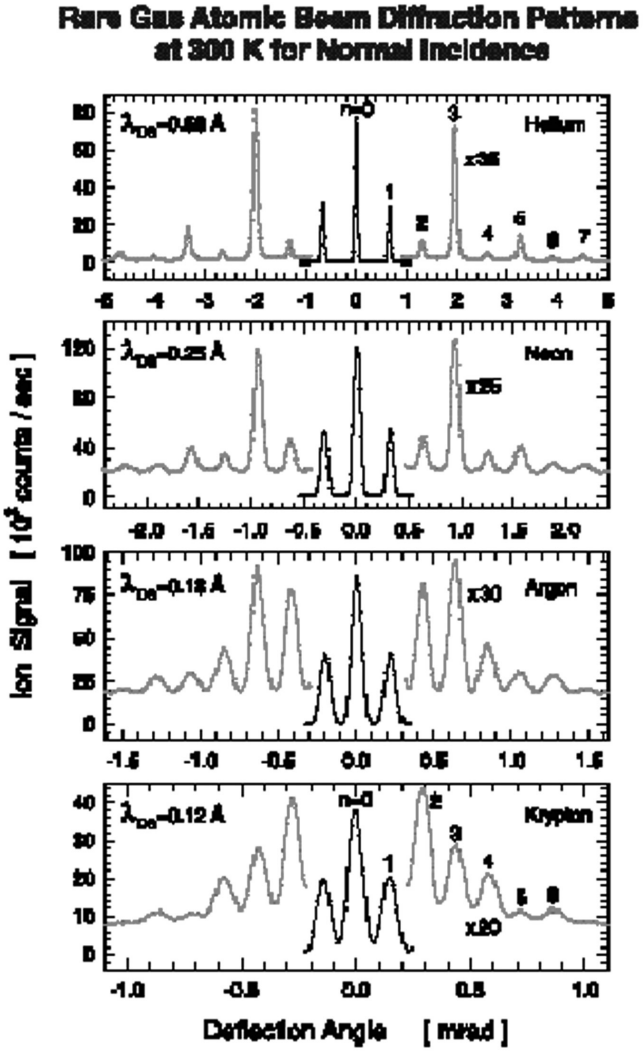

Fig. 61: Rare-gas atom-beam diffraction patterns. These results were obtained by Wieland Schöllkopf and Peter Toennies at the Max-Planck Institute in Göttingen, Germany, using a free-standing, 100nm-period grating

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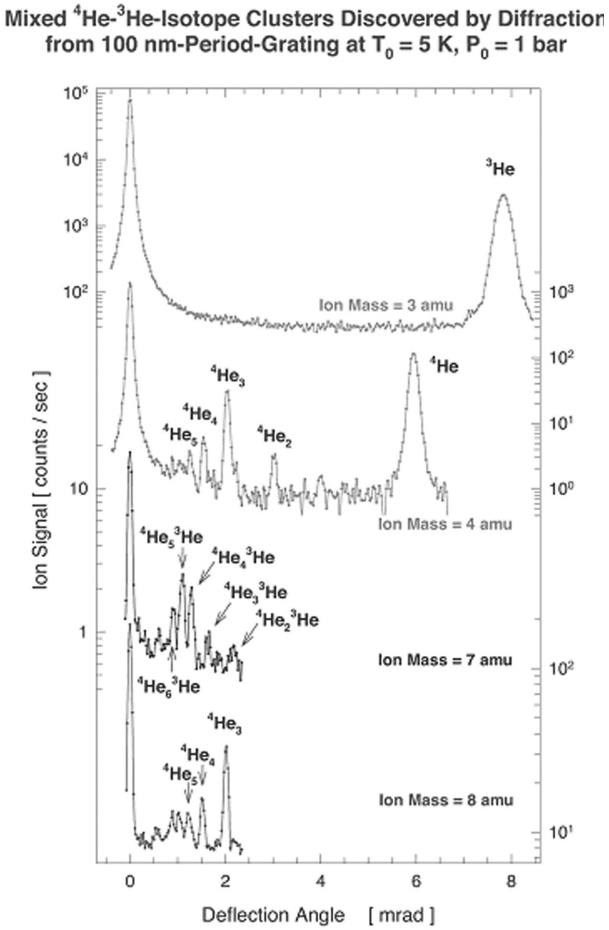

Fig. 62: Non-destructive mass separation of small mixed-isotope helium clusters. These results were obtained by Peter Toennies, et al, at the Max-Planck Institute in Goettingen, Germany, using free-standing, 100 nm-period gratings made in the NSL at MIT.

X-Ray Foil Optics Shaping Technology

Personnel

M. Akilian, C. Forest, Dr. R. Heilmann, and Y. Sun
(C.R. Canizares, G.R. Ricker and M.L. Schattenburg)

Sponsorship

NASA and QED, Inc.

Future X-ray astronomy missions will require orders-of-magnitude improvement in collecting area and resolution. Thin-foil optics are attractive candidates for X-ray telescopes because of the tremendous weight and cost savings which can be achieved compared to traditional monolithic optics. However, substantial improvement in our ability to shape foils to high accuracy is required. In this research program we are developing technology for high-volume shaping of thin (~0.5 mm) glass and silicon substrates, including both reflective and diffractive components.

Over the last several years we have developed methods for thermally shaping glass sheets. This process involves heating the sheet in a furnace until it begins to slump, conforming to quartz or silicon mandrels that have been lithographically patterned with thousands of pins. The pins reduce the surface area of the mandrel to minimize sticking and mitigate the effects of dust particles. We are also developing an alternative slumping method based on air bearings.

We are also developing a complementary shaping process called block lapping. This novel process involves the bonding of foils to rigid polishing blocks, while in their relaxed state, using special UV-cured epoxies and thermoplastics. The bonded foils are then mechanically polished into the desired shape.

A third method involves a process called Magneto-Rheologic Fluid polishing (MRF) to deterministically shape the surface of the substrate. A magnetic polishing compound is entrained onto a spinning sphere that is scanned over the substrate. A magnetic field stiffens the fluid in a confined area generating high shear polishing forces. This method requires an accurate surface error map as input to the MRF shaping machine.

A critical component of this research is accurate surface metrology of thin foils. We are developing a variety

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Nano-Accurate Assembly Technology for X-Ray Foil Optics

Personnel
M. Akilian, C. Chen, C. Forest, R. Heilmann, and Y. Sun (C.R. Canizares, A. Slocum, G.R. Ricker, and M.L. Schattenburg)

Sponsorship
NASA

of Hartmann and Shack-Hartmann surface metrology tools for this purpose, and special fixturing that holds the sheets during metrology, while minimizing holding torques and gravity distortions.

Our short-term goal is to develop foil shaping technology with sub-500 nm accuracy. This will enable a number of important NASA missions such as *Constellation X*. Our long term goal is to realize sub-20 nm shaping accuracy, which will enable diffraction-limited X-ray imaging with resolution improved ~1000X more than today's telescopes.

Future X-ray astronomy missions will require orders of magnitude improvement in collecting area and resolution. Foils optics are attractive candidates for X-ray telescopes because of the tremendous weight and cost savings which can be achieved compared to traditional monolithic optics. However, substantial improvements in our ability to assemble foils with high accuracy are required. In this research program, we are developing microstructures to assemble foil optics, including both reflective and diffractive components.

Plasma micromachining is used to lithographically fabricate silicon "micro-combs" designed to guide and register silicon and glass foils into precise three-dimensional shapes with sub-micron accuracy. Thousands of ~500 μm-thick foils are typically required in an X-ray telescope, each shaped and assembled to form the precise curves or flats that focus X-rays by grazing-incidence reflection. Figure 63 shows SEM images of two types of micro-combs under development.

A prototype flight mirror structure based on these principles has been built and tested. Test results show that glass sheets are assembled to a repeatability of ~0.3 micron, corresponding to an angle error of <1 arc-second. This accuracy exceeds previous foil assembly methods by a factor of ~100. Our microstructure technology is being supported by NASA as the baseline technology for assembling foil optics in the *Constellation X* telescope.

Recent effort seeks to improve the accuracy of the micro-combs from the current level of ~200 nm to under 100 nm. With further progress it may be possible to achieve diffraction-limited X-ray imaging, which can potentially improve the accuracy of telescopes by over 1000X.

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Functional 3D Nanostructures Achieved via Folding of 2D Membranes

Personnel

S.M. Jurga and C.H. Hidrovo-Chavez
(G. Barbastathis and H.I. Smith)

Sponsorship

NSF

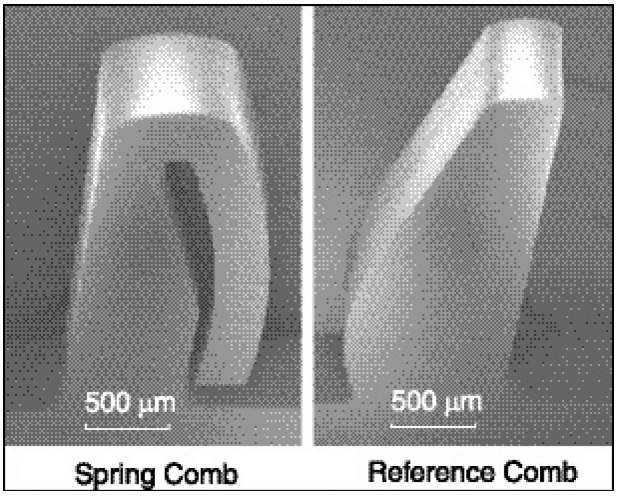

Fig. 63: Electron micrographs of silicon micro-combs. Teeth are ~500 µm wide. a) Spring comb. b) Reference comb.

Functional Three-Dimensional (3D) nanostructures are of interest in numerous technological domains. The 3rd dimension promises to extend micro processors and memories beyond "the end of Moore's law," *i.e.* when feature sizes of planar electronics reach their minimum practical limit. In applications other than electronics, the need to conquer the 3rd dimension is even more urgent; examples include optical elements that integrate sensing and processing for defense or commercial applications, miniature reactors for chemical and biochemical analysis, drug delivery by miniaturized microfluidic implants, micromechanical and nanomechanical energy storage elements, and environmental monitoring and industrial quality control applications. However, 3D fabrication is not well understood and developed. Our CMSE seed grant research is aimed at 1) developing a specific method for 3D fabrication and assembly, which we refer to as "membrane folding.," and 2) conducting a case study in three-dimensional diffractive optical elements.

For a three dimensional technology to be successful and widely applicable to the worlds of solid-state electronics, MEMS, and nanomanufacturing, it must satisfy the functional requirement of sufficient connectivity between the micro and nano devices that compose the system (i.e. the transistors and capacitors of a microchip). Additionally, a winning technology must avoid fighting against the momentum of an existing industry with established tool-sets and large capital investments; a new 3D technology must be easily integrated and compatible with current methods of fabrication that remain planar in nature (i.e. photolithography, plasma etching and deposition are all 2D).

Our approach is a two step process designed to satisfy the following functional requirements: (a) integration of dimensional scales from the nano to the micro and beyond; (b) maximum utilization of existing fabrication tools; and (c) flexibility in achieving a large number

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of possible 3D configurations with minimum cost and maximum repeatability and yield. In the first step, all devices are fabricated on a planar substrate just as they are in today's semiconductor industry. In the second step, the planar substrate is folded into a 3D structure as depicted in Figure 64. Designated compliant zones act as hinges between stiffer regions that contain micro and nano devices. By virtue of compliant circuitry that spans the hinge areas, full 2D connectivity is preserved across the entire length after folding. This is important for electronics as well as communication in MEMS sensors and actuators and integrated nano devices. Connectivity may also be achieved in the vertical, 3rd direction by designing vertical connections to be formed when the planar folds reach predetermined locations during folding.

At present, our study aims to build 3D Diffractive-Optical Elements (3D-DOEs) as a case study in the technology development for folded-membrane devices. 3D-DOEs promise better performance in terms of efficiency and angular selectivity than traditional 2D diffractive-optical elements. Spacing multiple diffractive gratings or Ffresnel zone plates (perhaps as many as 50) vertically above one another establishes a matched filter with very high efficiency. Although such a 3-D structure could be fabricated one layer at a time, the folded-membrane approach should be far more cost effective. Also, the folded membrane approach may enable tuning of the diffractive optical systems, for example, by electrically varying the spacing of the stack.

In our preliminary work, we have demonstrated a single 180 degree fold in a silicon-based device with magnetic-actuation-effectinginduced folding (See Figure 65). The gold hinges are plastically deformed so that the folded membrane remains near 180 degrees. Electron beam evaporated gold was chosen for the compliant hinges due to its high ductility and comparatively small spring back angle. The hinges also complete a current loop around the perimeter of the membrane. By placing the device in a magnetic field and controlling the magnitude of current in this loop, a Lorentz force is generated that rotates the flap about its hinges. The Lorentz force is highly controllable and thus allows extensive experimental characterization of the mechanics of folding in our device. In the future, we will also explore other means of actuation such as stress and chemically-induced folding. Some of these alternatives are more attractive than the magnetic method from the point of view of alignment and flexibility in 3D assembly schemes. is an ideal means of actuation for the first round of prototypes because it is a highly controllable force that allows for good experimental analysis of the mechanics of folding.

The first 3D diffractive device is displayed in its unfolded state, still attached to the substrate in Figure 66. Electrostatic combdrives tune the period of the binary grating, which changes the angle of the diffracted orders. The Fresnel zone plate (essentially a diffractive lens) will be folded over and aligned to the grating as a demonstration of compound diffractive optics in 3D. Future work will focus on the final alignment and latching of the folds in addition to new actuation methods for folding that could be categorized as templated-self-assembly. Work in implementing multiple folds and studying the behavior of multiple folds is also underway. These steps are the early formative building blocks for establishing a multi-use platform. 3D assembly through folding lends itself to a broader goal such as combining discrete devices of varied functionality (optics, electronics, microfluidics, etc) into one cohesive, self-contained system capable of multiple tasks such as advanced sensing and response.

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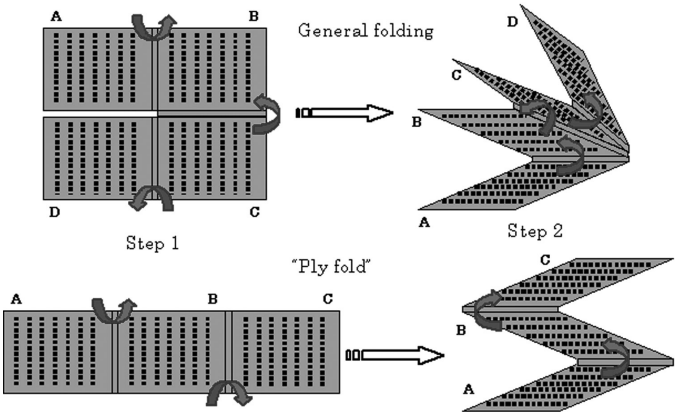
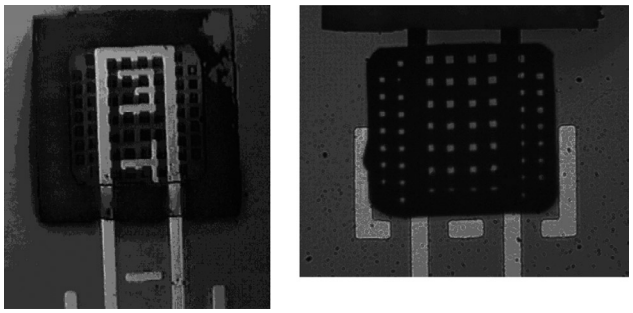


Fig. 64: Examples of how 3D structures can be obtained by folding pre-fabricated thin 2D membranes in a two step process. Black dots



denote surface features nanofabricated on the membrane surface. Fig. 65: Membrane flap before folding (left) and after folding to 180 degrees (right). Note the alignment tolerance achieved in folding. (Alignment fiducials are 50mm wide).

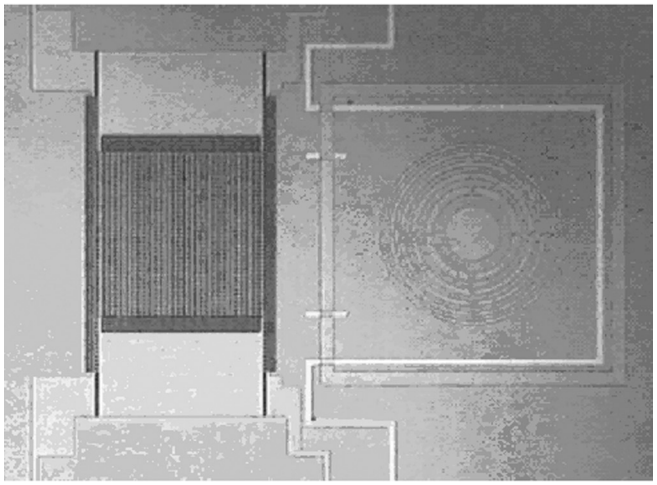


Fig. 66: Top view of tunmable grating (left) and static Fresnel zone plate (right) before release from substrate and before folding.

Integration of Nanowires Embedded in Anodic Alumina Templates with a Large Silicon Substrate

Personnel

O. Rabin, P. R. Herz, Y.-M. Lin, and S. B. Cronin (A. I. Akinwande and M. S. Dresselhaus)

Sponsorship

Navy, ONR MURI, DARPA, and ONR

More and more new miniature devices include nanowire components, exploiting the unique properties of these nanostructures for optical, electronic, and sensing applications. Nanowires can show enhanced quantum and surface effects, while still providing a guiding path for electrons or photons to transmit electrical or optical signals, respectively. In this context, we have developed a non-lithographic process to fabricate arrays of metallic and semimetallic nanowires, aligned perpendicular to the surface of a silicon wafer. The process takes advantage of the self-assembly of an array of pores during the anodization (electrochemical oxidation) of aluminum to Porous Anodic Alumina (PAA). The PAA is grown on top of a silicon wafer coated by a conductive layer (Ti or Ti/Pt) which serves both as an adhesion layer to the wafer, and as an anodization barrier to protect the wafer. The PAA is used as a template for the growth of nanowires by filling its pores with the chosen nanowire material. This can be done electrochemically, using the conductive layer on the wafer as a cathode for the electrodeposition of metallic nanowires into the pores of the PAA. The geometrical parameters of the PAA (thickness and pore diameter, controlled by the anodization conditions) dictate the shape of the wire, while the electrodeposition process dictates its composition profile. In addition to the mechanical advantages of mounting the nanowire arrays on silicon wafers, this process greatly facilitates the establishment of electrical contact to both ends of millions of nanowires, which we utilized to measure the transport properties of these arrays (See Figure 67). The integration of the array on a silicon wafer offers a convenient way to construct nanowire-based devices, such as field emitters, thermoelectric coolers, and photo-diodes.

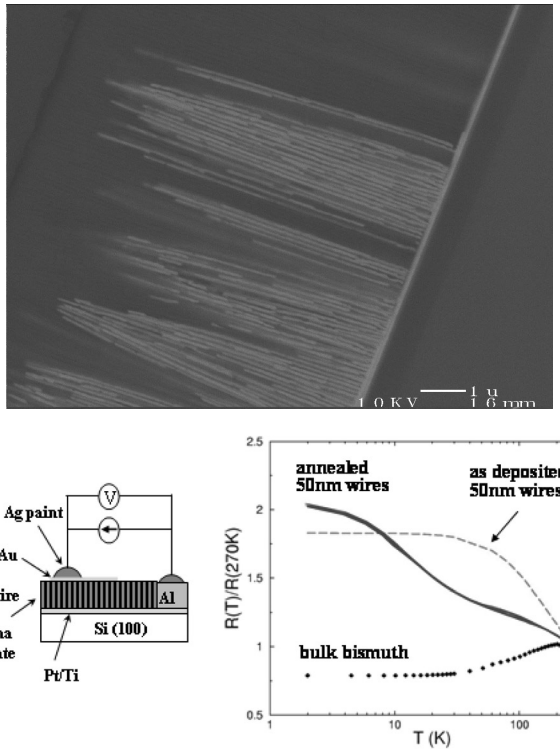


Fig. 67: Cross-section SEM micrograph of bismuth nanowire arrays grown on a Pt-coated silicon wafer. Scheme of 2-point resistance measurement setup. Resistance versus temperature characteristics of electrodeposited bismuth nanowire arrays.

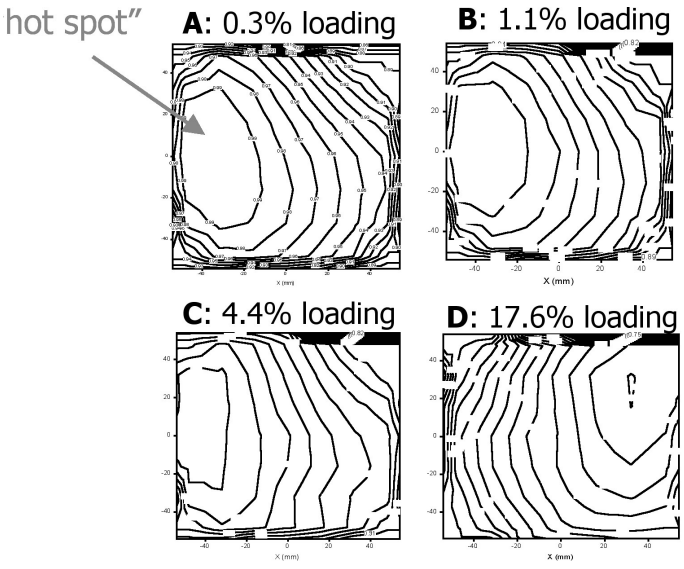
Opposite page:

Normalized wafer-scale DRIE etch rates. Uniform grid of circles etched with diameter Φ *and separation distance* Δ *(mm/mm): A (0.6/16); B (2/16); C (2/8); D (2/4).*

Courtesy of T. Hill, H. Sun, H. Taylor, D. Boning, and M.A. Schmidt.

Sponsor:
CMI, ARO, and DARPA.

Manufacturing, Modeling and Simulation



Manufacturing, Modeling and Simulation

- *Characterizing Process Variation Using a Ring Oscillator Based Test Chip*
- *Modeling of Deep Reactive Ion Etching (DRIE) for MEMS Manufacturing*
- *Modeling of Pattern Dependencies in the Fabrication of Multilevel Copper Metallization*
- *Modeling of Nanoscale Advanced Devices*
- *Modeling of Shallow Trench Isolation CMP*

Characterizing Process Variation Using a Ring Oscillator Based Test Chip

Personnel

K. Gonzalez-Valentin and J. Panganiban (D. Boning)

Sponsorship

SEMATECH and IBM

Process variation is an increasingly difficult challenge in the design of high-yielding integrated circuits, and techniques are needed to measure and extract variation in a given process and link it to circuit performance. A test chip implemented in the MOSIS 0.25 μm TSMC process has been designed and fabricated, containing test structures aimed at extracting gate-length, interconnect geometry, threshold voltage, and other process variations. The core test structure is a Ring Oscillator (RO) composed of an odd number of cascaded inverters; since the RO frequency is dependent on device parameters and the load between stages, distributions of measured RO frequencies can be used to characterize variation in the devices and interconnect loads.

The 2.5 mm by 4.0 mm test chip is composed of forty-five unique ring oscillator types, which are replicated throughout the chip to incorporate over two-thousand RO test structures. Approximately half of the test structures are used to extract Front-End-Of-Line (FEOL) variation, such as gate-length and threshold voltage, while the other half concentrates on interconnect and Back-End-Of-Line (BEOL) process variation. A scan chain architecture, as shown in Figure 1, is used to enable frequency measurement of each structure. The basic building block is a "tile" which includes a single ring oscillator test structure as well as control circuitry responsible for enabling the RO and outputting the RO signal onto a horizontal bus which feeds into frequency dividers. These tiles are cascaded side by side to compose a row, and these rows are replicated vertically. In addition to increased RO density, this architecture allows for efficient data collection on the board level using Labview-based digital I/O without the need to probe the die for individual RO measurements.

Testing of fabricated chips confirms the functionality of the control architecture. Table 1 summarizes a subset of device variation ROs. Density vs. isolation analysis shows that as the number of fingers increases, the variation increases for all types of structures, likely due to ΔL changes. The polysilicon effect analysis shows that both local and global density of polysilicon affect circuit performance, with decreasing frequency as the poly proximity or density around the ROs increases. The proximity or local effect has a more drastic impact than the global or polysilicon density effect. All vertical structures have a larger standard deviation and lower frequency than their corresponding horizontal structures; designers should take the orientation of digital circuits seriously to achieve good matching. Chip-to-chip variation has proven to be larger than the within-chip variation for almost every structure. Future work includes further investigation of random and systematic device and interconnect variation sources, and relating these to circuit impact.

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Description	Mean Freq. [MHz]	σ Total [KHz]	σ wafer [KHz]	σ within-chip [KHz]	Variation Effect
Three Finger RO	4.42	130	122	45	Canonical Structure
2 Fingers, 1.5x Min L	4.21	76	73	19	Density vs. Isolation Effect
4 Fingers, Min L	2.76	77	71	28	
2 Fingers, 2x Min L	2.64	39	36	15	
1 Finger, 4x Min L	2.7	29	25	13	
1.2x Spacing	4.3	132	123	48	Proximity of Polysilicon Finger Effect
1.5x Spacing	4.2	127	122	34	
2x Spacing	4.13	129	120	46	
3x Spacing	4.12	135	126	49	
Vertical Canonical FEOL	4.36	144	135	51	
Vertical, 3x Spacing	4.05	143	134	49	
Vertical Single Finger	4.22	59	51	30	
0% Polysilicon Density	4.38	126	124	27	Polysilicon Density
12% Polysilicon Density	4.36	127	125	23	
25% Polysilicon Density	4.32	129	125	30	
50% Polysilicon Density	4.29	128	124	33	
Canonical at end of Density	4.38	126	120	40	
Single Finger	4.25	52	47	22	Single Finger
Small Single Finger	4.23	51	48	18	

Table 1: Comparison of differently laid out ring oscillators with the same gate length

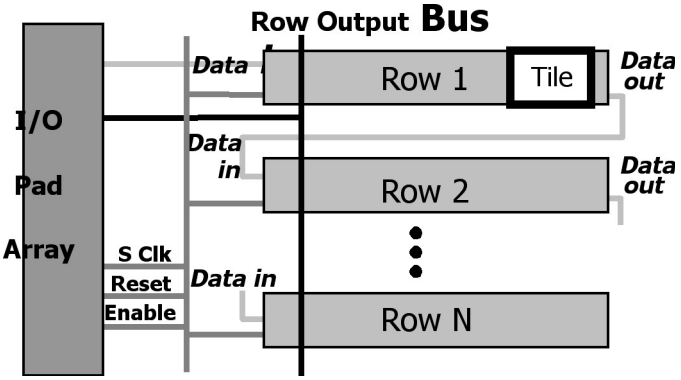

Fig. 1: Variation test chip architecture.

Modeling of Deep Reactive Ion Etching (DRIE) for MEMS Manufacturing

Personnel

T. Hill, H. Sun, and H. Taylor
(D. Boning and M.A. Schmidt)

Sponsorship

CMI, ARO, and DARPA

MEMS devices have become increasingly prevalent in recent years. An important distinction between MEMS and conventional IC fabrication is a need for high aspect ratio structures. Deep Reactive Ion Etching (DRIE) can successfully produce such features. However, wafer and feature level non-uniformities may result when multiple devices are placed on a single wafer. Understanding uniformity issues is critical to high volume MEMS manufacturing. While the immediate benefit of this project would be better yield for the Microengine Project, the knowledge gained here can be applied to many current and future MEMS devices.

We have developed a software model to simulate DRIE uniformity given a mask design. The basic idea of the model is to develop a filter based on the physical flow behavior of etchant in the etch chamber. The filter transfer function can then be convolved with the mask map to obtain an etch map. Currently, the filter is based on the diffusion equation. In this equation, there are two important parameters: the reaction coefficient **k** and the diffusion coefficient **D**, which represent the consumption rate of silicon and transport rate of etchant to the etching area. A set of test masks has been designed to identify parameters **k** and **D** for a specific recipe. We assume the etching occurs in the transport limited regime. The assumption behind this model is that the etch rate variation is caused by etchant density variation along the wafer. The area close to the etch area will be etched more slowly than the area away from the exposed etch area due to a depressed etchant density. The inputs of this model are a mask design layout, **k** and **D** (based on the specific recipe), filter (current diffusion model), and a global etch map. The output is an etch variation map.

Experiments have been conducted to verify/debug the model. There appears to be a connection between the wafer loading (ratio of etched/un-etched area) and the uniformity pattern (See Figure 2). We are specifi-

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cally focusing on the Bosch method of etching, which includes cycles of SF_6 etching, followed by C_4H_8 passivation. Test patterns were etched for 30 minutes in a Surface Technology Systems (STS) etcher with 11 and 13 second etch and passivation cycles, respectively. Masks with a loading ratio below 10% exhibit a "hot spot" with higher than average etching, while those with higher loading have a "cold spot." Other experiments include examination of aspect ratio (feature size) dependence, depth dependent etch rate, photoresist wafer mounting, and the effect of dummy fill on etch rate.

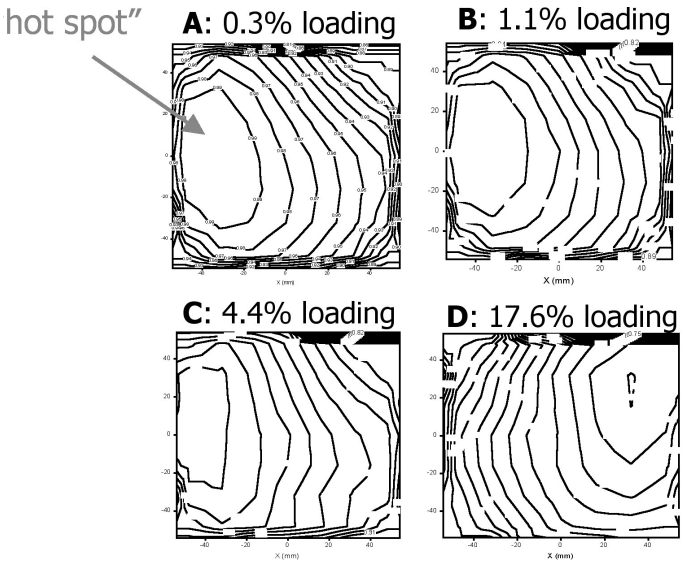

Fig. 2: Normalized wafer-scale DRIE etch rates. Uniform grid of circles etched with diameter Φ and separation distance (mm/mm): A (0.6/16); B (2/16); C (2/8); D (2/4).

Modeling of Pattern Dependencies in the Fabrication of Multilevel Copper Metallization

Personnel

H. Cai and T. Park (D. Boning)

Sponsorship

Hynix Semiconductor, NSF/SRC ERC for Environmentally Benign Semiconductor Manufacturing, Praesagus, Inc.

Multilevel copper metallization is an active and critical area of research and development in industry and academia to meet performance requirements for future advanced interconnect technologies with sub-micron dimensions. It is well known that multilevel topography resulting from pattern dependencies in plating, deposition and CMP is a major problem in interconnects. An integrated pattern-dependent chip-scale modeling of multilevel copper metallization is needed to help optimize the design of multilevel copper metallization to achieve higher yield and performance. The existing integrated chip-scale model of pattern dependencies developed by Park and Gbondo-Tugbawa is the basis to further develop the copper plating and CMP models for multilevel copper metallization for realistic interconnect. New model development and tuning make use of the existing MIT-developed 854 multilevel mask. At the same time, a simple model for pattern dependent inter-level dielectric (oxide) deposition is being developed and incorporated into the model to help address topography creation in multilevel interconnects. CVD or spin-on processes eventually will also need to be characterized for future low-K dielectric deposition, and the multilevel copper metallization modeling will be applied to more aggressive and advanced multilevel copper/low-K metallization processes.

Cooperation with Hynix is in progress and provides access to fine feature multilevel interconnect processes and data. The electroplating process is characterized by using an MIT-designed test mask. The pattern-dependent electroplating model is first applied to fit experimental data, extract model parameters, and finally, to perform topography profile simulation across an entire chip. Wafers are patterned with the MIT 854 mask (metal 1 layer) and electroplated with two baseline processes of different target thicknesses: 8500 Å and 11500 Å. It has been found that the model root-mean-square errors are generally less than 300 Å. To perform

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chip-scale simulation, a layout extraction tool is used to obtain relevant layout information, such as pattern density and line width distributions, from the MIT 854 test mask. Using the extracted model parameters and the layout information, topography height is simulated for each grid cell of the entire chip, and the result shows good match between the model result and measured data. The simulated result for the entire chip (target thicknesses 8500 Å) is shown in Figures 3 and 4.

CMP process simulation and model verification are in progress for metal 1; the next stage of work will focus on multilevel effects with electroplating and CMP of metal 2 test structures.

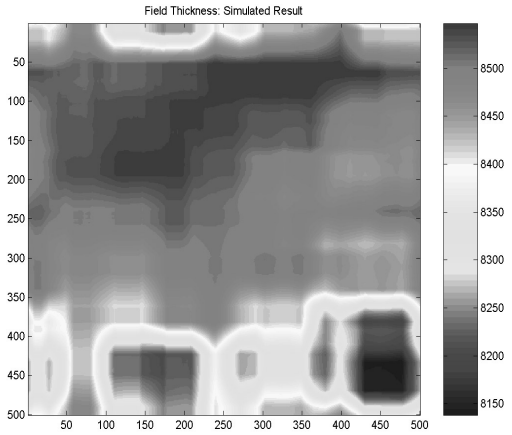

Fig. 3: Field Thickness: Simulation Result

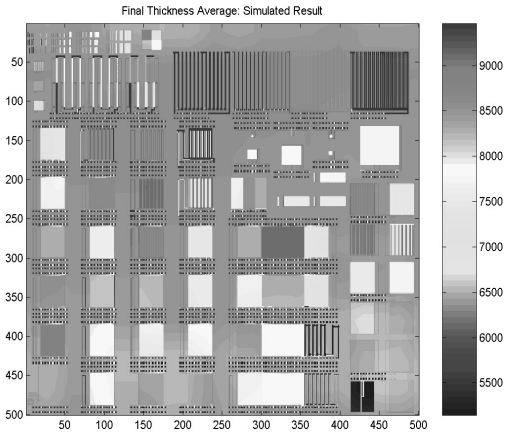

Fig. 4: Final Thickness Average: Simulation Result

Modeling of Nanoscale Advanced Devices

Personnel
O. M. Nayfeh and S. Yu (D. A. Antoniadis)

Sponsorship
SRC

Demand for miniaturization and higher performance have pushed Modern Electronic Devices into the sub-50 nanometer regime. Minimum feature sizes have been continuously reduced, and new mobility-enhanced materials have been engineered by modern epitaxial technology to increase a devices functional complexity and improve performance.

However, at the nanometer scale, electrons come under the influence of High Electric Fields, and the Quantum Mechanical wave nature of electrons is exposed. These effects have a direct impact on the design of high performance "well-tempered" devices; devices that exhibit large on-current while still maintaining electrostatic integrity by minimizing the current in the off-state.

Computer simulation is a dominant mechanism in direct quantitative 2-D characterization of sub-50nm devices; exploring new possible "well-tempered" device structures, and in studying transport and electrostatic phenomenon in materials/devices in general. Simulation models must be fast and accurate.

Correct quantum mechanical correction is critical in the inverse modeling methodology. Quantum Correction of Subthreshold IV, Cgsd-V, and the Cgg of the gate-stack, are all crucial elements in extracting the elaborate 2-D doping profile and oxide thickness of a modern device. Accurate inverse modeling enables robust calibration of carrier transport models that can then predict device behavior. For treating the quantum mechanical nature of electrons, a full-Schrodinger solution is accurate, yet extremely time-consuming. Other methods, including the Density Gradient and the VanDort approximation, have have been shown to be extremely robust in capturing these effects, yet more time-friendly than a full-Schrodinger treatment. In this research, we explore the effect of different quantization models on 2-D device characterization.

With correct device characterization, we then use computer simulation ranging from Full Band Monte Carlo techniques to widely used device TCAD tools to explore high-field transport and electrostatics in materials/devices at the Nanoscale. We are evaluating the benefit from mobility enhanced materials such as Strained-Silicon, and Germanium, in terms of drive current in real device substrates in the sub-50 nanometer regime.

Modeling of Shallow Trench Isolation CMP

Personnel
X. Xie (D. Boning)

Sponsorship
National Semiconductor Corporation

As advancing technologies increase the demand for planarity in integrated circuits, nanotopography has emerged as a new challenge in Shallow Trench Isolation (STI) on wafers polished by means of Chemical-Mechanical Planarization (CMP). Nanotopography – starting silicon surface height variations 100 nm in amplitude extending across millimeter-scale lateral distances – can result in CMP-induced localized thinning of surface films such as the oxides or nitride used in STI.

Two alternative approaches for simultaneous simulation of both pattern and nanotopography effects are implemented to better understand the impact of nanotopography on STI CMP. In the first approach, we perform a "pure" contact wear simulation on a finely discretized grid. Because of high computational demands, this approach is only feasible for one-dimensional cut lines. In the second approach, an integrated model incorporating contact wear and density/step-height effects in STI CMP is used. A contact-wear component on a coarsely discretized grid accounts for pressure differentials across the chip due to long-range nanotopography and other surface height variations. Patterned feature effects are then captured by a pattern density and step-height dependent component. This makes feasible 2D simulations of patterned structures over underlying uneven surfaces to study the effect of realistic nanotopography maps on the CMP of STI patterns. The simulation shows that nanotopography results in longer oxide clearing time, in agreement with previous work. Depending on the specific random configuration of any given nanotopography map, either more or less nitride erosion may result despite the increased polishing time (as illustrated in Figure 5). Thus, nanotopography effects should be considered an additional component of STI nitride loss budgets, in addition to that required by layout pattern dependencies.

Applying the contact mechanics-based model formulations, we re-examine the physical basis of several chip-scale CMP models proposed by our group. Planarization length, as the key concept of all pattern density related models, is the characteristic length of an elliptic weighting function based on the long-range pad deformation and pressure distribution during CMP. This semi-physical model is often adequate and usually gives a fitting error of a few hundred angstroms. A more physical understanding of the model will enable us to develop a chip-scale CMP model with better accuracy. We also investigate different weighting shapes, including square, cylinder, Gaussian, and elliptical filters by comparing the results with experimental data.

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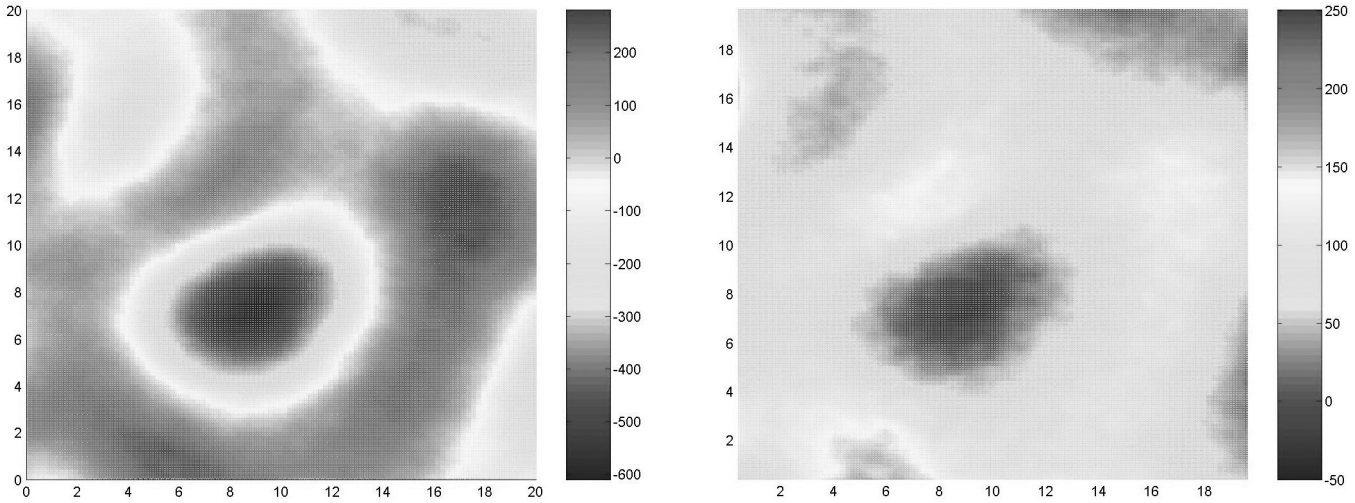


Fig. 5: (a) Nanotopography map measured on a chip size region on bare wafer; (b) Additional nitride erosion caused by the nanotopography shown in (a); height variation is shown in color bar and is in angstroms

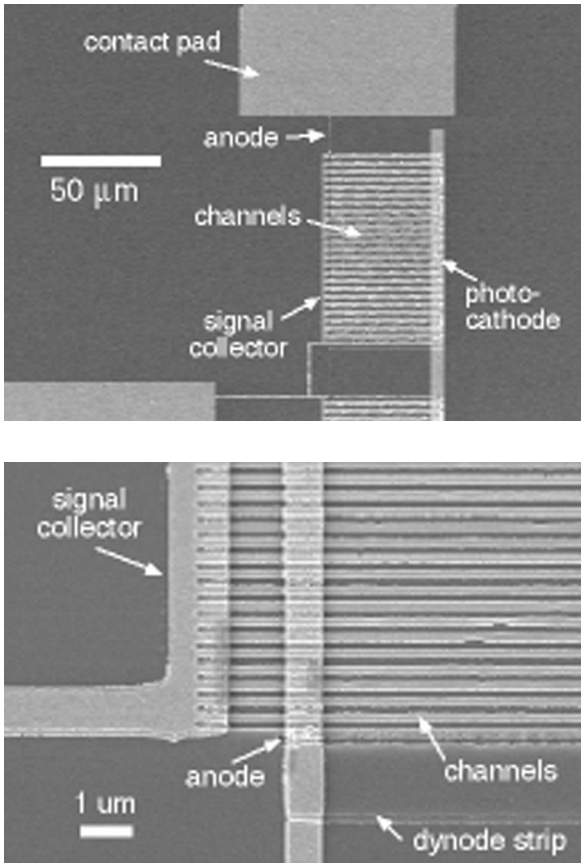
Opposite page:

These SEM images show a prototype microphotomultiplier. Three levels of conformable-contact photolithography, which includes two aligned levels, were carried out in fabricating this device. A large-area view is shown in (a), and a close-up view of the lower left corner of the device is shown in (b).

Courtesy of J. Daley, J.G. Goodberlet, H. Kavak, and V.H.S. Moorthy (H.I. Smith)

Sponsor:
DARPA

Fabrication Technology



Fabrication Technology

- *A Silicon Through-Substrate Interconnect Technology and Applications*
- *Alternative Chemistries for Wafer Patterning*
- *Solventless Lithography*
- *Fabricating Advanced Microsystems with Conformable-Contact Photolithography*
- *Hot Filament Chemical Vapor Deposition of Polyoxymethylene as a Sacrificial Layer for Fabricating Air Gaps*

A Silicon Through-Substrate Interconnect Technology and Applications

Personnel

J. H. Wu (J. A. del Alamo, in collaboration with K. A. Jenkins, IBM, and R. Livengood and P. Winer, Intel)

Sponsorship

MARCO Focused Research Center on Interconnect (MARCO/DARPA) and Intel

Si CMOS and HBT device technologies have shown their potential for use in systems operating in the millimeter-wave (mmw) range. A Si-based mmw mixed-signal IC technology would make available a large portion of bandwidth for affordable and pervasive applications. Perhaps the greatest challenges in front of this technology are low-loss interconnects (especially power and ground), substrate isolation in the millimeter-wave regime, thermal management, and cost-effective, low-loss packaging. Several of these problems arise from the Si substrate under the active devices. MEMS-like engineering of the substrate can effectively deal with these challenges. Exploring these opportunities for operation in the mmw regime is the goal of this project.

We have developed a high-aspect ratio, substrate-via technology that allows for ground distribution with very low impedance. We have also shown that this technology has the potential for compact, yet effective substrate crosstalk isolation. Both applications have been demonstrated up to 50 GHz. This simple, through-wafer interconnect technology has potential for addressing other substrate issues in the mmw regime (See Figure 1).

In addition to ground connections, through-wafer vias could be used to distribute power as well as ground through the substrate on the same chip. In ICs, decoupling capacitors used to minimize power and ground bounce are discrete components external to the chip package. As clock frequencies increase, more capacitance is required ever closer to the chip. Decoupling capacitors could be integrated on-chip using the very substrate vias that are used to distribute power and ground.

Our substrate-via concept is currently based on solid vias filled with Cu. These vias represent ideal heat shunts from the wafer surface to its back. Vias strategically located around the chip can minimize hot spots on a chip and ease thermal management. Finally, in the millimeter waver regime, system-in-package concepts will have to be utilized to integrate entire systems from chips fabricated using specialized Si processes. A small-footprint substrate-via technology will allow the compact stacking of multiple chips using flip-and-bond concepts.

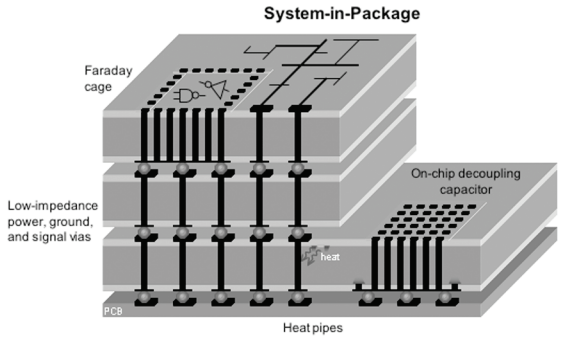


Fig. 1: Conceptual picture of a system-in-package utilizing through-substrate vias as low-impedance power, ground, and signal interconnects, heat pipes, on-chip decoupling capacitors, and a Faraday cage for substrate crosstalk isolation.

Alternative Chemistries for Wafer Patterning

Personnel
R. Chatterjee and A. Somani (R. Reif)

Sponsorship
NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

The goal of this project is to identify possible alternatives for perfluorocompound chemistries for wafer patterning of dielectric films that do not pose long term environmental problems. The etch viability of a variety of alternatives has been determined, and the most promising candidates from the etch viability study will be further tested to define an alternative wafer patterning process. The effluents are identified with Fourier Transform Infrared Spectroscopy (FTIR) to assess their potential ESH impact. Beta testing of alternative processes are performed at the facilities of industrial collaborators.

Gases such as fully fluorinated alkanes - CF_4, C_2F_6, C_3F_8 - as well as inorganic compounds like NF_3 and SF_6, collectively termed as PerFluoroCompounds (PFCs), are used heavily by the semiconductor industry for the etching of dielectric films in wafer patterning applications. Their use and emission is problematic, however, from an environmental standpoint because of the global warming nature of these substances coupled with their long atmospheric lifetimes.

This report highlights recent work accomplished in the development of etch processes with alternative chemistries, specifically C_4F_6, for etching Dow-Corning XLK spin on low-k films. The experimental work has taken place on an Inductively coupled Plasma Etcher (IPS) at Motorola; diagnostic tools include optical emission spectroscopy for plasma analysis and FTIR spectroscopy for effluent analysis.

The dielectric stack of the ultra low-k XLK films is shown in Figure 2. This is one of the most complex film stacks. There is a thin Bottom Anti-Reflective Coating (BARC) underneath the 4000 A photoresist. Under the BARC is a thin oxide layer and a thin hard SiCN capping layer, followed by the ultra low-k film, and finally, a SiCN stop layer.

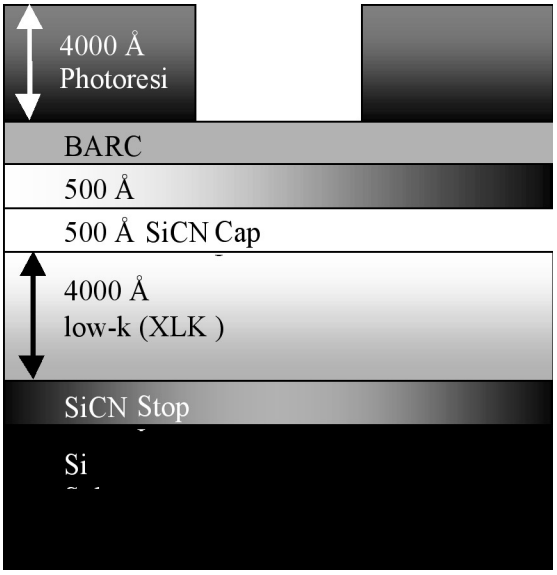


Fig. 2: XLK and LKD wafer film stack with via test structure critical dimensions as low as 0.25 μm (not drawn to scale).

The *c*-C_4F_8 reference process on the IPS (IPS-LK3-XLK), as shown in Figure 3, exhibits high selectivity to SiCN underlying film, as well as good etch selectivity to the photoresist. There was no evidence of CD blowout on this process. The total global warming emissions from this process run on the LKD film were 0.120 kgCE.

The cross-sections of the 0.25 μm CD vias of the hexafluro-1,3-butadiene process are shown in Figure 4. They look very similar to the *c*-C_4F_8 process of comparison,with a similar via profile; selectivity to the underlying SiCN stop layer, and selectivity to photoresist. The hexafluoro-1,3-butadiene process (IPS-LK4-XLK) has a slightly reduced CD blowout. The total emissions from this process were 0.026 kgCE, which represents a 78.7% reduction compared to the *c*-C_4F_8 process of comparison. Etch rates of both the process look alike.

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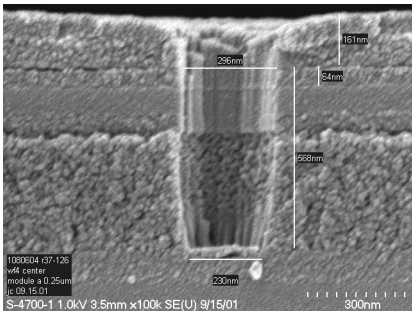
The quantity of each effluent emitted for two different IPS process is shown in Figure 4. It is evident that these films have similar emissions in similar conditions. It also shows that *c*-C_4F_8 is one of the major contributors to emissions because of its poor destruction efficiency. Thus, shifting to low global warming gas such as C_4F_6 is beneficial.



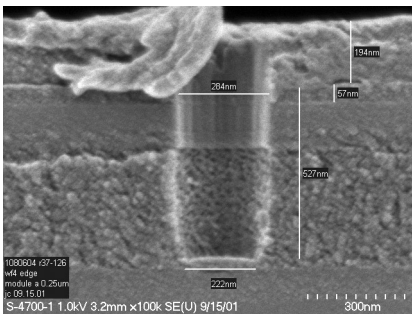
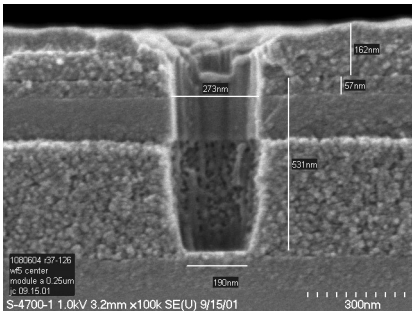


Fig. 3: 0.25 μm via cross sections for IPS c-C_4F_8 process of comparison for LKD film. BARC BT: 800 W Outer, 400 W Inner, 300 W Bias, 4 mT, 5 sccm c-C_4F_8, 10 sccm O_2, 100 sccm Ar, 15s; SiCN BT: 1000W Outer, 200 W Inner, 300 W Bias, 15 sccm c-C_4F_8, 5 sccm O_2, 100 sccm Ar, 25s; Main Etch: 1540 W Outer, 260 W Inner, 1800 W Bias, 7 mT, 8 sccm c-C_4F_8, 100 sccm Ar, 60s. (IPS-LK3-XLK)



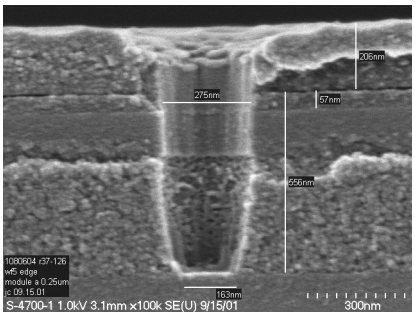


Fig. 4: 0.25 μm via cross sections for the best IPS hexafluoro-1,3-butadiene process for LKD film. BARC BT: 800 W Outer, 400 W Inner, 300 W Bias, 4 mT, 5 sccm C_4F_6, 10 sccm O_2, 100 sccm Ar, 15s; SiCN BT: 1000W Outer, 200 W Inner, 300 W Bias, 10 sccm C_4F_6, 5 sccm O_2, 100 sccm Ar, 25s; Main Etch: 1540 W Outer, 260 W Inner, 1800 W Bias, 7 mT, 12 sccm C_4F_6, 100 sccm Ar, 60s. (IPS-LK4-XLK)

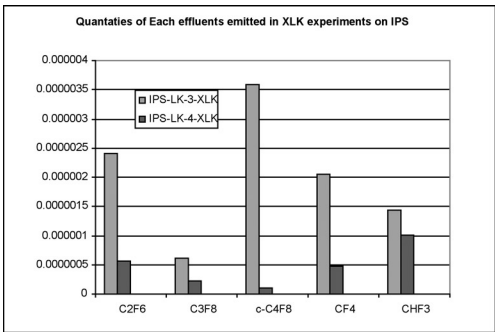


Fig. 5: Quantity of each effluent emitted for XLK and LKD processes on IPS.

continued

Solventless Lithography

Personnel

Y. J. Mao (K. K. Gleason in collaboration with P. Nguyen and Prof. C. K. Ober of Cornell University)

Sponsorship

NSF/SRC Engineering Research Center for Environmental Benign Semiconductor Manufacture

Current semiconductor manufacturing uses a solvent intensive photoresist processing to lithographically define features at every mask level. In each of the dozens of mask levels per wafer, significant volumes of liquid waste are generated during the deposition, development, and stripping of the photoresists. Thus, photoresist processing presents a clear need and opportunity to reduce environmental, safety, and heath impact of the microelectronics industry. The strategic solution is to design a patterning process that completely eliminates wet chemical steps. Moving towards sustainable, solventless lithography is advantageous since this "dry" processing requires less materials usage, fewer processing steps, lower energy consumption and waste disposal; translating to lower overall cost.

Solventless lithography was demonstrated by integration of two novel technologies: The resist layer was applied using Hot Filament Chemical Vapor Deposition (HFCVD) and subsequently, developed in supercritical carbon dioxide ($scCO_2$). Vapor deposition of "dry" resists of sensitivity comparable to conventional spin-on materials requires promotion of those reactions that form linear polymeric chains over reaction pathways which would normally lead to either crosslinked networks or to the destruction of sensitive functional groups. Such selective control is extremely difficult to achieve using conventional plasma enhanced CVD. In contrast, hot filament excitation can be much "gentler" and thus, possesses a greater potential for achieving selective control over vapor deposition process. The low excitation energies of HFCVD allow for the design of film stoichiometry through control over precursor fragmentation and polymerization pathways. HFCVD from the precursor, glycidyl methacrylate (GMA), requires only modest filament temperatures of 200-250 °C. Even though < 0.05 W/cm^2 power is utilized, the HFCVD rates from the precursor mixture of GMA with an initiator can exceed 200 nm/min.

Calculation shows that the material utilization efficiency exceeds 10% in this HFCVD process. The films also demonstrate excellent uniformity and smoothness with thickness variation less than 2% and rms roughness less than 2 nm which is very promising for potentially deceasing Line Edge Roughness (LER).

Dry resists created by HFCVD from GMA demonstrated high sensitivity (<5 μC/cm^2). The plasma enhanced CVD film deposited from GMA could not be similarly patterned. Thus, the structural characteristics of the HFCVD film, including the absence of crosslinks and retention of functional groups, appear to be crucial for creating CVD resists.

To achieve dry development, the HFCVD process was engineered to enhance the polymer's solubility in sc CO_2. Specifically, a fluorine containing monomer, fluoroalkyl acrylate (FAA) was introduced along with GMA as a precursor feed. The result was a high sensitivity dry resist composed of the copolymer of GMA with FAA which could be developed by sc CO_2 after e-beam exposure. A scanning electron micrograph of line and spaces for this solventless lithography process is shown in Figure 6.

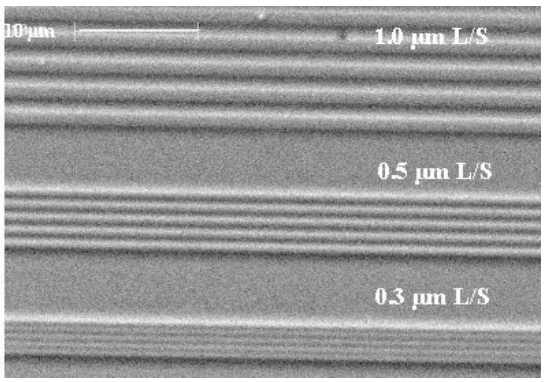


Fig. 6: Solventless lithography using a dry resist developed by supercritical CO_2 after e-beam exposure, demonstrating 0.5 μm and 0.3 μm line/spaces pattern in the vapor deposited copolymer of GMA and FAA.

Fabricating Advanced Microsystems with Conformable-Contact Photolithography

Personnel
J. Daley, J. G. Goodberlet, H. Kavak, and V. H. S. Moorthy (H. I. Smith)

Sponsorship
DARPA

The goal of this research program is to apply Conformable-Contact Photolithography (CCP) to the fabrication of novel or technologically advanced sub-micron devices. In a previous program under the same sponsor, it was shown that CCP enables low-cost, sub-100-nm patterning with sub-100-nm overlay capability. A particular thrust of this program is to use CCP in the development of a novel integrated photomultiplier termed the "microphotomultiplier." This device would enable on-chip, ultrasensitive, and ultrafast photodetection for potential applications in optical, biochemical sensing, communications or low-light-level imaging technologies. Also during this program, the CCP technology has been transferred to a company that is developing grating-based, integrated-optical devices for signal multiplexing/demultiplexing, and to a foreign university with an active program in near-field photolithography. Additionally, a local company has begun manufacturing equipment to make CCP available to universities or small businesses with interests in deep sub-micron patterning, but constrained by limited budgets.

The microphotomultiplier, illustrated in Figure 7 and described in last year's report, poses several fabrication challenges. Long, deep, narrow channels, which provide electron amplification, must be patterned and etched into the substrate. Channels with high aspect ratio, defined as length divided by width, provide greater electron multiplication or device gain and are preferred. To reduce the overall size of the device, and reduce the difficulty in sealing the channels for vacuum operation, narrower channels are preferred. After etching the channels, the walls must be coated with a resistive film that enhances secondary electron emission and prevents their charging. Further, a photocathode must be fabricated at one end, and two closely-spaced electrodes, the anode and signal collector (not shown in the figure), must be defined at the opposite end to enable photodetection, device bias, and signal detection.

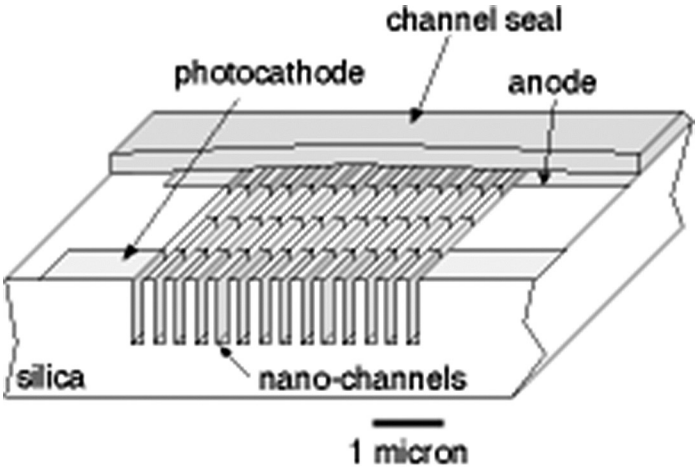


Fig. 7: This cut-away illustration of the integrated microphotomultiplier shows the electron-amplifying channels and device electrodes. This device offers the promise of ultrasensitive and ultrafast photodetection in a micro-scale package.

For the first fabrication attempts, the microphotomultiplier's channel width was chosen to be about 125 nm, and several device lengths, ranging from about 3 μm to 50 μm were trialed. There were typically 200 or more channels in a single device. The channels were defined in the first level of lithography and subsequently, etched into an oxide substrate. In the second level of lithography, a resistive strip was aligned to the channels with better than 200 nm overlay accuracy. (In a separate alignment evaluation experiment, it was shown that sub-50-nm overlay accuracy could be achieved.) Amorphous silicon was deposited to define the resistive strip. In a third level of lithography and subsequent processing, the photocathode, anode, and signal collector were defined in gold. The use of gold enabled photoemission, at short-wavelength radiation, and would not rapidly degrade upon exposure to air. The anode was spaced about 800 nm from the signal collector. A prototype device, fabricated through these three levels of lithography is shown in Figure 8. All levels of patterning and alignment were done using CCP techniques.

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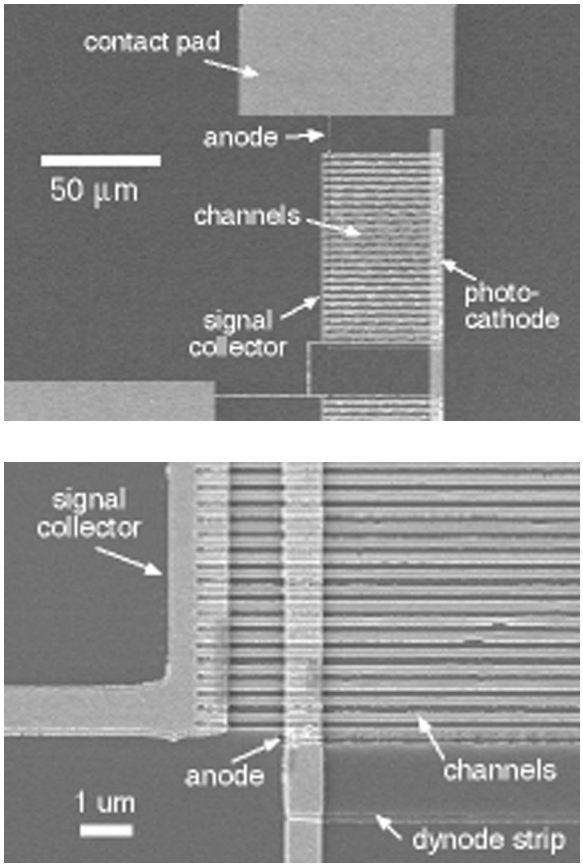

Fig. 8: These SEM images show a prototype microphotomultiplier. Three levels of conformable-contact photolithography, which includes two aligned levels, were carried out in fabricating this device. A large-area view is shown in (a), and a close-up view of the lower left corner of the device is shown in (b).

Preliminary device testing was carried out in a small, custom-built vacuum chamber that housed contact probes and positioning stages. Devices were illuminated with a deep ultraviolet radiation source located outside the chamber. Four initial measurements were carried out to test for (1) resistivity of the amorphous silicon, (2) photoconduction between the photocathode and anode, (3) electrical breakdown when high voltage is applied between the cathode and anode, and (4) continuity of electrode leads across the narrow channels. The first three tests were carried out on test devices located on flat surfaces, i.e. without the presence of the channels, and the last test was carried out with the channels present.

The results from the resistivity measurement yielded 31 MΩ-cm for the strip. The measured resistivity was four orders of magnitude higher than expected and reported in other work. [J. Sangrador, et al, Thin Solid Films 125 (1985) 79.] This is believed to be due to poor e-beam deposition conditions. In our deposition chamber, the base pressure was 10-5 Torr, and we expected the dynode strip to be rich in oxide. Photoconduction was readily measured between the photocathode and anode, and is graphed in Figure 9. For this measurement, the device was illuminated with a small pencil lamp, $\lambda = 253$ nm, while a +9V bias was applied to the signal collector. The graph reports the measured photocurrent from cathode to anode as a function of time. The change in photocurrent, despite constant illumination intensity, is due to surface contamination effects on the photocathode, and has been observed in similar work with gold photocathodes. [S. Gosavi et al, J. Vac. Sci. Technol. B 19 (2001) 2591.] The amount of photocurrent suggested a quantum efficiency in the 10^{-3} range for gold which agrees with previously reported values. [A. H. Sommer, *Photoemissive Materials*, John Wiley & Sons, Inc., New York, NY (1968) 33.] Measurements of breakdown voltage showed an average device failure about 500V bias, based upon testing of eight devices. This result was encouraging because sufficient device gain would be expected at such a high potential along the amplifying channels. The results from the continuity measurements showed no devices with continuous electrical leads across the narrow channels. This problem, which precluded further testing, was traced to a lithographic error at the edge of the channel regions. By augmenting fabrication procedures, this problem can be eliminated and future prototype devices can be fully demonstrated.

continued

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A secondary objective of this research program was to extend conformable-contact photolithography to other microfabrication applications. Accordingly, the technology has been successfully transferred to a California-based company that is developing a novel integrated-optical mux/demux device. This company has patterned 500-nm-pitch gratings and micron-sized waveguides, and successfully implemented multi-level alignment using CCP techniques. Mask making procedures, a critical component to CCP, were transferred to the University of Canterbury in Christchurch, New Zealand where an active research program in near-field photolithography is ongoing. Additionally, a local company has begun manufacturing conformable-contact photolithography equipment which will enable low-cost pattern replication and multi-level alignment at the sub-200-nm level.

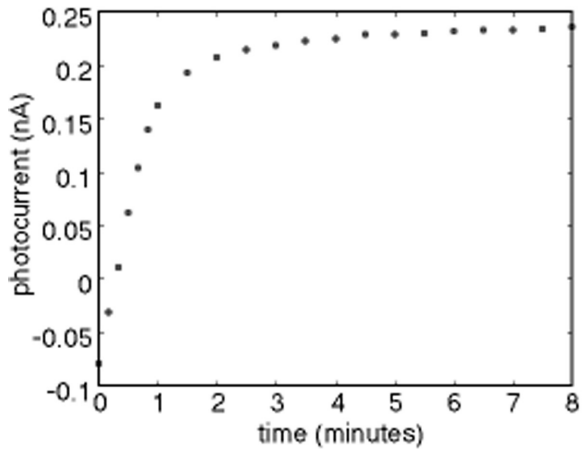


Fig. 9: The typical photocurrent measured in test devices shows an increase with time. This is due to a reduction of surface contamination at the photocathode.

Hot Filament Chemical Vapor Deposition of Polyoxymethylene as a Sacrificial Layer for Fabricating Air Gaps

Personnel

K. Chan (K. K. Gleason)

Sponsorship

MARCO Focused Research Center on Interconnect (MARCO/DARPA)

In the rapid evolution towards electronic devices with smaller feature sizes and faster speed, the factor limiting overall performance is no longer gate delay, but the Resistance-Capacitance (RC) delays due to interconnects. To reduce the capacitance part of the problem, novel low dielectric constant, κ, materials have been introduced to replace traditional silicon dioxide (κ = 4.0). Air is a "material" with the lowest dielectric constant (κ = 1.0). Air gaps can be formed by the removal of a sacrificial layer deposited in an earlier processing step. The properties of the sacrificial layer material must satisfy the following criteria: ease of synthesis and integration, thermal stability for compatibility with existing processing while having rapid decomposition at low to moderate temperatures, removal in the absence of oxygen, and negligible residue left behind after decomposition.

Polyoxymethylene, $-(CH_2O)-_n$ or POM, has great potential to be used as a sacrificial layer. POM was chosen because of its clean decomposition via an unzipping mechanism in the absence of oxygen to form its monomer formaldehyde (CH_2O) gas at less than 300˚C. Hot Filament Chemical Vapor Deposition (HFCVD) utilizes an array of heated wires to cleanly decompose the incoming precursor gas, trioxane, into lower three formaldehyde units which then react on a cooled substrate to form POM. Polymer initiation chemistry has also been used to deposit POM from trioxane with no thermal or plasma excitation of the precursor gases.

A new method for synthesizing polyoxymethylene (POM) film at high deposition rates was achieved via HFCVD and initiation chemistry. Spectroscopy shows that the structure of the deposited polymer is linear rather than cross-linked (which plasma enhanced CVD would have produced). The linear structure is critical for clean complete depolymerization. Air gaps were fabricated with lateral dimensions of 1 to 10 micron using a vapor deposited POM layer. A

continued

cross-sectional view of one such structure is shown in Figure 10. The vertical dimension of the void space, 100 nm, corresponds to the thickness of the sacrificial POM deposited. The bridge layer is 300 nm of plasma enhanced CVD silicon dioxide.

Polymethylmethacrylate (PMMA) is another candidate sacrificial material and is deposited via pulsed plasma enhanced CVD (pulsed-PECVD) and low power continuous PECVD. PECVD is the process currently used for dielectric deposition in device fabrication.

FTIR and NMR of deposited PMMA films show good agreement with bulk PMMA indicating structural similarity with the bulk polymer. PMMA undergoes a depolymerization reaction to pure monomer via thermal degradation between 280 and 320°C making it a good candidate sacrificial material. Large scale air gap structures have been fabricated using PPECVD PMMA and an organosilicate glass (OSG) overlying dielectric material and are shown in Figure 11. By using OSG, the dielectric constant of the overlayer is reduced in comparison to silicon dioxide.

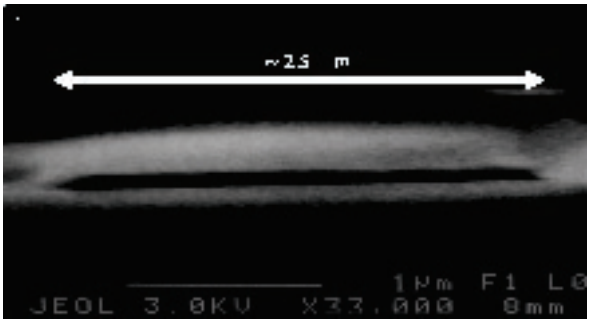


Fig. 10: Scanning electron micrograph of the cross section of air gap having lateral dimension of 2.5 micron fabricated using an HFCVD POM sacrificial layer and CVD oxide.

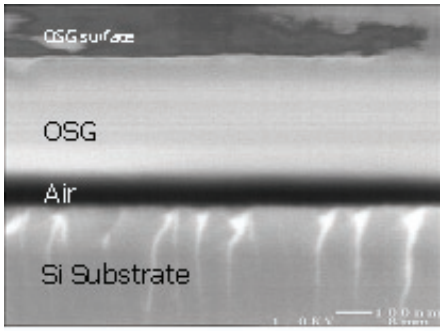


Fig. 11: ~400 nm OSG deposited over ~100nm PMMA annealed at 350°C to create void of the same ~100nm thickness.

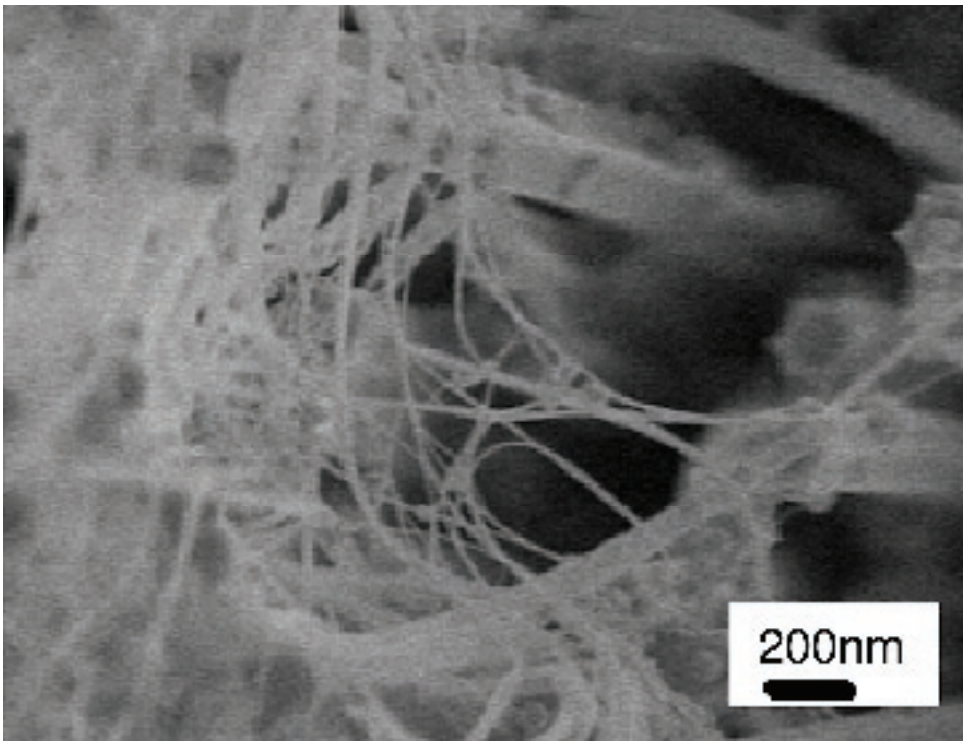
Opposite page:

Gold nano-wires (~20nm) grown by halide reduction in nano-porous alumina template. Template chemically etched to expose nano-wires.

Courtesy of R. Krishnan, R. Tadepalli, and A. Giermann (C.V. Thompson in collaboration. with K. Nielsch, C.A. Ross, and H.I. Smith).

Sponsor:
NSF and MARCO Focused Research Center on Interconnect (MARCO/DARPA)

Materials



Materials

- *Development of Processes and Technologies for Interconnects for 3D Integrated Circuits*
- *Interfacial Electromigration in Cu-Based On-Chip IC Interconnects*
- *Inelastic Deformation of Polycrystalline Films, Lines, and Dots*
- *Yellow-Green Emission for ETS-LEDs and Lasers Based on a Strained–InGaP Quantum Well Heterostructure Grown on a Transparent, Compositionally-Graded InAlGaP Buffer*
- *Ge Photodetectors for Si Microphotonics Circuits*
- *Epitaxial Growth of GaN on Silicon*
- *Integrated Materials Growth System*
- *Capillary Bonding of Nano-Structures*
- *Fabrication and Assembly of Metallic Nano-Wires, Rods, and Dots for Micro- and Nano-Systems*
- *Magnetic and Magnetooptical Films Made by Pulsed Laser Deposition*
- *Magnetic Thin Films*
- *Resonant Gas Sensors*
- *Stress Evolution During Reactive Film Formation*
- *Ferroelectrics for High Strain Actuation*
- *Stress Evolution During Volmer-Weber Growth of Thin Films*
- *Characterization of Electromigration-Induced Failure of Cu-Based IC Interconnect Trees for Circuit-Level Reliability Assessments*

Development of Processes and Technologies for Interconnects for 3D Integrated Circuits

Personnel

R. Tadepalli and R. Krishnan (L. R. Reif, S. M. Spearing, and C. V. Thompson)

Sponsorship

MARCO Focused Research Center on Interconnect (MARCO/DARPA)

The remarkable evolution of semiconductor technology has allowed production of integrated circuits with performance and functionality that have increased exponentially with time, while their cost has decreased exponentially with time. For this evolution to continue into the future, the critical dimensions in Ultra Large-Scale Integrated (ULSI) circuits must continue to shrink. As this happens, system performance will be increasingly dominated by interconnect delay. ICs laid out and fabricated in three dimensions, rather than the traditional two dimensions, can have reduced interconnect delay because of increased flexibility in system design and wiring placement and routing. The flexibility to place devices along the vertical dimension allows layout of circuits with higher device densities and reduced total interconnect lengths.

Wafer bonding is an attractive route to the fabrication of 3-D ICs. In this approach, previously processed device layers are bonded using metal-metal bonds that also serve as layer-to-layer interconnects. Evaluation of bond quality and reliability is critical to the implementation of wafer-bonded 3-D IC technology. Towards this end, we have developed techniques to measure the toughness of bonded copper interconnects. Bond toughness measurements were used to optimize the bonding process. High quality Cu-Cu bonds were fabricated at a low bonding temperature of 300 ^{0}C using a novel cleaning procedure.

A four-point bend technique has been employed to measure the toughness of Cu-Cu bonds. Cu line structures that were patterned on oxidized silicon wafers were thermo-compression-bonded in the EV501 bond chamber and then tested for bond toughness. The bonding temperature, chamber ambient, and the pre-bonding clean procedures were varied to identify the optimized bonding route.

The results from mechanical testing are summarized in Figure 1. While toughness was found to increase monotonically with increasing bonding temperature, there is an obvious dependence of bond toughness on the cleaning methods and chamber ambient. A reducing gas (5% H_2, 95% Ar) ambient improved the toughness and uniformity of Cu-Cu bonds. Best results were obtained by combining a glacial acetic acid pre-bond clean with a reducing gas chamber ambient, as is evident from the graph. A significant point of interest is that bonds created at 300 ^{0}C were comparable (17J/m^2) to industry-standard bonded SOI wafers (10J/m^2) in terms of toughness values. This favorable comparison accentuates the superior quality of bonds created at a low-k dielectric-compatible temperature of 300 ^{0}C. Poor chamber vacuum conditions limit the ability to maintain ultra-clean Cu surfaces, thereby, limiting the quality of bonds. *In-situ* cleaning procedures would, however, provide a solution to this bottleneck.

Having developed a robust technique to evaluate bond quality, we are now fabricating test structures to study bond reliability. These electrical/mechanical structures will allow us to study statistical bond toughness variations. Critical fabrication steps are: deep reactive ion etching to create through-wafer vias, electrodeposition for via filling, and CMP of Cu plated structures.

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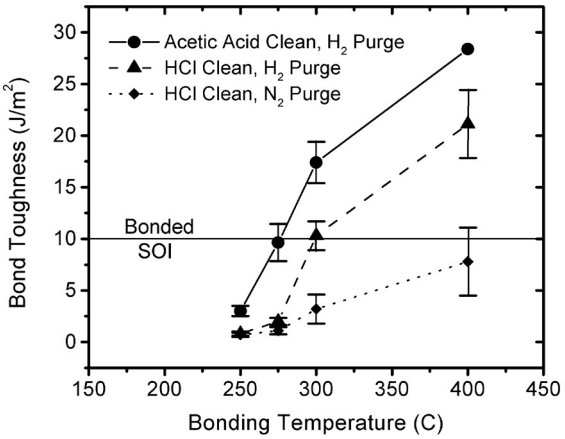

Fig. 1: Variation of bond toughness for wafers 0.4MPa thermo-compression bonded using 300nm-thick Cu films at different temperatures, after different surface preparations. Wafers bonded after an acetic acid pre-clean had higher bond toughness than bonded SOI wafers, even when bonded at temperatures below 300C. The point indicated by an '' is a lower bound.*

Interfacial Electromigration in Cu-Based On-Chip IC Interconnects

Personnel
Z. S. Choi, H. Verma, F. Wei, C. L. Gan, K. L. Pey, W. K. Choi, and R. Augur (C. V. Thompson)

Sponsorship
Intel Corp., SRC, and SMA

Electromigration in polycrystalline Al-based interconnects is known to preferentially occur along grain boundaries. This leads to a very strong dependence of the reliability of Al-based interconnects on their grain structure, with interconnects with bamboo grain structures having reliabilities orders of magnitude higher than interconnects with polygranular grain structures. The factors relating grain structures to the reliability of Al-based interconnects, and relating processing conditions to grain structures, are relatively well understood.

With the move to lower resistance Cu-based interconnects, it has become clear that the role of grain structures in determining reliability has become fundamentally different. Grain boundaries no longer provide preferred high-diffusivity paths for electromigration. Instead, the interfaces between Cu and the surrounding diffusion barriers provide higher diffusivity paths. This is a consequence of the relatively high diffusivity at these interfaces in current Cu technology, rather than due to relatively low diffusivities in Cu grain boundaries. The barrier-Cu interfaces also appear to be sites for relatively easy stress-induced void formation, and for rapid electromigration-induced void growth. It appears that the interface between Cu and the interlevel diffusion barrier (typically SiN in current technology) is an especially easy site for void nucleation and growth, as well as a path for relatively rapid electromigration.

We have developed several test structures for experimental characterization of interfacial electromigration in Cu. One structure, a 'drift structure', consists of Cu lines patterned along the length of a continuous underlying Ta line (See Figure 2). When current is passed through the Ta line, it shunts into the lower resistance Cu segments, when possible. At sufficiently high currents, this causes electromigration that leads the Cu to accumulate at the anode end of the segments and deplete at the cathode end, resulting in a 'drift' of the

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Cu segments (See Figure 2b). Measuring the current density at which drift begins, as a function of segment length, as well as the rate of drift as a function of the current density, provides important information about interfacial electromigration. We are acquiring this information from drift structures that are not covered with a passivating layer, as well as structures with passivating layers (e.g., SiN) (See Figure 2c), to investigate the effects of passivation layers on the stress required to initiate drift, as well as the drift velocity and its scaling with current density.

In a different set of experiments, we are using via-to-via test lines in a second layer of metallization, with connecting lines and pads in the first layer of metallization, to characterize drift in fully-processed dual-damascene structures provided by Sematech International. In addition to providing fully processed structures, Sematech has also provided samples that have been processed through chemical mechanical polishing of the second level of metallization. We have developed a process within MIT that allows us to complete the fabrication of test structures. This, in turn, allows us to investigate the effects of different interlevel diffusion barriers on top of the Cu test lines, as well as the effects of different surface treatments. Experiments of both types are underway.

In a related study we have characterized electromigration drift in fully processed via-to-via test structures of the type shown in Figure 3, as well as in similar structures in which the test line is in the first layer of metallization (M1). In both types of structures, we observed that in a significant fraction of the test population, the resistance of the lines increased steadily over time, prior to failure. We postulate that this gradual resistance increase results from void growth and that the rate of resistance increase correlates with the electromigration drift velocity (See Figure 4). The values of the electromigration drift velocities determined in M2 lines were similar to those measured in M1 lines, though there was a broader range of variation in the former case. The larger variation is correlated with the larger range of void shapes and sizes in M2-type structures. Given that the stress for void nucleation should be the same, the observation that the rate of void growth is the same supports our earlier proposal that the asymmetry in reliability in these two different configurations is associated with differences in the void sizes required to cause failure.

Using the interfacial electromigration test structures described above, we also plan to investigate the effects of grain structures and grain orientations on interfacial electromigration. To do this we will use Scanned Laser Annealing (SLA) of Cu lines to produce long-grained-bamboo or near-single-crystal Cu interconnects for electromigration testing. This will allow characterization of electromigration and electromigration-induced voiding for single-via and multi-via structures that contact single Cu grains or crystals.

In earlier work in our group, Scanned Laser Annealing (SLA) was developed as a means of modifying and controlling the grain structures of polycrystalline interconnects. In this technique, a laser spot is scanned along the length of an interconnect, to create a moving hot zone in which grain boundary mobilities are significantly increased over those of boundaries in unheated regions (See Figure 5). This leads to a grain growth in the hot zone, and as the zone is scanned, grain boundary motion is caused to occur preferentially and specifically in the direction of zone motion. This technique can be used to produce bamboo grain structures in lines that would not develop bamboo grain structures in conventional anneals. Furthermore, the grain sizes obtained from scanned laser annealing can be significantly longer than those obtained from conventional annealing. Lines with bamboo grain sizes as long as 10μm were produced by scanned laser annealing of 0.5μm-wide Cu lines.

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Modeling of the SLA process suggests that still longer bamboo grains can be obtained under the proper conditions. In ongoing research, we will investigate this possibility. We will also use SLA to produce large-grained structures in the dual-damascene drift structures described above. With Cu interconnects having 10μm-long grains or longer, contacted at either end with single vias, most vias will contact a single grain. By analyzing SLA grain structures before completing the processing of the electromigration test structures, we hope to assess the effect of grain crystallographic orientation on interfacial electromigration. The results will be used to develop models for interfacial electromigration in Cu interconnects that account for the effects of crystallographic orientations.

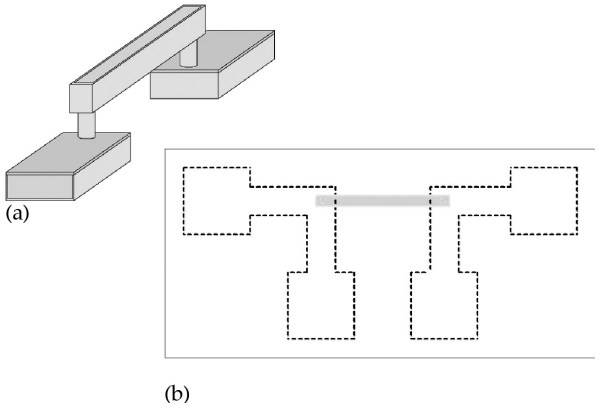

Fig. 3: A second structure for characterization of interfacial electromigration of Cu. A via-to via metal 2 test line connected to larger metal 1 lines, connected to bond pads. (a) Conventional dual-damascene processing through CMP of metal 2 is carried out at Sematech. Metal 2 surface treatment and passivation, and the rest of the test structure processing, are carried out at MIT.

Fig. 4: Void growth causes a gradual resistance increase during elec-

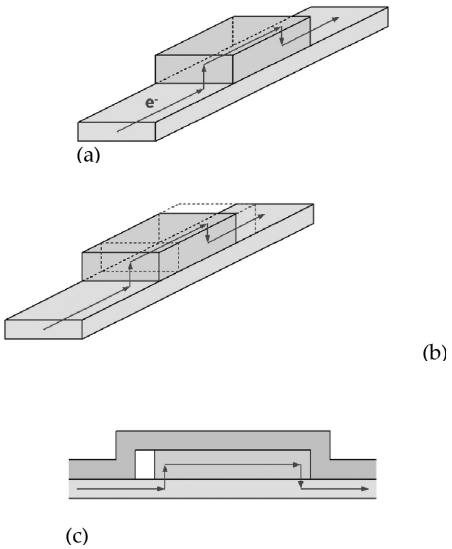

Fig. 2: Drift test structure for characterization of interfacial electromigration of Cu. (a) Cu segments are patterned on continuous Ta underlying lines. (b) Current shunts into the lower resistance Cu segment and causes it to drift. (c) Passivation will affect the rate and character of drift.

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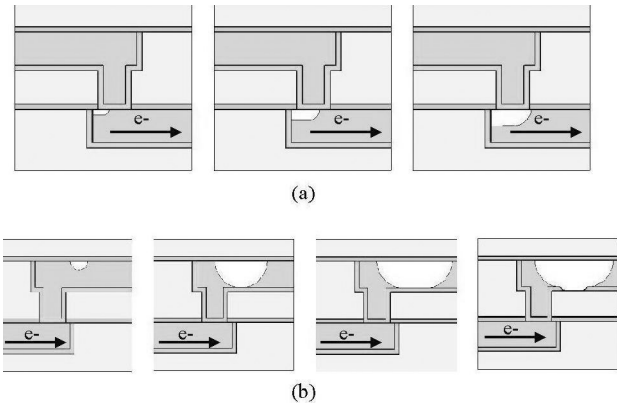

tromigration tests in (a) M1-type test structures and in (b) M2-type structures.

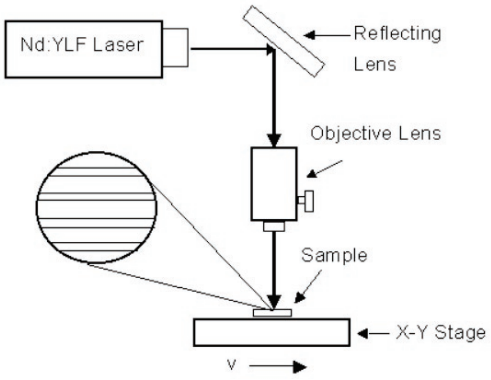

Fig. 5: An apparatus for scanned laser annealing (SLA) of Cu interconnects.

Figure 5: The grain structures that result from SLA depend on the

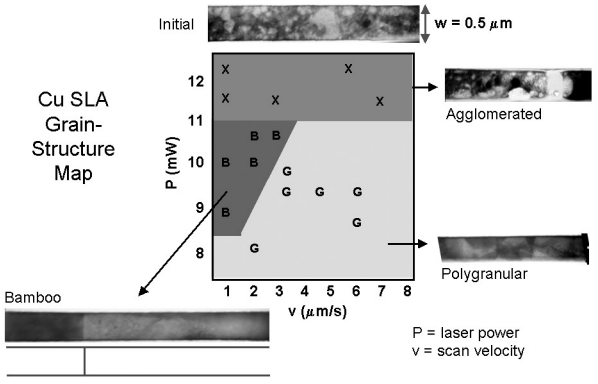

Fig. 6: The grain structures that result from SLA depend on the laser power and the scan velocity. Long-grained bamboo structures are obtained at intermediate powers and low velocities.

continued

Inelastic Deformation of Polycrystalline Films, Lines, and Dots

Personnel
R. Bernstein (C. V. Thompson)

Sponsorship
NSF and CMI

In earlier studies, we have characterized inelastic deformation of polycrystalline metallic films using *in-situ* Transmission Electron Microscopy (TEM), and *ex-situ* substrate curvature measurements during heating, cooling, and isothermal anneals. *In-situ* TEM studies were made possible through the use of micromachined silicon membranes. We have demonstrated that uncapped Ag and Cu films undergo rapid diffusional creep at temperatures as low as 0.25Tm, where Tm is the melting temperature in degrees Kelvin. At these temperatures, creep rapidly decreases with decreasing film thickness. This can lead to a decrease in the flow stress observed at room temperature as the film thickness is decreased. We have also demonstrated that dislocation-mediated plasticity dominates in capped films, or in uncapped films that are thicker or deformed at lower temperatures. We have shown that dislocation-mediated plasticity is thermally activated and controlled by pinning due to obstacles whose spacing is small compared to film thickness and grain size. This leads to the high flow stresses often observed in capped thin films. We have seen similar effects to those described above in Cu films patterned into lines through a damascene process. This work demonstrates that the inelastic properties of polycrystalline metallic films depend strongly on the film dimension, the surface condition of the film, and temperature.

We are currently investigating the use of micromachined cantilevers for isothermal studies of deformation of thin films and films patterned into dots. These cantilevers can be deflected at a set temperature, and the relaxation at that temperature can be studied. The deflection of the cantilevers can be measured with very high resolution (of order nm) using an optical profilometer at fairly high sampling rates (up to once every five seconds).

Yellow-Green Emission for ETS-LEDs and Lasers Based on a Strained–InGaP Quantum Well Heterostructure Grown on a Transparent, Compositionally-Graded InAlGaP Buffer

Personnel

L. McGill and J. Wu (E.A. Fitzgerald)

Sponsorship

NSF GOALI Program and ARO Program

Epitaxial-transparent-substrate light emitting diodes with a primary emission peak at 590nm and a secondary peak at 560nm have been fabricated in the indium aluminum gallium phosphide (InAlGaP) system. The active layer consists of an undoped, compressively strained indium gallium phosphide (InGaP) quantum well on a transparent $In_{0.22}(Al_{0.2}Ga_{0.8})_{0.78}P/\nabla_x[In_x(Al_{0.2}Ga_{0.8})_{1-x}P]/GaP$ virtual substrate. Light emitting diodes have been fabricated utilizing simple top and bottom contacts. The highest LED power of 0.18μW per facet at 20mA was observed for a quantum well composition of $In_{0.32}Ga_{0.68}P$ and a bulk threading dislocation density on the order of $7x10^6$ cm^{-2}. The spectrum of this device was composed of two peaks: a weak peak at the predicted 560nm wavelength and a stronger peak at 590nm. Based upon superspots present in electron diffraction from the quantum well region, we believe that the observed spectrum is the result of emission from ordered and disordered domains in the active region (See Figure 7). The same device structure grown with a bulk threading dislocation density on the order of $5x10^7$ cm^{-2} exhibited an identical spectral shape with a reduced power of 0.08μW per facet at 20mA. For a quantum well composition of $In_{0.37}Ga_{0.63}P$ and an overall threading dislocation density on the order of $5x10^7$ cm^{-2}, a single peak wavelength of 588nm with a power of 0.06μW per facet at 20mA was observed.

Work in the near future will focus on improving electrical characteristics and reducing the bulk threading dislocation density in the devices in order to maximize efficiency and brightness. We must suppress ordering in the quantum well in order to recover the observed 560nm emission as the peak wavelength of devices with a quantum well composition of $In_{0.32}Ga_{0.68}P$. Perhaps the fundamental factor limiting the development of high-brightness green LEDs in the InAlGaP system is the direct bandgap-to-indirect bandgap crossover problem. We believe that confinement within the quantum well active region, in conjunction with increased extraction due to the transparent substrate, will compensate for the reduction in internal efficiency expected at the compositions of interest for green LEDs, allowing for the production of a bright device. Ultimately, we hope to improve the overall material quality and design of these devices to the extent that they are a viable option both for high-brightness yellow and green LEDs and for yellow lasers.

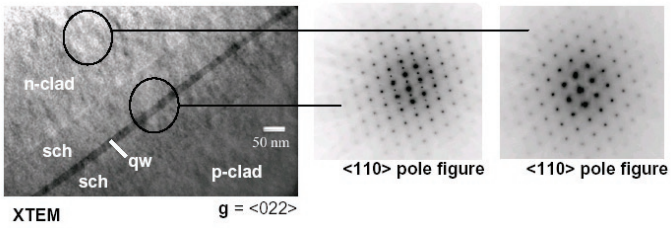

Fig. 7: X-TEM of device structure with an $In_{0.32}Ga_{0.68}P$ quantum well. Electron diffraction of the quantum well (center) shows ordering superspots, while the clad (right) does not.

continued

Ge Photodetectors for Si Microphotonics Circuits

Personnel

D. Cannon, D. T. Danielson, J. Liu, S. Jongthammanurak, A. Eshed, K. Wada, and J. Michel (L. C. Kimerling)

Sponsorship

Pirelli Labs and Analog Devices, Inc.

Epitaxially grown Ge on Si is a promising technology with significant technological applications. Because the direct bandgap of Ge is 0.8eV, it is highly absorbing at optical communications wavelengths. Because Ge is also compatible with existing Si technology, it offers the potential for high quality CMOS compatible integrated photoreceivers.

Current research is focused on increasing our fundamental understanding of epitaxial Ge growth and the influence of processing conditions on the film quality and properties. We have recently demonstrated the ability to decrease the direct transition energy of Ge films, thus extending the useful wavelength range for photoreceivers to longer wavelengths.

This transition energy reduction is achieved by increasing the biaxial strain in the film (See Figure 8). Deformation potential theory predicts a reduction in the direct transition energy of Ge with increasing biaxial strain. By varying the growth temperature, we are able to control the amount of residual strain in the films induced upon cooling to room temperature. Post growth annealing treatments are also effective in controlling strain. Our experimental results agree well with theoretical predictions.

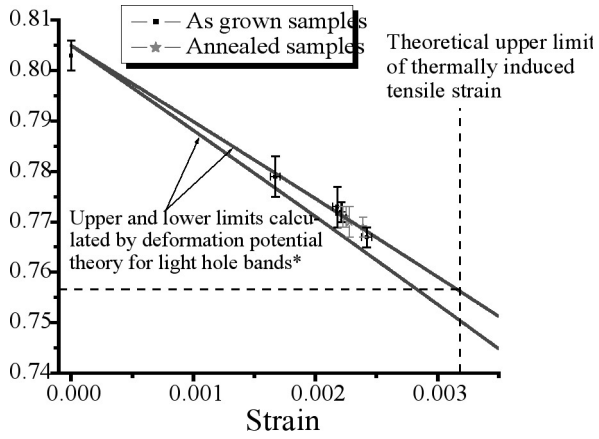

Fig. 8: Direct Ge bandgap vs. strain for several different as grown and annealed samples.

We have also demonstrated high quality selective growth of Ge mesas on Si substrates with a patterned SiO_2 layer (See Figure 9). Because Ge will not deposit from the gas phase onto SiO_2, film growth will only occur on those areas where the Si substrate is exposed. Because of the special cleaning and surface passivation procedures required for epitaxial Ge growth on Si, achieving high-quality, high-yield mesas is a significant accomplishment.

Selectively grown mesas are important, because they offer the potential for even higher quality Ge than for bulk films. Post-growth cyclic annealing of films reduces the dislocation density by two orders of magnitude in bulk films. In mesas, threading dislocations can glide to the edge of the mesa, where they leave the film. This allows for the potential of completely dislocation free mesas.

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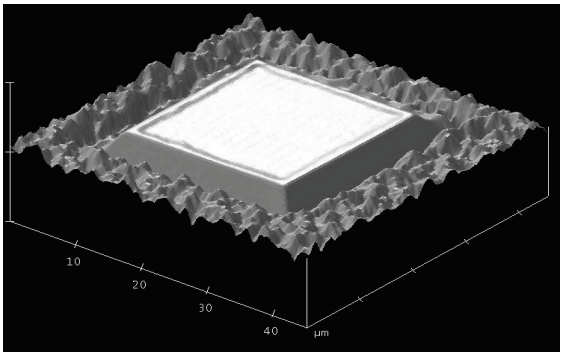

Fig. 9: AFM image of a selectively grown Ge mesa.

Epitaxial Growth of GaN on Silicon

Personnel
K. Zang and S. J. Chua (C. V. Thompson)

Sponsorship
SMA

GaN can be used for high power and high efficiency photonic devices. There is great interest in the possibility of monolithic integration of GaN and silicon for multi-chip optical communication and other applications. However, GaN and silicon have a lattice mismatch of 17%, which makes heteroepitaxial growth of low-defect-density GaN films on silicon difficult. We are investigating structure and stress evolution during the heteroepitaxial growth of GaN films on patterned silicon surfaces, and on silicon surfaces with different crystallographic orientations. We are also investigating the effects of changes in growth temperature or thermal variations during growth, as well as the use of surfactants and changes in film stoichiometry during growth. Our goal is to develop new techniques for monolithic integration of high performance GaN devices on silicon.

Integrated Materials Growth System

Personnel

S. Coe, C. Madigan, D. E. Mascaro, S. H. Kang, and J. Tischler (V. Bulovic)

Sponsorship

Defense University Research Instrumentation Program (DURIP) - Air Force Office of Scientific Research, and
NSF Center for Materials Science and Engineering SEED Grant

Vacuum growth of organic materials can generate atomically flat thin films of high purity, facilitating fabrication of complex multi-layer devices with excellent uniformity and sharp interfaces between adjacent layers. Such vacuum grown devices are highly reproducible from run to run, and can have complex structures containing thin layers of precisely controlled composition. Increased control over the growth parameter is essential for the better performance devices. Additionally, flexibility of van der Waal bonds in the organic thin films facilitate their integration with both conventional technologies and less conventional materials such as flexible, self-assembled, or conformable substrates.

We are in the process of developing a versatile materials growth system (See Figure 10) that combines conventional materials growth techniques with novel deposition methods developed in our laboratories. The completed growth system will integrate the method for physical and vapor phase deposition of hybrid organic/inorganic thin-films with a low-pressure RF/DC sputtering chamber, an evaporative growth chamber, and a chemical vapor deposition chamber. The completed vacuum system will be capable of depositing molecular organics, polymers, metals, metal oxides, inorganic nanodots, and colloids in a controlled layer-by-layer fashion. An *in-situ* shadow masking system enables fabrication of complex patterned structures inside a vacuum environment, while the integrated N_2-filled, dry glove box facilitates handling, measuring, and packaging of organic thin film samples that are susceptible to reactions with atmospheric oxygen and water vapor. When the analysis chamber is built, the completed samples will be in-situ tested by contacting them with an electrical probe attached to an X-Y-Z manipulator. Optical ports on the analysis chamber allow for a telescopic view of the devices and facilitate optical excitation of probed samples. Optoelectronic properties of the hybrid materials and structures will be investigated at a range of temperatures form 5 K to 600 K, generated by the liquid helium cryostat and the boron-nitride heater situated behind the sample stage. Existing chambers are presently connected to the central transfer system that has linear degrees of freedom. Maximum substrate size is 10 cm with a 5% variation in the thickness and composition of deposited films over the substrate area. The integrated growth system is the centerpiece of our materials growth effort, as in its completed form it will accommodate solvent-free deposition and co-deposition of polymers, colloids, and molecular organic materials in vacuum. Its versatility is unsurpassed in the field of organic/inorganic materials deposition, and it is among the first to integrate organic and inorganic material deposition methods.

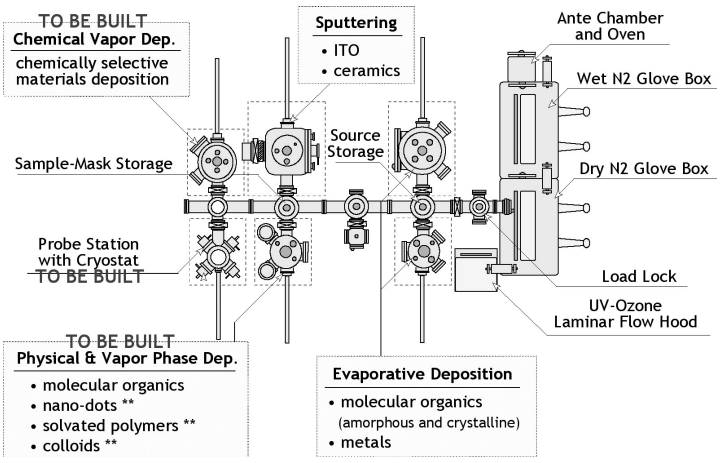

Fig. 10: Integrated Materials Growth System. Both present and projected chambers are indicated. Projected chambers and chambers in construction are labeled as "TO BE BUILT".

Capillary Bonding of Nano-Structures

Personnel

A. R. Takahashi, R. Tadepalli, S. C. Seel, N. Q. Hung, and M. Yeadon (C.V. Thompson)

Sponsorship

NSF and SMA

When small objects come into contact, capillary forces can lead to bonding that occurs at a rapid rate without atomic diffusion. Capillary bonding of curved surfaces can lead to elastic and inelastic deformation. This is most likely to occur when objects are very small (i.e., have high surface to volume ratios) because capillary forces scale with area, and the energy required for deformation scales with volume. We are studying the effects of capillary bonding through experiments on stress evolution during film formation. We are also developing both finite element models and molecular dynamics simulations of capillary bonding.

As discussed in detail in another section, during thin film formation through the Volmer-Weber mechanism, crystalline islands nucleate and grow to impinge and coalesce to form continuous films. When islands first come into contact, grain boundary formation can proceed from the point of contact (See igure 11), and leads to the reduction of the high-energy surface area of both coalescing islands. For small islands, with high surface-to-volume ratios, the energy-per-unit-volume released due to the replacement of two surfaces by one lower-energy grain boundary can be very high. The fastest way for this process to occur is for the islands to strain to close the gap between them, as the grain boundary 'zips' up from the substrate surface. The strain energy that can be accommodated is balanced by the accompanying surface energy reduction.

We have analyzed the zipping process using finite element models and molecular dynamics simulations. Finite element models have been used to calculate the strain energy as a function of zipping distance, z_0. The total energy associated with zipping (the strain energy plus the grain boundary energy, minus the energy of the replaced surfaces) is calculated and the zipping distance that minimizes the total energy is determined. The stress associated with the energy-minimizing zipping is then calculated. This allows calculation of the stress as a function of the size of the coalescing islands and leads to predicted stresses that are in better agreement with experimental observations than analytic models developed by others. Finite element analyses have been combined with simulations of island nucleation and growth to predict the average stress as a function of the mass-equivalent thickness. These calculations are quantitatively consistent with experimental observations for Ag films deposited on oxidized silicon. We have also modified finite element calculations to account for the effects of variable traction at the island-substrate interface, for different island-substrate contact angles up to 90 degrees (See Figure 12), and for coalescence of islands with different sizes.

Molecular dynamics simulations of the zipping process have also been conducted. So far, only islands bound to substrates *without* interface traction have been investigated. Islands composed of up to 5876 Ag atoms have been modeled using embedded atom potentials. Island-substrate interactions are modeled using a Leonard-Jones potential. We find that grain boundary formation occurs over time scales that are accessible through MD simulations, in that zipping occurs at very high rates. The observed zipping height is consistent with the results of finite element modeling, suggesting that the physical model on which the finite element calculations are based, grain boundary formation through island straining, is valid. Additional simulations have shown that the zipping height does indeed increase with increasing cluster size (See Figure 13), in qualitative agreement with continuum models.

We are further developing molecular dynamics simulations that will account for traction at the island-substrate interface. We also plan to conduct experiments involving in-situ Transmission Electron Microscope (TEM) observations of the early stages of polycrystalline film formation, using micromachined membranes. Through collaboration with Prof. Mark Yeadon of the

continued

Institute for Materials Research and Engineering in Singapore, we have observed deposition of Ni on both SiN membranes and on MgO substrates. More experiments are planned; as well as, more detailed analysis of the available data from earlier experiments.

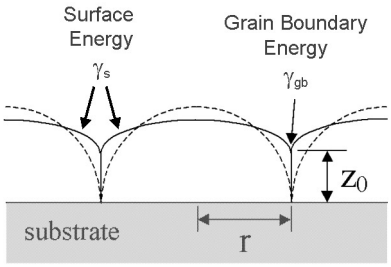

Fig. 11: When islands impinge, grain boundaries form as islands strain to close the gap between them, zipping a distance z_0 to replace two surfaces of energy γ_s with a boundary of energy γ_{gb}.

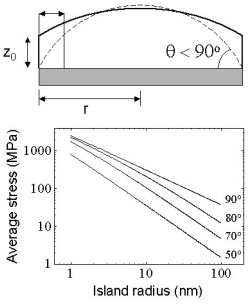

Fig. 12: Effects of the equilibrium island-substrate contact angle on the coalescence stress, as indicated by finite element analyses.

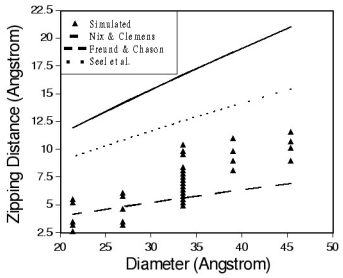

Fig. 13: Comparison of zipping height versus island size based on MD simulations, finite element simulations, and models of Nix and Clemens and Freund and Chason.

Fabrication and Assembly of Metallic Nano-Wires, Rods, and Dots for Micro- and Nano-Systems

Personnel

R. Krishnan, R. Tadepalli, and A. L. Giermann (C. V. Thompson in collaboration with C. Ross, H. I. Smith, and K. Nielsch)

Sponsorship

NSF and MARCO Focused Research Center on Interconnect (MARCO/DARPA)

Metallic nano-wires, rods, and dots can be used in a number of applications in micro- and nano-systems, such as nanowire-interconnects (wires), on-chip magnetic storage devices (rods), on-chip Peltier cooling devices (wires and rods), and plasmonic waveguides (dots). We are developing new methods for fabricating and assembling metallic nano-wires, rods, and dots, for new applications including nano-contacts for devices and interconnects for mixed-material and multifunctional micro- and nano-systems.

We have developed a new templating technique to produce metallic nano-structures on a silicon wafer. Highly ordered alumina nanopores with controlled symmetry have been grown by anodization of aluminum evaporated on lithographically-corrugated silicon surfaces (See Figure 14). We have used ordered porous alumina templates to grow nano-wires of copper and gold (See Figure 15) by electrodeposition and a halide reduction process. While nano-wire growth by electrochemical deposition has been shown previously by others, we have demonstrated for the first time the use of a novel halide reduction process to obtain metallic nano-wires. This technique can be used to obtain a wide range of materials suitable for nano-devices. Our goal is to fabricate nano-wire, rod, and dot arrays with controlled symmetry and spacing and characterize their electrical, mechanical, and thermal properties.

We are also investigating Templated Self-Assembly (TSA) as a route to fabrication of ordered arrays of nano-dots and nano-wires. Templated self-assembly is a self-assembly process on a surface patterned with conventional lithography techniques that leads to long-range periodic structures with a final characteristic length scale that is smaller than that of the initial pattern, thus overcoming the minimum size limitations of standard lithography. Our approach is to create ordered metallic nano-particles by annealing thin films at high temperatures on surfaces with artificial lithographically-defined surface topography. When a polycrystalline film is annealed at high temperatures, the grain boundaries form grooves at the surface. These grooves deepen to intercept the film/substrate interface. Once such voids form, the film proceeds to agglomerate into individual islands, resulting in a field of micro- or nano-particles. In earlier studies, we have characterized this process in films deposited on planar surfaces. We are developing methods to induce these islands to self-align during agglomeration by creating various periodic topographies on substrates. We are also investigating the use of such ordered arrays of nano-particles as catalysts for semiconductor nano-wire growth by the metal-mediated vapor-liquid-solid CVD technique.

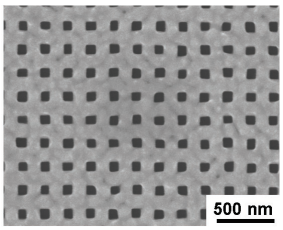

Fig. 14: Anodized alumina template on a Si wafer containing ordered nano-pores. (Pore spacing = 200nm, Pore diameter =80nm)

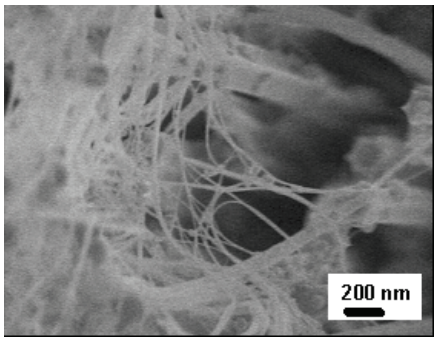

Fig. 15: Gold nano-wires (~20nm) grown by halide reduction in nano-porous alumina template. Template chemically etched to expose nano-wires.

Magnetic and Magnetooptical Films Made by Pulsed Laser Deposition

Personnel

T. Tepper, F. Ilievski, R. Ram, and G. Dionne (C. A. Ross)

Sponsorship

Pirelli and Ferry Fund

We have established a Thin Film Laboratory which includes a Pulsed Laser Deposition (PLD) system and a UHV Sputter/analysis system. In PLD, a high energy excimer laser is used to ablate a target, releasing a plume of material which deposits on a substrate to form a thin film. PLD is particularly useful for making complex materials such as oxides because it preserves the stoichiometry of the target material. We have used PLD to produce films of Cr and CoCrPt alloys to compare with films produced by sputtering, in order to understand the influence of energetic bombardment on the formation of the Cr (200) / CoCrPt (1120) preferred orientation. We have also been using PLD to deposit a variety of oxide films for magnetooptical devices such as isolators. These materials include iron oxide, which can adopt one of three different ferri- or antiferromagnetic structures depending on deposition conditions, and bismuth iron garnet (BIG, $Bi_3Fe_5O_{12}$), which is useful for magnetooptical isolators in photonic devices.

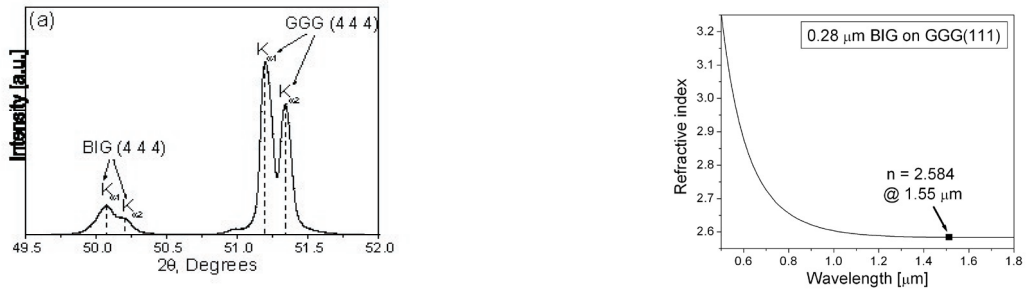

Fig. 16: Left: X-ray diffraction spectra from 300 nm thick BIG film deposited on (111) GGG (gallium gadolinium garnet) single crystal substrate, illustrating epitaxial growth. Right: Refractive index vs wavelength, measured from ellipsometry data, assuming zero absorption, for a 280 nm thick BIG film on (111)GGG.

Fig. 17: Left: XRD spectra of a 420nm maghemite (Fe_20_3) film deposited on a MgO (001) substrate, showing the cube-on-cube film-substrate epitaxial relationship. Right: Faraday rotation measurements of maghemite with different thickness at a wavelength of 645nm showing an average saturation rotation of about 1.9deg/μm.

Magnetic Thin Films

Personnel
C. A. Ross, P. Chambers, M. Shima, E. Lyons, and R. C. O'Handley

Sponsorship
NSF

Magnetic CoCrPtTa films on a Cr underlayer are used in hard disks to store data. The films are deposited at temperatures of 200˚C or above, which causes the b.c.c. Cr to grow with a (200) crystallographic texture. The hexagonal Co-alloy grows epitaxially on the Cr with a (11.0) texture, putting its c-axis parallel to the film plane. In such films, the presence of substrate roughness has significant effects on in-plane magnetic anisotropy. In particular, the presence of grooves or scratches in the substrate causes the coercivity, remanence and squareness of the film to be considerably higher parallel to the grooves compared to their values in the perpendicular direction. This effect is useful in hard disks, but the physical origin of this anisotropy is still debated.

We have measured the anisotropy in films deposited onto oxidised silicon substrates with well-controlled submicron surface topography, to explore the origins of the effect and to demonstrate how it can be enhanced by choice of substrate features. Substrates are patterned with shallow, parallel grooves, then coated with Cr/CoCrPt films. Both the stress in the films, and the preferred c-axis orientation, have been characterized. We find that magnetostrictive effects, due to the biaxial stress state of the Co-alloy films, account for about 1/4 of the measured anisotropy. The majority of the anisotropy, however, is caused by a preference for the Co c-axes to lie parallel to the grooves. This is thought to be a result of preferential nucleation of certain Co variants on the biaxially-strained Cr.

We have also been investigating the nucleation and growth of these Co and Cr films, to help understand their morphology and to control grain size for high-density media. This has been done by comparing films grown using pulsed laser deposition to those grown by sputtering under a range of conditions such as base pressure. The wide range in available processing parameters allows the importance of factors such as substrate bombardment and surface mobility to be investigated.

Another project involves the influence of strain in the magnetic anisotropy of Ni films grown epitaxially onto Cu. The lattice mismatch leads to in-plane strain which influences the anisotropy in the Ni, leading in some cases to a perpendicular anisotropy. By patterning the films into narrow lines, we are exploring how the relaxation of stress can influence the net anisotropy in the Ni nanostructures.

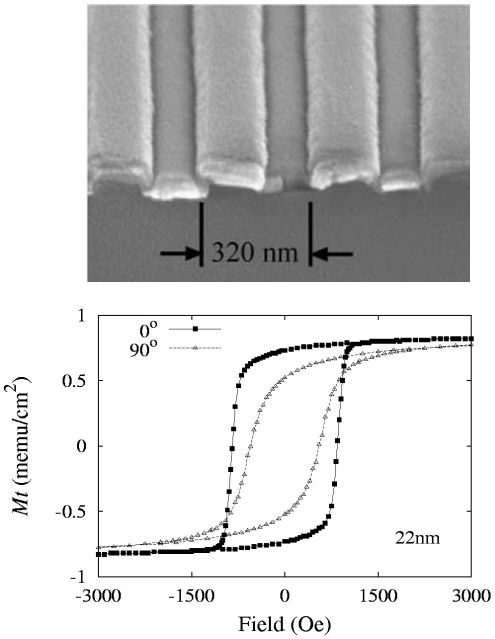

Fig. 18: Top: Example of a film sputtered over a substrate with 320 nm period grooves. Bottom: Magnetic hysteresis loops from a sample of Cr/CoCrPt sputtered onto a substrate with 200 nm period, 22 nm deep grooves. Coercivity, remanence and squareness are higher parallel to the grooves (filled symbols) compared to perpendicular to the grooves (open symbols).

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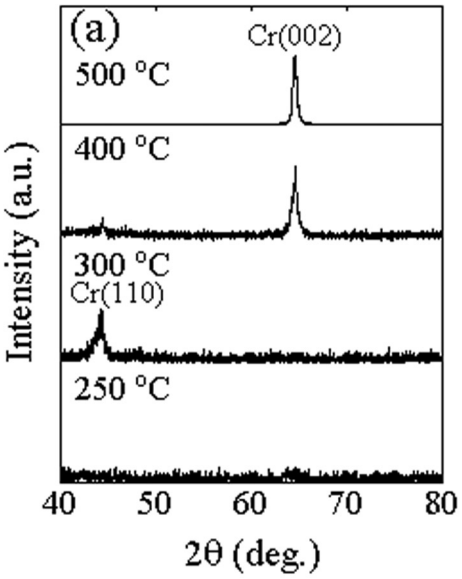

Fig. 19: Cr grown on Si by PLD. As the substrate temperature increases, the texture of the Cr changes from (110) to (200). A similar effect is seen in sputtered Cr films used in hard disks.

Resonant Gas Sensors

Personnel
H. Seh and H. Fritze (H. L. Tuller)

Sponsorship
NSF and DAAD

Langasite ($La_3Ga_5SiO_{14}$) exhibits piezoelectric properties comparable to quartz, but undergoes no phase transition below its melting temperature (1470°C), making it of interest as a potential gas sensor platform for high temperature operation. Measurements with TiO_2 films demonstrate strong sensitivity to hydrogen gas. As part of the evaluation of this material, the electrical conductivity and the electromechanical characteristics are being examined as functions of temperature and oxygen partial pressure and models are being developed which provide guidance for device optimization.

Stress Evolution During Reactive Film Formation

Personnel
K.-P. Liew, R. Bernstein, M. Yeadon, and Y. Li
(C. V. Thompson)

Sponsorship
Singapore-MIT Alliance (SMA)

Reactive film formation is widely used in the processing of micro- and nano-devices. Common examples include oxidation of silicon and formation of metal silicides through reactions between metallic films and silicon. The latter is an example of solid-state reactive film formation. During reactive film formation, the molar or atomic volume of the substrate material is significantly changed as it is incorporated into the reaction product. This volume change should lead to a large stress that would affect both the reaction rate and the stress state of the reaction product. The stress generated during reactive film formation may also affect what phase forms as a reaction product. We have studied stress evolution during reactive formation of nickel silicide films, using substrate curvature measurements. We find that the stress generated during reactions is partially relieved through mechanical relaxation, *as* the reaction proceeds. We have independently characterized the rates of stress generation and stress relaxation as a function of temperature, in order to better understand the stress conditions at the reacting interface. This allows determination of a lower bound for the instantaneous stress generated at the interface where the reaction is occurring. This was found to be 2 GPa in the case of nickel silicide formation.

Ferroelectrics for High Strain Actuation

Personnel
Y. Avrahami (H. L. Tuller)

Sponsorship
MIT Microphotonics Center

Perovskite and related oxide systems are being explored as potential candidates for high strain actuators with good thermal stability and low hysteresis and as electro-optic modulators. Several techniques are investigated for the preparation of polycrystalline, single crystalline and thin films materials. Integration into microphotonic devices is examined with emphasis on MEMS structures and electro-optic modulators. The integration of these ferroelectric films on silicon is investigated. The work is being performed in conjunction with a multidisciplinary group that is working on the integration of microphotonic devices onto silicon wafers.

Stress Evolution During Volmer-Weber Growth of Thin Films

Personnel
C. Friesen, A. R. Takahashi, and S. C. Seel (C. V. Thompson)

Sponsorship
NSF and SMA

The earliest stages of thin film formation have a profound effect on the evolution of film structures, and ultimately on the properties of films used in micro- and nano-systems. In most circumstances, epitaxial and polycrystalline (and perhaps amorphous) films grow through a Volmer-Weber mechanism, in which adsorbed atoms (adatoms) form stable clusters through a stochastic nucleation process. These clusters grow as islands on the substrate surface, eventually impinging and coalescing to form continuous films. During these processes, very high forces on the substrate can result in large residual stresses in the as-grown films. We have developed several new methods for making highly-sensitive stress measurements during Volmer-Weber growth of thin films, and used them to characterize adatom and island dynamics before, during, and after island coalescence. We are also developing simulations of adatom-substrate interactions and island coalescence processes.

We have developed several new techniques for measuring forces associated with growing films. One is a microelectromechanical device with which stresses in single crystal cantilever substrates are measured through piezoresistance measurements (described in more detail in another section). A second device allows

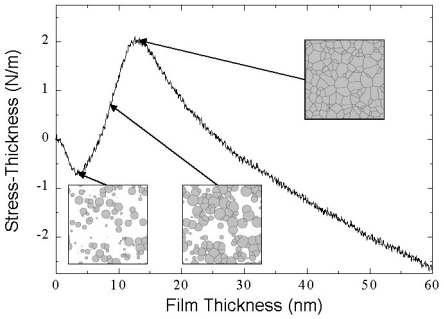

Fig. 20: Stress-thickness product measured during deposition of a Cu film. The stress is compressive as islands nucleate and grow, becomes tensile as islands coalesce, reaching a maximum when the film is continuous, and becomes compressive at higher thicknesses.

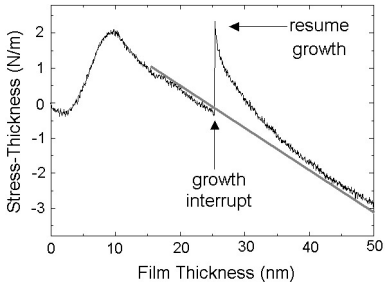

Fig. 21: Interruption of post-coalescence growth leads to a reversibly relaxed stress.

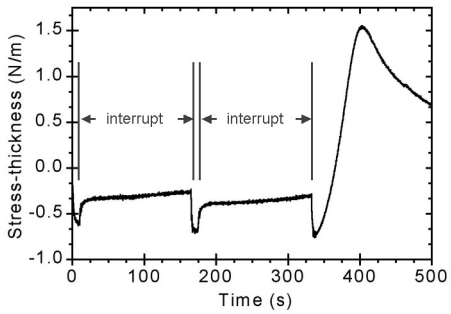

Fig. 22: Interruptions in pre-coalescence growth also leads to a reversibly relaxed stress.

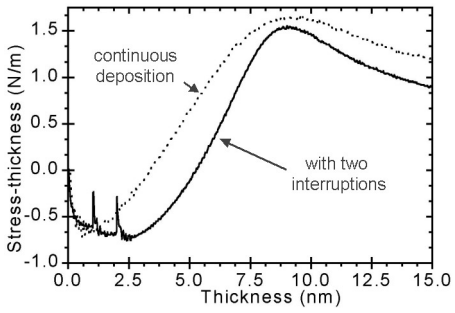

Fig. 23: The onset of coalescence occurs at a higher film thicknesses when growth is interrupted, presumably due to island coarsening during the interruptions.

continued

measurement of the deflection of the tip of a cantilever substrate by measuring the displacement of a laser beam reflected from the cantilever tip onto a diode detector pair. By placing both the laser and detectors in pressure vessels and assembling all components of this system on a rigid frame that is immersed completely in the deposition system, tip displacements of a few nanometers can be measured. The third device is also a cantilever-curvature based stress monitor and functions by measuring the changes in capacitance between the cantilever and sensor. Tip deflection can be measured with nanometer scale accuracy with this device as well. These devices have relative advantages and disadvantages, and we have used all three to study stress evolution during deposition of polycrystalline Cu films.

Figure 20 shows stress evolution observed during evaporative deposition of polycrystalline Cu films, and Figure 21 shows results for a similar deposition processes that was interrupted for 120 minutes when the film was 25nm thick. Others have reported similar behavior for Cu as well as other polycrystalline metallic films. The initial compressive stage is known to occur before significant island coalescence has occurred. The development of a tensile stress is known to correlate with island coalescence, and the peak tensile stress correlates with formation of a continuous film. In some materials and under some deposition conditions, a high tensile stress (of order GPa) develops and is retained in thicker films after deposition is complete. However in Cu, and similar materials, a compressive stress develops during further film growth.

The tensile stress that develops during island coalescence is associated with grain boundary formation and is an example of capillary bonding, which is the subject of a separate research project. The compressive stress that develops both before and after coalescence of Cu and similar materials, and the reversible stress change that occurs during growth interruptions, are less well understood.

It has been postulated that the reversibly-relaxed stress observed during post-coalescence growth interruptions (Figure 21) is associated with trapping and out-diffusion of excess atoms at grain boundaries. Using our improved ability to make very highly sensitive in-situ stress measurements, we have shown, for the first time, that there is also a reversible stress relaxation during growth interruptions in the pre-coalescence regime (Figures 22 and 23). We have also shown that the magnitude of the reversibly relaxed stress in both the pre-coalescence and post-coalescence regimes scales with the atomic flux prior to the interruption, and that the initial rate at which the stress during deposition increases is extremely high, corresponding to stress change rates of order GPa per monolayer. These results have lead us to postulate that the reversible stress change observed during growth interruptions is the result of changes from a high steady state adatom concentration during deposition, to a lower equilibrium concentration attained during interruptions in growth. The reversible stress then gives a measure of excess adatom concentration during growth. This interpretation is consistent with calculations of the effects of individual adatoms on surface stress, as determined through molecular dynamics simulations with embedded atom potentials. Calculations based on ab-intio simulations are under development.

High-sensitivity *in-situ* stress measurements during film formation provide a powerful tool for real time characterization of the dynamics of adatom populations, and during growth interruptions of adatom diffusion and island coarsening. They also provide quantitative tools for analysis of stress evolution during film coalescence and during post-coalescence structures evolution. The use of these tools will lead to better understandings and control of the film formation processes that so strongly affect film properties and performance in micro- and nano-systems.

Characterization of Electromigration-Induced Failure of Cu-Based IC Interconnect Trees, for Circuit-Level Reliability Assessments

Personnel

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Sponsorship

SRC and SMA

Delay associated with over a kilometer of metallic interconnections in a single high-performance integrated circuit now limits the overall circuit speed. The delay associated with interconnects is due to parasitic capacitances that can be reduced by reducing the resistivity of the metal (until recently, Al) and by decreasing the dielectric constant of the material between interconnects (currently SiO_2). Because Cu has lower resistance than Al, this has driven the development of new Cu-based IC interconnection technologies. The major limitation on the reliability of interconnects is associated with electromigration-induced failure. Electromigration is a current-induced diffusion, and it results in interconnect failure when it causes the formation of voids or extrusions. Cu is expected to have intrinsically lower rates of electromigration. However, aspects of the technology changes associated with the introduction of Cu lead to new reliability issues. To accurately assess the reliability of circuits made using Cu-based interconnections, it is necessary to understand the effects of electromigration on the reliability of the collections of complexly connected interconnect segments, known as interconnect trees. Toward this goal we are investigating the reliability of both standard two-terminal test structures as well as more complex multi-terminal test structures.

The standard electromigration test structure consists of a straight line of uniform width, that terminates at vias at either end and has no other terminals. We refer to these as 'i' structures (see Figure 24). The simplest interconnect tree is a straight line with vias at either end as well as a terminal in between, so that the line is broken into two segments that can carry different currents. We call these structures "dotted-i" structures. Width changes in a line can also lead to a change in current density, so that an "i" structure with a width transition can also be considered to be a simple tree. Other simple trees are 'T' and '+' structures. Test chips with all of these structures have been fabricated for us by the Institute for Microelectronics (IME) in Singapore and International Sematech Inc. in the U.S. In the last two years we have carried out experiments on 'i' structures in the first layer of metallization (M1) as well as in the second layer (M2). We have also carried out experiments on symmetric and asymmetric dotted-i and T structures, as well as width-transition and "+" structures. Testing was carried out in collaboration with IME, Sandia National Laboratory, Intel, and Advance Micro Devices.

Highlights of results found so far include:

- M2 'i' structures have consistently higher lifetimes than M1 'i' structures. This is thought to be due to differences in the locations of void formation, and corresponding differences in the time required for voids to grow large enough to cause failure.
- Short M1 and M2 'i' structures have increased median lifetimes below a critical current density line-length product (jL). This critical jL product is larger for M2 lines than for M1 lines.
- The median lifetimes of long M1 and M2 'i' structures increases with increasing line length. This is thought to be due to liner rupture at one or both of the terminating vias, resulting in Cu flow from the lead lines and into the lead lines, so that the lead lines act as reservoirs and sinks for Cu.
- The lifetime of a segment of a dotted-i structure is very strongly dependent on the current density in the linked segment (Figure 25), indicating that reliability analyses must be tree-based rather than segment-based (as they commonly are now).
- The lifetime in a segment in a dotted-i can be increased if the linked segment is unstressed or if it is stressed so as to replace electromigrating Cu.

continued

continued

- The segment that fails first is not always the most highly stressed segment, and can in some cases be an unstressed linked segment.
- Trends are similar in dotted-i and T structures.
- The reliability of the central via in dotted-i, T and + structures with the same segment characteristics, with the central via acting as the cathode for all segments, is very similar.

To better and more quantitatively understand the implications of these studies, we are developing a new tool for simulation of electromigration and electromigration-induced damage in Cu-based interconnects. This tool tracks stress evolution that results from current -induced atomic transport, and allows for void nucleation, growth, and drift. The new tool is based on the same basic model as an earlier tool developed for assessment of the reliability of Al-based interconnects (EmSim), but is faster and more stable solution algorithm. The new code also addresses issues that are especially important in Cu, including the effects of voids that only partially span a line. This work is being carried out in collaboration with Prof. Jacob White.

All of the experimental results cited above were obtained for Cu interconnects with SiO_2 as the embedding dielectric. In the coming year we plan to carry out comparative studies on Cu interconnects embedded in low-k dielectrics. Some of these low-k dielectrics also have lower elastic moduli, and may flow inelastically under test conditions. These properties can profoundly affect the measured lifetimes as well as their interpretation for use in assessing reliability at service conditions. In anticipation of these issues, we have begun to study the mechanical properties of the Cu/low-k materials systems, using, among other tools, nano-indentation. This work is being carried out in collaboration with Professor Olowolafe.

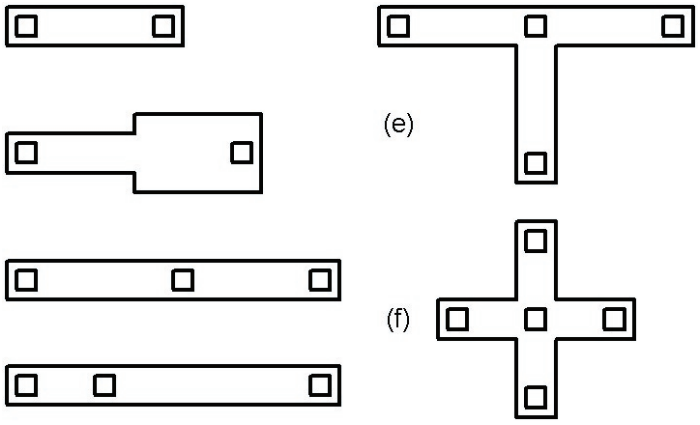

Fig. 24: Test structures used for development of circuit-level reliability assessment methodologies for Cu based interconnects: (a) 'i' structure with 2 terminals, (b) 'i' structure with a width transition, (c) symmetric 'dotted-i' structure with 3 terminals, (d) asymmetric 'dotted-i' structure, (e) 'T' structure with 4 terminals, and (e) '+' structure with 5 terminals.

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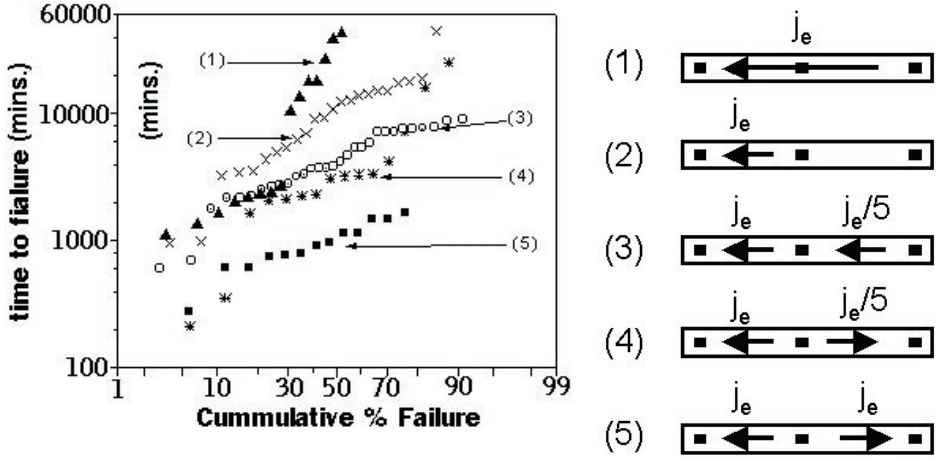

Fig. 25: Failure times (right) for 3-terminal Cu interconnects tested under different current configurations (left).

Opposite page:

A schematic of the MIT 3D photonic crystal.

Courtesy of M. Qi, J.Joannopoulos and H. I. Smith

Sponsor:
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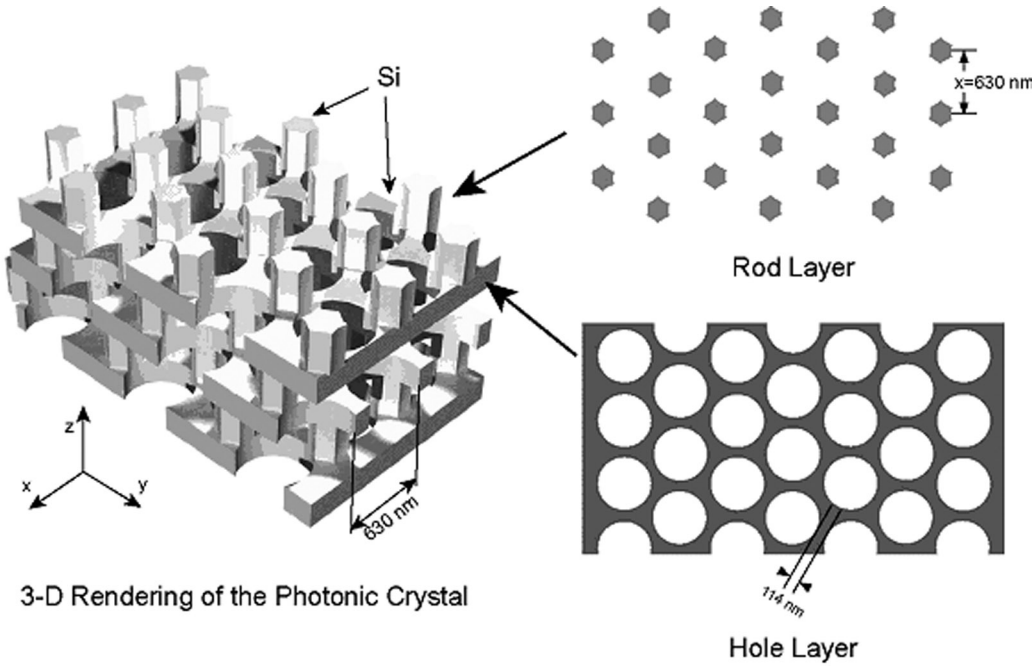
Optoelectronics



Optoelectronics

- *Fabrication of H-tree Waveguide Structures for Optical Clock Signal Distribution*
- *Erbium-Doped Waveguide Amplifiers*
- *Silicon Photonic Band Gap, Microcavity and Waveguide Structures*
- *Silicon Waveguide Structures*
- *Planarization of Processed Si IC Wafers for Planar Optical Waveguide Formation*
- *Waveguide Materials for Microphotonics*
- *Strain-tunable Photonic Band Gap Microcavity Waveguides at 1.55 μm*
- *Enhanced Extraction from a Light-Emitting Diode Modified by a Photonic Crystal and Lasing Action*
- *Fabrication of 3-D Photonic Bandgap Structures*
- *Guiding Light Through Sharp Bends Using Two Dimensional Photonic Crystals*
- *GaAs Superprism Using Two-Dimensional Photonic Crystals for Enhanced Beam Steering*
- *Application of RM^3 Integration to Optical Clock Distribution on Si-CMOS*
- *Aligned Pillar Bonding Technology for RM^3 Integration*
- *Optimization of Cells for Microscale Themophotovoltaic Energy Conversion*
- *Recess Mounting with Monolithic Metallization (RM^3) Polylithic Integration Technology*
- *Magnetically-Assisted Statistical Assembly*
- *Large Scale Oxidation of AlAs Layers for Broadband Saturable Bragg Reflectors*
- *Variable Amplitude Optical Fourier Filtering Using Controlled Thickness Metal Structures*
- *Towards Optical Logic*
- *Design and Variation Analysis of an On-Chip Optical Clock Receiver Circuit*
- *Optical Nano-Electromechanics*
- *Optoelectronic Integrated Circuits for Diffuse Optical Tomography*
- *Investigation of Dark Line Defects in Semiconductor Laser Diodes*
- *Compact Optoelectronic Neural Co-processor Project*
- *Terahertz Quantum Cascade Lasers*
- *Development of Bipolar Cascade Lasers*
- *Design and Fabrication of a Superprism Using Two Dimensional Photonic Crystals*
- *Coupling into Photonic Crystal Waveguides*
- *Development of Birefringence-Free Ridge Waveguides for Waveguide Isolators*

Fabrication of H-tree Waveguide Structures for Optical Clock Signal Distribution

Personnel
D. Ahn, J. Michel, K.Wada, and L. C. Kimerling

Sponsorship
MARCO/DARPA Focused Research Center on Interconnect

Electrical interconnects are the current platform for clock signal distribution across a chip, which governs the internal operations of a microprocessor in a synchronous chip design. However, the continuous enhancement of electrical clocking speed is expected to face severe limitations in the near future. Electrical clocking will have difficulties arising from jitter and skew of the signal and increased power consumption, as the clocking frequency is increased.

A solution to overcome this barrier is optical clock signal distribution. Using photons instead of electrons can help reduce skew and jitter of clocking and therefore enables the increase of the clock signal frequency well above 10 GHz, while keeping the power consumption and heat generation low. We fabricated waveguides for H-tree structures that split and distribute the source optical signal across the chip, while keeping the waveguide interconnect length identical.

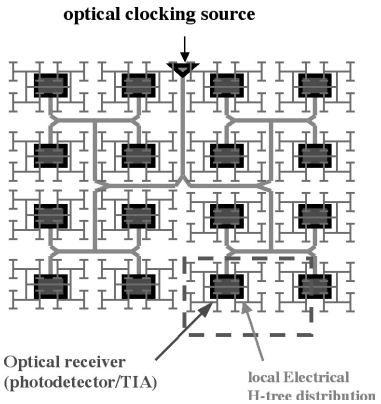


Fig. 1: Schematic of optical clocking and H-tree waveguide structure

We used SiO_xN_y and SiO_2 as waveguide core and cladding material, respectively. SiO_xN_y has the benefit of good compatibility with Si CMOS processing and gives the flexibility to adjust the refractive index within the range of 1.45-2.0 by changing the composition ratio of nitrogen and oxygen.

Using 850nm wavelength and designing waveguide dimensions such that it retains only one single optical mode, we fabricated 1x4, 1x16, and 1x 64 fan-out H-tree structures. They have bending radii of 800μm, 250μm, and 120μm, respectively. All waveguides successfully distributed optical signals to each leaf node passing through all splitting and bending stages. Optical loss in the waveguide was measured to be about 2dB/cm.

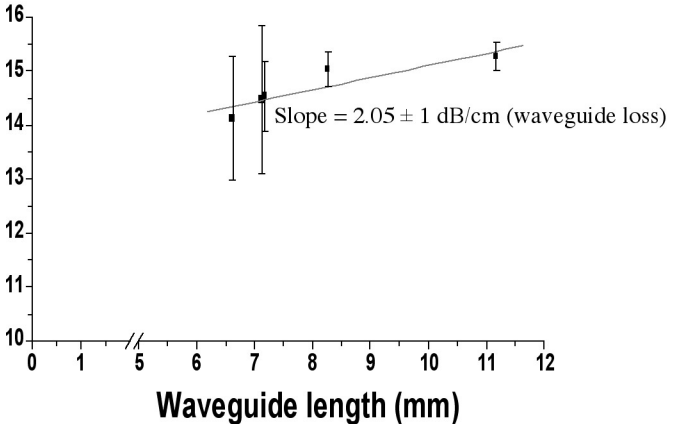


Fig. 2: Waveguide loss for 1.5μm 1.5μm PECVD-deposited SiON waveguide (Δn=0.05, unannealed)

One of the key requirements is equal power distribution at the 3 dB splitters. Conventional Y-splitters can exhibit high losses at the split fork due to limitations in lithography. These splitters are therefore susceptible to unequal splitting of the optical energy. By developing a new splitter design, we significantly reduced splitter loss and achieved more even splitting of optical energy.

Erbium-Doped Waveguide Amplifiers

Personnel
S. Saini, X. Duan, and J. Michel (L. C. Kimerling)

Sponsorship
CMSE and NSF

Erbium ion-based optical amplification has been a technological enabler in the establishment of long distance telecommunication at λ=1.55 μm wavelength light. The current evolution of telecommunication systems is to higher information capacity (by means of wavelength-division multiplexing) and to lower cost planar waveguide components (creating a new economy-of-scale technology). To meet both these demands, our research is focused on meeting two key amplification goals, using the broadband Er atom in glass hosts: (i) to take advantage of index scaling effects to reduce the required optical pump power for gain amplification, and (ii) to dope the highest possible concentration of optically active Er within a waveguide amplifier. These two goals are synthesized into a critical performance figure of merit, called the device gain efficiency.

Figure 3 is a theoretically computed plot summarizing our studies of goal (i): the effect of waveguide core-cladding index difference Δn on amplifier gain. Traditional Er-doped fiber amplifiers operate at index differences of Δn=0.05; design of a waveguide amplifier with Δn=1.0 results in an 80× increase of device gain efficiency. This means 80× less pump power shall be required for the Δn=1.0 waveguide amplifier, to achieve the same gain per unit length, as the fiber amplifier.

This stunning performance scaling advantage occurs because for different Δn waveguides, core dimensions just below single mode cut-off result in 64% of the λ=1.55 μm light being confined to the Er-doped core. From a confinement perspective, the two waveguides are morphologically equivalent for both pump and signal wavelengths. But for the higher Δn single mode cut-off waveguide, this confinement of the waveguiding modal fraction is within a smaller core cross-section. As a result, the optical flux rate (photons/cm^2) increases, and Er atoms within the core are pumped at a higher excitation rate.

Figure 4 is an experimentally acquired plot summarizing our studies of goal (ii): the exploration of new Er-based materials systems that yield ultra-high concentrations of optically active Er atoms. To evaluate the ultimate high-concentration candidate, we performed PhotoLuminescence (PL) studies on erbium oxide Er_2O_3, a ceramic-class material with ~10^{22} Er/cm^3 density. Studies from room temperature down to 4.2 K were done in order to isolate the effect of phonon-assisted non-radiative de-excitation. A factor of 60× drop in PL peak was observed from 4.2 K up to room temperature. In addition, the spectra shape was observed to profoundly change between 4.2 K and 20 K, indicating the presence of competing light-emitting Er optical centers, whose emission is intimately related to non-radiative processes. Comparison of integrated 4.2 K PL and room temperature absorption intensities of this sample, versus a standard Er-doped SiO_2 glass sample, allowed us to conclude that the 4.2 K main PL peak is associated with a minority volume phase, making up ~3% of the ceramic. Correlation with X-ray diffraction and Transmission Electron Microscopy has helped identify this minority phase to be a metastable FCC phase. If this phase can be made into the majority phase, gain coefficients 10× better than the best current fiber amplifier may be realized, for nearly the same device gain efficiency. Studies are underway to increase volumetric yield of this FCC phase.

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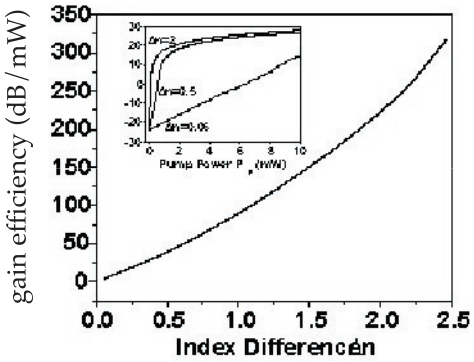

Fig. 3: Device gain efficiency versus index difference Δn for a 1 m long waveguide amplifier with 10^{20} Er/cm^3 optically active. Inset: plot of device gain γ_d vs. optical pump power P_p shows an increasing slope with higher Δn. The slope of this plot gives the device gain efficiency.

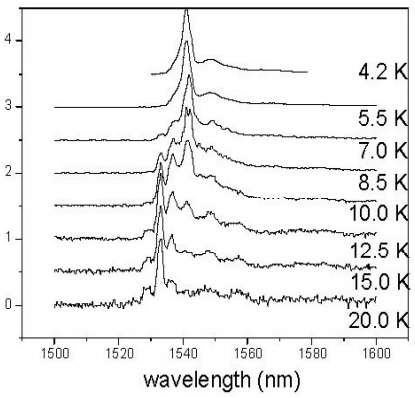

Fig. 4: Low temperature photoluminescence study of Er_2O_3. Observations indicate the presence of three optical light-emitting centers, correlated by X-ray diffraction with the formation of three crystal phases.

Silicon Photonic Band Gap, Microcavity and Waveguide Structures

Personnel

Y. Yi, S. Saini, M. Lipson, X. Duan, and K. Wada
(L. C. Kimerling)

Sponsorship

NSF and MRSEC

Tunable photonic crystals are key devices for microphotonics, especially for future WDM applications. Since the first introduction of Photonic Band Gap structures (PBG), also known as photonic crystals, new concepts and designs are being proposed, which could be building blocks for next generation photonic integrated circuits. When defects are formed within PBG materials, localized state can be introduced where light is strongly confined around the defect. The confinement of light to small volumes on the order of a wavelength will lead to large reduction of photonic circuit size and numerous useful devices, especially for Si microphotonics. Realization of the tunability of the photonic crystal, which makes it an active component, will play a key role for switching, modulation and wavelength conversion. This project is in collaboration with Profs. Joannopoulos, Ippen, Haus, Kolodziejski, and Smith.

Here, we demonstrate a tunable one-dimensional photonic crystal with a large air defect in silicon based PBG materials. Multiple localized resonance modes are observed within the photonic band gap at 1.402 μm, 1.582 μm, 1.792μm and 2.072μm. The observed photonic band gap is from 1.19μm to 2.18μm, which has 1000nm bandwidth. The Free Spectral Range (FSR) is larger than 100nm. Employing an electrostatic force, low voltage tuning of the localized modes are achieved simultaneously around the two telecom wavelengths of 1.3 μm and 1.55 μm. At 10V, an almost 60 nm mode shift is achieved. This is the lowest as we know so far.

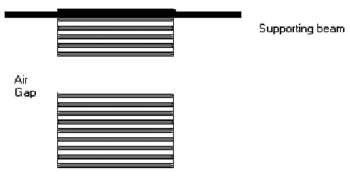

Fig. 5: The illustration of the one-dimensional photonic crystal with a large air defect.

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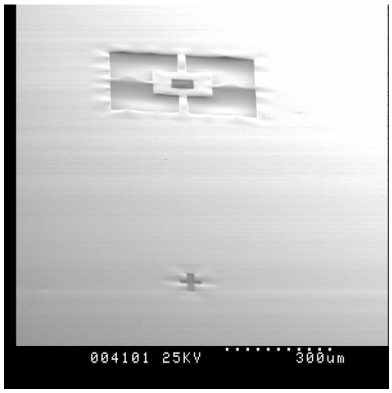

Fig. 6. SEM picture of the one-dimensional photonic crystal with a large air defect.

While fabrication of 3D photonic crystals by CMOS compatible process as is still challenging, the 1D omnidirectional PBG is easily incorporated into a CMOS process, while retaining important features of 3D PBG structures. Tunability can also be realized. Here we utilize the Micro-Electro-Mechanical-System (MEMS) method to realize low voltage tuning of the 1D PBG structure with large air defects. The top Si/SiO_2 mirror a membrane suspended by supporting beams over an airgap (cavity) and bottom mirror (see Figure 6). Applying a voltage between the membrane and substrate can tune the cavity thickness, i.e, can shift the multiple resonance modes within the PBG. Here, we emphasize that the low voltage can be used to tune a large wavelength. We concentrate on the windows from 1.2 μm to 1.7 μm. We plot the wavelength shift vs. voltage square in Figures 7 and 8 around 1.402 μm and 1.582 μm which are close to the two telecom wavelengths of 1.3 and 1.55 μm. The near-perfect linear relationship between the wavelength shift and voltage square confirms the electro-static tuning of the localized modes. We notice that, at 1.582 μm resonance, an almost 60 nm shift is realized with up to 10 volts. This is the lowest shift we have observed. Switching and modulation mechanism can be realized with such a shift.

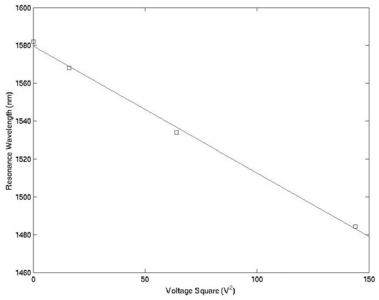

Fig. 7 The resonance wavelength shift with voltage square at 1.582μm.

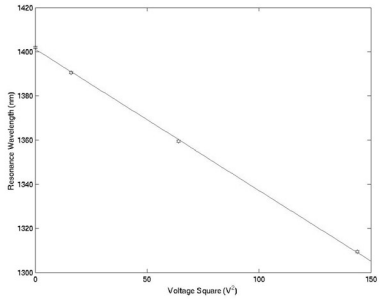

Fig. 8: The resonance wavelength shift with voltage square at 1.402μm.

Figures 7 and 8 indicate the possibility of continuous tuning from 1.3 to 1.5 μm by applying higher voltages, using flexible beams or a larger defect cavity. This is because the discrepancy between two tunable wavelength bands is only 60 nm. Figure 9 shows the first continuous tuning using a single defect in a microcavity in terms of electrostatic force. The voltage swing is up to 20 V, which covers a 1000 nm tuning range. This is the first demonstration of such wide range tuneability by a single filter.

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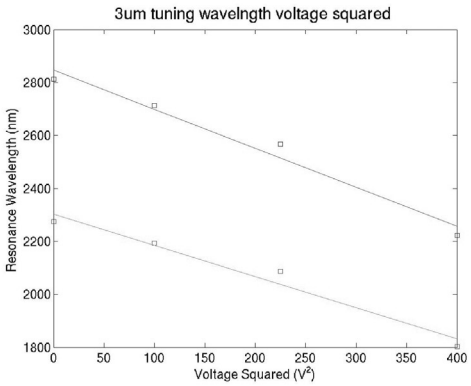

Fig. 9: First demonstration of an optical filter with a continuous tuning wavelength range of 2 μm.

This presented one-dimensional PBG filter with large air defect will be of importance in various applications other than data and telecom, such as solid state sensors of chemical substances.

Silicon Waveguide Structures

Personnel

D. Sparacin and K. Wada (L. C. Kimerling)

Sponsorship

NSF and MRSEC

The Si-SiO_2 materials system is an ideal platform for microphotonics because of the large index contrast between core and cladding, and the semiconductor characteristics of Si allowing carrier injection for ultra fast index change. Despite these attractive properties, the Si-SiO_2 system has a tradeoff associated with device processing: surface roughness. Waveguide surface roughness causes light scattering, resulting in transmission loss. This phenomenon scales with Δn^{2-3} and is crippling for high Δn photonic systems. Thus, surface roughness is a barrier for realizing silicon photonic devices.

Silicon On Insulator (SOI) wafers, with a 0.2 μm top Si layer and 1 μm SiO_2 layer, were patterned with a G-line (x=436nm) 10X stepper. RIE with SF_6 was used to etch the silicon waveguides, defined by photoresist, above the SiO_2. All samples were taken from the same wafer to ensure uniformity in the experiment. Dry oxidation of waveguide samples was performed for 30, 60, and 120 minutes at 1050ºC. Buffered Oxide Etch (BOE) was used to remove the oxide for roughness measurement.

A Digital Instruments NanoscopeIIIa Atomic Force Microscope (AFM) was used to measure the roughness of the waveguides. Measurement scans (3 X 3 μm^2) were performed parallel to the direction of the waveguides using the tapping mode. This was necessary for distinguishing between waveguide roughness and errors between adjacent scans. The problem seems to be provoked when measuring on a surface with a large slope, such as the sidewall of a waveguide. Another point to note is that unlike planar surfaces, which are scanned with the end of the AFM tip, the side of the tip is used when measuring sidewalls, diminishing the feature size resolution that can be obtained. The lessened resolution results in a smoothing of the surface in terms of amplitude height. Thus the values obtained in our measurements are understated. Roughness measurements were averaged over the entire waveguide

continued

continued

sidewall area. Care was taken to measure all samples with the same tip orientation. TSUPREME4, a simulation program for CMOS design, was used to model the oxidation smoothing of the waveguides. In our simulation, an SOI substrate was created with a chosen surface roughness containing one frequency and amplitude. Trapezoidal cut outs in the silicon surface were used to simulate the roughness. This approximation only affects the short-term oxidation behavior, since the high surface energy corners of the trapezoids are oxidized fastest, leaving an ideal sinusoidal profile after only a few minutes of oxidation. The simulated roughness underwent dry oxidation at 1050°C and roughness amplitude was recorded as a function of time.

Surface roughness, when created by dry etching processes, exhibits a distribution of spatial periods. In our study, roughness profiles obtained from AFM were processed using the Digital Instruments Nanoscope Software. The reduction of surface roughness is clear, when viewing the AFM images as oxidation time, increases. As seen in Figure 10, the as-fabricated waveguide surface contains mostly short period roughness, but as oxidation time is increased, the surface roughness period increases. This is expected since short period roughness is associated with a higher surface energy than long period roughness. Therefore, as oxidation time increases, the shorter period roughness is diminished more rapidly than the longer period roughness.

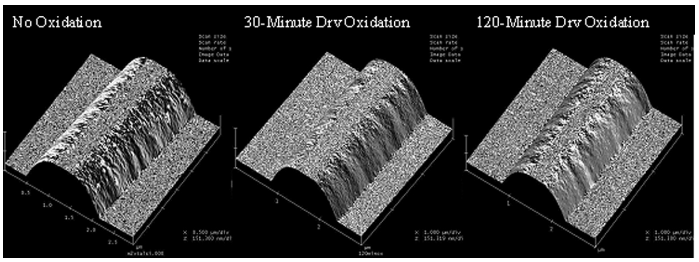

Fig. 10.: AFM images of silicon waveguides, the left image is as-fabricated whereas the center and right waveguides have undergone 30 and 120 minutes of dry oxidation and subsequent oxide etch respectively.

A quantitative measurement of this roughness is contained in Figure 11. There are three things to note about this plot. First, the roughness amplitude increases with period. The origin of this roughness distribution is thought to be associated with the grain size of the photoresist film under our baking conditions. Second, the shorter period roughness diminishes faster, relative to its respective initial amplitude, than the long period roughness. This is expected given our surface energy arguments stated earlier. Third, there appears to be "saturation" in the roughness profile. This is evident when comparing the 60-minute and 120-minute curves. Roughness saturation indicates that there is a practical limit in reducing propagation loss in Si waveguides. A waveguide designed for 1550 nm light is particularly sensitive to roughness periods around 125 nm ($\lambda/4n_{eff}$). TSUPREME4 simulations indicate that saturation should not occur, and roughness amplitude should continuously decrease to a perfectly smooth surface. While TSUPREME4 treats materials as a continuum of matter and neglects discrete atoms, this explanation does not contribute to why saturation occurs.

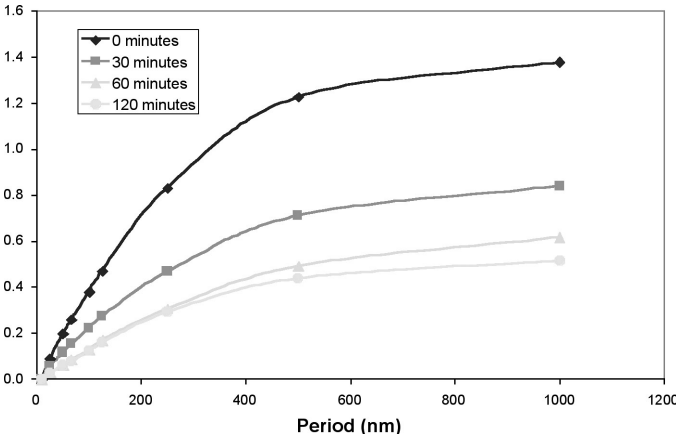

Fig. 11: Plot of waveguide roughness amplitude versus roughness period for different oxidation times.

continued

One explanation for the discrepancy between the observation and simulation is the error in comparing a surface roughness with a single amplitude and period to a distribution of amplitudes and periods. When a single roughness amplitude and frequency is simulated, the roughness period does not change. To see if this is always the case, a roughness with two sets of roughness was simulated. The shorter period of the bimodal roughness was given a smaller amplitude, to imitate the experimentally found roughness distribution. When the bimodal roughness distribution was simulated, the longer period roughness dominated and the shorter period roughness was absorbed as it was oxidized. The overall result, as seen in Figure 12, is a roughness with a smaller amplitude but longer period. This is an important kinetic phenomenon to note, for it lengthens the oxidation time needed to minimize the amplitude of a specific spatial period, such as the highly attenuating quarter wavelength period. This behavior can be likened to Oswald Ripening in grain growth, in which larger grains grow at the expense of smaller grains, but with respect to spatial period rather than grain size.

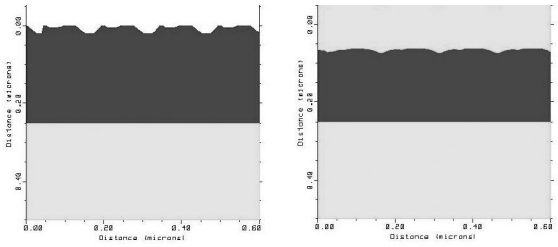

Fig. 12: Simulation images of a surface roughness profile, with a bimodal roughness distribution, before and after oxidation.

The bimodal simulation suggests that the roughness distribution in Figure 11 should shift to the right as oxidation time increases. This qualitatively explains the saturation, but cannot explain the presence of roughness near the origin after long oxidation times. A possible explanation for this is the nucleation of roughness by oxidation. The phenomenon of roughening by oxidizing {111} silicon has been observed by other studies. Likewise, the waveguide sidewalls in this study are very close to the {111}. Thus we suggest that oxidation of the {111} silicon waveguide sidewalls creates short period roughness that is absorbed by larger period roughness. This in turn feeds into the roughness distribution, eventually creating a "steady state" roughness distribution. In essence, there is a competition between roughness minimization and creation by oxidation of silicon waveguides. This "steady state" roughness distribution leads one to wonder whether there is a limit on propagation loss reduction of Si waveguides by oxidation. Further studies into oxidation smoothing kinetics are needed to better understand this.

In this study, we examined the oxidation kinetics of silicon waveguide roughness minimization. As anticipated we found that small period roughness is reduced faster than long period roughness. Unexpectedly, we also observed saturation in oxidation smoothing, which is problematic because it increases the needed oxidation time for minimizing roughness and prevents the possibility of atomically smooth silicon waveguides. We suggest that oxidation smoothing saturation is due to a competition between long period absorption of short period roughness and the nucleation of short period roughness by oxidation of the {111} silicon waveguide sidewall surface.

Planarization of Processed Si IC Wafers for Planar Optical Waveguide Formation

Personnel
E. Barkley (C. G. Fonstad, Jr.)

Sponsorship
Singapore-MIT Alliance

The integration of mixed materials and the corresponding material technologies has implied benefits for various applications from MEMs and sensors to optical communications and smart RF systems. Low temperature wafer bonding is an attractive technique that can be used to achieve the wafer-scale integration of various materials. The reduced temperatures allow for integration (bonding) with fully processed wafers, meaning that the well established separate base processes need not be altered. Our low temperature wafer bonding process starts with the deposition of several microns of PECVD oxide layer on both wafers. This layer is CMP'd (Chemical-Mechanically Polished), removing much of the deposited oxide layer and significantly increasing the planarity of the surface. This cycle is repeated until the required level of planarity is achieved. The wafers are then cleaned with the dual purpose of removing particles and achieveing surface activation to ensure a strong initial room termperature bond. The wafers are bonded at room temperature and are then annealed at higher temperatures to harden the bond. The upper temperature limit is set by the difference in thermal expansion coefficients for the two materials. In the case of wafer bonding in which one of the wafers is an SOI wafer, the SOI sustrate may be selsctively removed resulting in an increase in the annealing upper temperature limit for the thinned bonded wafer pair.

In past research we discovered that it was difficult to repeatedly achieve strong wafer bonds. We now attribute this uncertainty to the past inability to quantitatively measure and detect particles present on the wafer surface that were not removed by the cleaning step. Through a collaboration with Lincoln Labs, we have been studying and quantifying the effects of particle counts and surface microroughness on low temperature wafer bonding unsing 6" test wafers. We have been using a Tencor SurfScan particle counter to determine particle counts for our wafers at each step in the process (post-dep, post-CMP, post-clean). Although more testing is still required, we have found that particle counts can be significantly reduced by water-polishing the wafers post-CMP. The water polish step is basically just the CMP step repeated with DI water used in place of the CMP slurry. However, we have found that the water polishing step even when combined with a standard piranha clean is not sufficient to achieve repeatable strong bonds. We are currently seeking additional cleaning steps such as megasonic cleaning which has been shown to be successful by the 3D integration group at Lincoln Labs.

We have recently begun a study of the integration of waveguides on processed Si wafers, a topic we are well positioned to address because of our expertise in planarizing processed wafers for bonding. Our objective is to be able to add upper layer dielectric optical waveguide interconnect layers to a processed silicon wafer to complement the already existing metallic electrical interconnect layers formed in standard back-end processing. There is an extensive literature dealing with dielectric waveguides on silicon wafers, and significant attention has been paid to improving the waveguide deposition and definition processes in an attempt to minimize losses while achieving proper core and cladding dimensions and refractive index difference. However, almost all of this work has been done on silicon wafers without underlying devices and circuitry, and thus it does not address the issue of fabricating guides in a realistic environment. In particular, it does not deal with the issue of potential losses caused by the non-planarity of the wafer surface introduced by the metal layers in the back-end. The surface upon which the waveguide core is deposited must be flat enough to keep surface-normal scattering at some acceptable level. We are planning on studying how CMP be used to planarize the wafer surface prior to core deposition in an attempt to minimize scattering losses. This work will build directly on our work planarizing processed wafers for bonding.

Waveguide Materials for Microphotonics

Personnel

S. Akiyama, J. Sandland, M. Stolfi, V. Nguyen, A. Eshed, M. Navi Marenzi, X. Duan, K. Wada, and J. Michel (L. C. Kimerling)

Sponsorship

MARCO/DARPA Focused Research Center on Interconnect, Pirelli Labs, Draper Labs, and CMSE

Silicon Oxynitride Film for Optoelectronic Applications

The Silicon Oxynitride (SiON) materials system provides a very flexible system for producing waveguides.

Silicon oxynitride films can be produced with refractive indices ranging from that of silicon dioxide (1.46) to that of silicon nitride (2.0). This wide index range allows a great deal of flexibility in index contrast while remaining in the silicon oxynitride materials system.

However, current deposition methods, such as PECVD, have significant limitations. Hydrogen incorporation during processing causes substantial absorption in the 1550 nm wavelength window. Additionally, high post-annealing stresses often lead to film cracking and delamination. These film quality issues limit the useable range of silicon oxynitride indices.

This study focuses on the materials properties of low-hydrogen, moderate stress silicon oxynitride films created by reactive rf magnetron sputtering. SiON films are sputtered from a silicon nitride target in an oxygen ambient to produce films with indices ranging from 1.55 to 1.89. The refractive index tunes linearly with gas flow rate, making the refractive index easy to tune. Wavelength dispersive spectroscopy shows these films have a good match with an SiO_2/Si_3N_4 alloy (Figure 13). SIMS (Figure 14) shows the good depth uniformity of the films, and TEM (Figure 14) demonstrates that the films are homogeneous. Preliminary waveguide measurements of sputtered n=2.29 silicon nitride on silica show losses of less than 10dB/cm.

Air Trench Waveguides

Silica Optical Bench (SiOB) technology is mature and widely used in integrated WDM applications, such as Arrayed Waveguide Gratings (AWGs). The low-index-

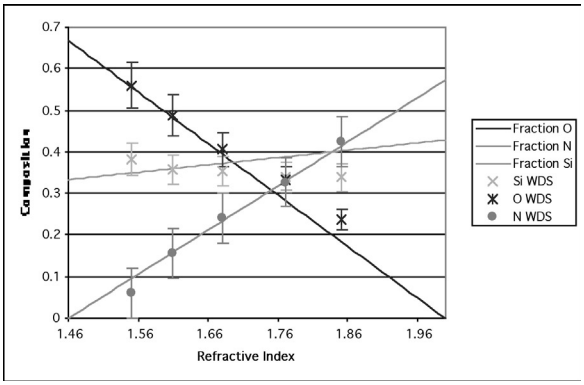

Fig. 13: Data points show atomic fraction as determined by WDS. Solid lines are predictions based on a silica/silicon nitride alloy.

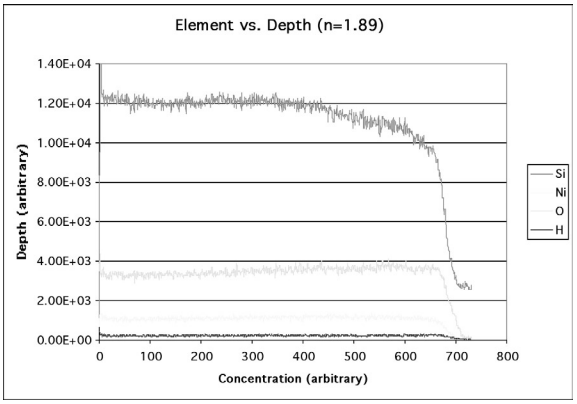

Fig. 14: SIMS profile of silicon, oxygen and nitrogen through the depth of a n=1.89 silicon oxynitride film.

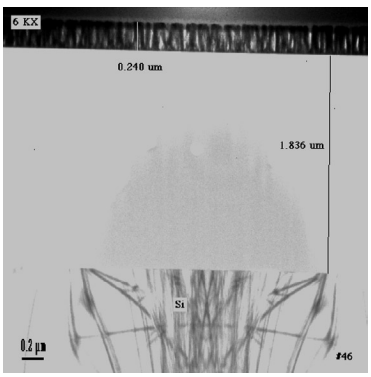

Fig. 15: TEM micrograph of n=1.89 silicon oxynitride film.

continued

continued

contrast waveguides permit low insertion loss at fiber coupling and low propagation loss. However, a major drawback is the large bending radius to keep radiation losses within acceptable range, limiting the density of integration. We proposed a simple, CMOS compatible technology that allows sharp bends in silica, therefore increasing the density of integration by orders of magnitude (Figure16). Air trench waveguides realize compact bending radii by introducing air or low index materials at the bends and hence locally increasing the index contrast. This air trench waveguide realizes high optical integration on chip using a low index contrast materials system. Therefore, this waveguide has excellent characteristics for future microphotonics applications such as low transmission loss, low bending loss, low coupling loss between fiber and waveguide in addition to small, compact bends. Simulations were done using the Finite Difference Time Domain (FDTD) method, primarily in two dimensions. These simulations show that a waveguide bend, designed to have a throughput efficiency of 98%, can be reduced in size by a factor of 10-100 with the use of air trenches. The bending radius decreases 30-500 times. For the fabrication, we employed Silicon Oxynitride (SiON) for the core and SiO_2 for the cladding. The fundamental processes such as the optimization of SiON deposition and successive defect removal annealing process, film stress management, and a precise deep oxide etch process were established.

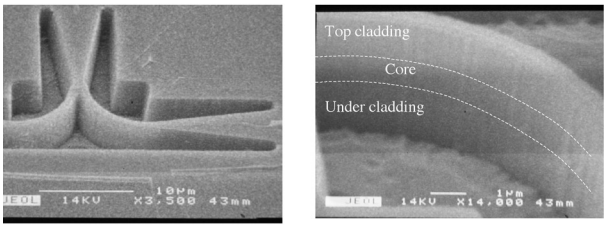

Fig.16: SEM images of an air trench T-splitter (x3,500) and an air trench waveguide(x14,000)

Strain-tunable Photonic Band Gap Microcavity Waveguides at 1.55 μm

Personnel

C. W. Wong, M. Qi, P. Rakich, S. G. Johnson, and Y.-B. Jeon (G. Barbastathis, S.-G. Kim, H. Smith)

Sponsorship

MIT Microphotonics Center

Concept and Key Idea

Photonic-bandgap microcavities in optical waveguides have demonstrated cavity resonances at wavelengths near 1.55 μm band, quality factors on the order of 300, and modal volume at 0.055 μm^3 in high-index contrast Si/SiO_2 waveguides and GaAs air-bridge waveguides. Applications include zero-threshold microlasers, filters and signal routers. For tunability in Si microphotonic platforms, thermal actuation is often utilized. Compared to thermo-optics, the novel strain-tuning via thin-film piezoelectric micro-actuators provides a significantly faster response, lower power consumption and better localization of tunability. This level of integration would permit dynamic reconfiguration of the cavity resonance and band-edges, fine-tuning for fabrication mismatches, and active compensation of device arrays to external disturbances. We have designed and fabricated the first tunable photonic-bandgap microcavities in optical waveguides, with the strain modulation via thin-film piezoelectric actuators on deformable membranes. Cavity resonance tunability, with sub-nanometer lattice control, is designed through perturbation on FDTD computations. Device fabrication integrates X-ray nanolithography, piezoelectric micro-actuators and bulk micromachining.

Device Design

The conceptual design is illustrated in Figure 17. The Si microcavity waveguide is located on a deformable double-anchored SiO_2/Si membrane. The thin-film piezoelectric actuators provide sufficient driving force, under 5V actuation, for the sub-nanometer strain control of the geometric lattice in the microcavity. Comparative designs of the double-anchored membrane have been demonstrated for analog tunable diffractive gratings. Experimental effects of static strain on coupled vertical microcavity resonators and theoretical designs for shear-modulated 2D photonic crystals on bulk piezoelectric substrates have also been reported.

continued

We employ first-order perturbation theory to obtain a semi-analytical result for the strain-induced shift in the cavity resonance; such methods ease the study of small modulations such as the 0.3% strain considered here. First, a closed-form solution for the hole boundary displacements is derived following classical mechanics. The material boundary displacements are then numerically meshed and employed in a perturbation-theory formulation, which involves surface integrals of the unperturbed fields (obtained by FDTD simulation) over the perturbed material boundaries. The result predicts a 0.8% shift in resonant wavelength (12.7 nm in the C-band) for a 0.3% mechanical strain from a 3D computation. This is illustrated in Figure 18a. While a 2D computation suggests similar final results in the resonant shift, the 3D computation highlights differences from the individual contributions – hole ellipticity, defect cavity length, and hole diameters – in the strain perturbation. Other effects such as photoelasticity and waveguide out-of-plane bending were found to be secondary.

Fabrication and Results

For resonance wavelength at 1.55 μm, the minimum feature size, located between the waveguide edges and the hole edges, is 130 nm. X-ray lithography is employed with a Cu_L source at 1.3 nm to transfer the pattern from the mask to a PMMA resist. The mask is a thin SiN_x membrane with 200 nm Au patterned with e-beam lithography. The resist image is then transferred to 50 nm of Cr, via lift-off, and etched into a 212 nm single-crystal Si layer to form our waveguide. The microfabricated piezoelectric film has an excellent dielectric constant of 1200 and a d_{31} coefficient of ~ -100 pC/N. A fiber lens assembly is used to couple a 1.430 μm to 1.610 μm tunable laser diode source, with TE polarization and lock-in amplification, into the prepared input/output waveguide facets. For a static microcavity waveguide, resonance is detected at 1555.4 nm with a Q of 159, as shown in Figure 18b. Experimental measurements of the tunable cavity resonance, band-edges and other cavity responses are currently underway.

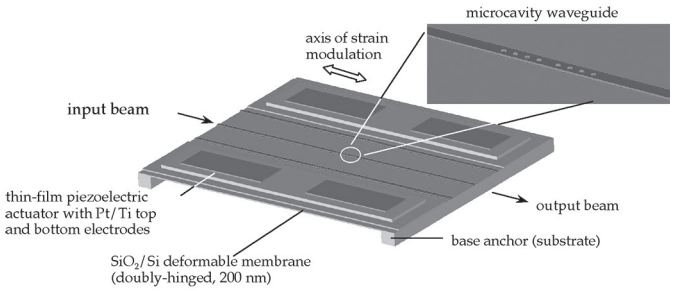

Fig. 17: Device schematic of the tunable photonic-bandgap micro cavity waveguide , with strain modulation via thin-film piezoelectric actuators on the deformable membrane.

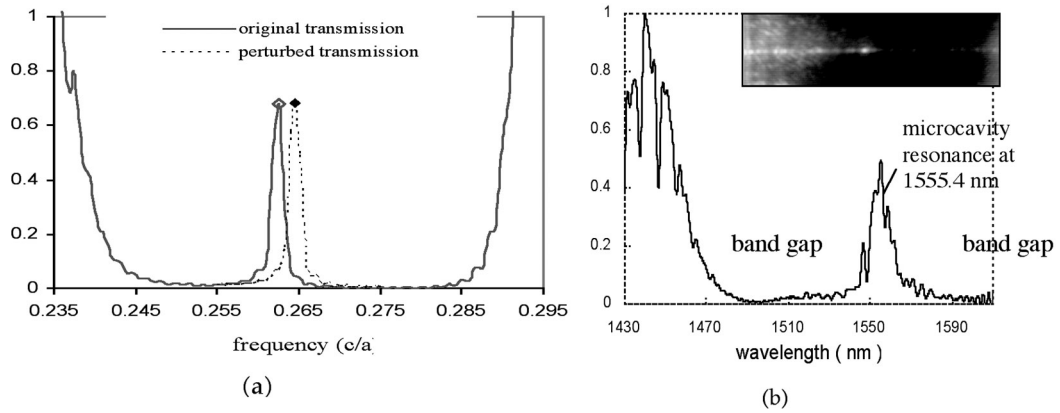

Fig. 18: (a) Computed transmission shift through perturbation theory in the photonic band gap; (b) Measured static microcavity resonance with Q of 159. Inset; top view of microcavity waveguide in transmission.

Enhanced Extraction from a Light-Emitting Diode Modified by a Photonic Crystal and Lasing Action

Personnel

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(E. P. Ippen, J. D. Joannopoulos, L. A. Kolodziejski, and H. I. Smith)

Sponsorship

NSF

Semiconductor LEDs have the potential to be low-cost and long-lifetime solid-state lighting sources for applications as varied as room lighting and flat-panel displays. LEDs are also used in short-range telecommunication systems and may be desirable for optical interconnects in computers. Unfortunately, most of the light emitted from a semiconductor LED is lost due to total internal reflection resulting in low extraction efficiency.

In this work, the effect of a Two-Dimensional (2D) Photonic Crystal (PC) on the emission properties of a Quantum Well (QW) inside an LED is examined. Enhanced extraction of light into the vertical direction is obtained and attributed to the presence of leaky resonant states created by the coherent scattering from the periodicity of the PC. Scattering along the high-symmetry directions also provides sufficient distributed feedback for lasing to occur. The 2D PC is fabricated in the top cladding layer of an asymmetric active region that emits at $\lambda = 980$ nm with a full-width at half-maximum of approximately 60 nm at room temperature. The PhotoLuminescence (PL) emission at 935 nm, normal to the surface, is enhanced by a factor of 100, and the spectrally integrated PL is enhanced by a factor of 8, both when compared to a reference structure without a PC. When optically pumped above threshold, lasing occurs at a wavelength of 1005 nm. This work provides a basis for the design of high efficiency LEDs and lasers based on 2D PCs.

The 2D PC is a 30 x 30 μm triangular lattice of holes etched within the upper InGaP cladding layer of a 50 μm mesa, as illustrated in Figure 19. To minimize carrier recombination at the etched surfaces, the holes do not penetrate the InGaAs QW; however, the hole depth is sufficient to cause enhanced extraction of light and laser feedback. The device structure is grown using gas-source molecular beam epitaxy. The separation layer is initially grown as $Al_{.98}Ga_{.02}As$ and the DBR consists of AlAs and GaAs layers. A SiO_2 layer is deposited on the grown structure using plasma enhanced chemical vapor deposition. The holes are defined in PMMA by direct-write electron-beam

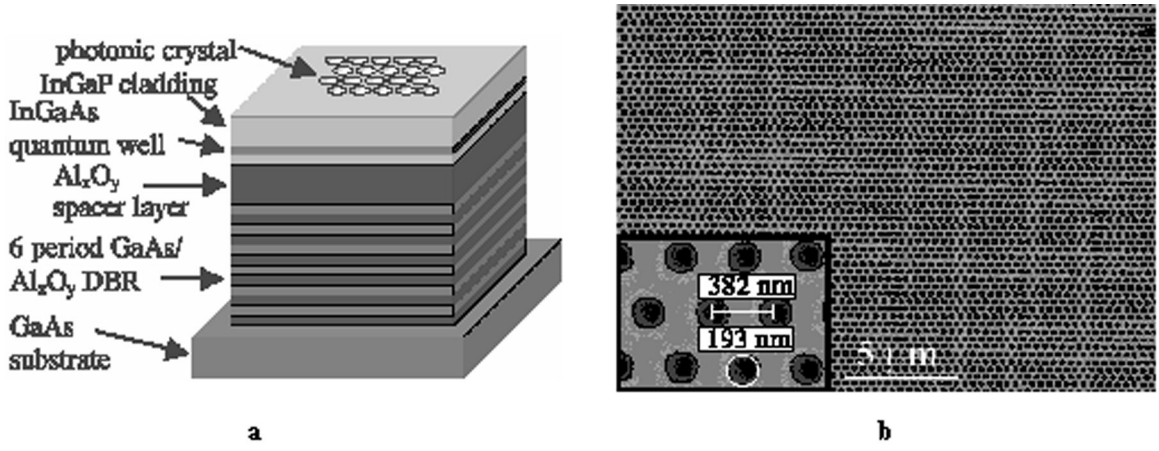

Fig. 19: a) The 2D PC structure. b) Scanning electron micrographs of PC structure.

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lithography. The electron beam writes a square pattern in the PMMA to represent each hole. The beam size, however, is larger than the step size for translating the electron beam. This leads to the desired circular pattern following development.

The PMMA is used as a mask in transferring the hexagonal pattern to the SiO_2 layer using RIE. This is accomplished by RIE with a CHF_3 plasma using 15 second steps in between 1 minute cool-down steps. The purpose of the cool-down step is to prevent flowing of the PMMA mask. The SiO_2 mask is subsequently used in the RIE of the holes into the upper InGaP cladding layer using RIE with a $CH_4/H_2/O_2$ plasma in a 20:20:2.5 gas flow ratio. The mesas are next defined using photolithography followed by RIE with the $CH_4/H_2/O_2$ plasma to penetrate the active region. RIE with a BCl_3 plasma is used to expose the mesa sidewalls. The final step in the device fabrication is the wet thermal oxidation of the $Al_{.98}Ga_{.02}As$ separation layer and the AlAs DBR layers. Figure 19b shows scanning electron micrographs of a PC structure with lattice constant, a, of 382 nm, hole diameter of 193 nm, hole depth of 101 nm, and an active region thickness of 198 nm. This structure is characterized and the results are reported below.

The photoluminescence is observed using a cw Ti:Al_2O_3 laser with an emission wavelength of 785 nm. Figure 20(a) shows a spectrum of the enhancement of PL from the PC region normalized to the same structure but without a PC. Figure 20(b) is a calculation of the photonic band structure near the G point in the first Brillouin zone. The bands represent leaky resonant states that provide a pathway for the enhancement of light extraction. On the long wavelength end of the spectrum, the range covered by the first three bands closely matches the large observed peak centered near 935 nm. The width of the peak is determined by the

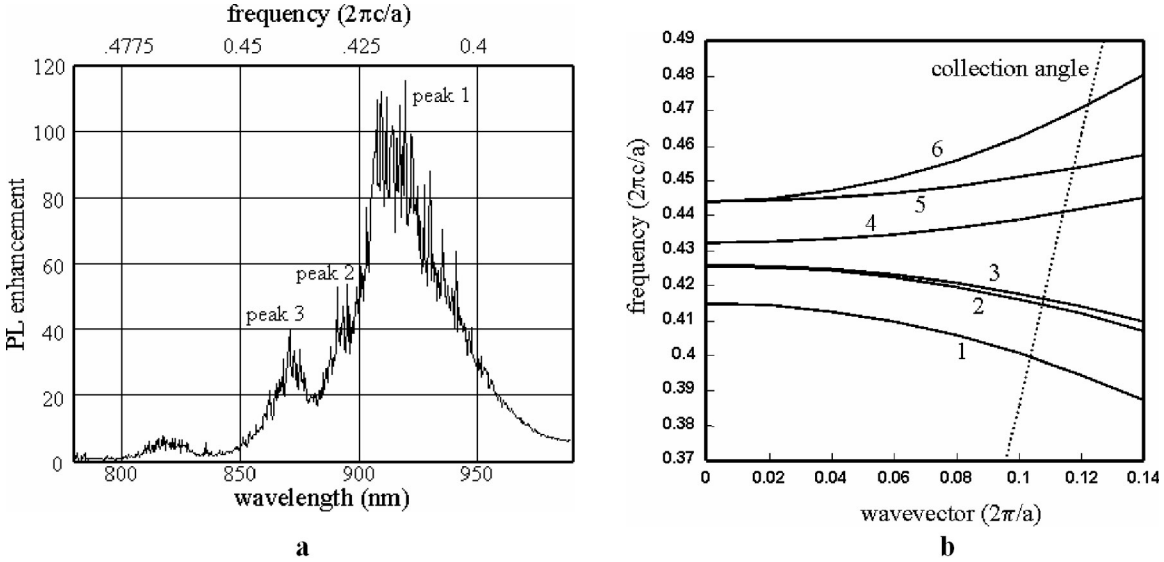

Fig. 20: a) PL enhancement spectrum from PC structure. b) Calculated hotonic band structure near G point.

continued

Q of the leaky resonance and by the collection angle (dotted line). Band 4 and bands 5 and 6 closely match the peaks near 890 nm and 860 nm respectively. The dip between peaks 2 and 3 corresponds well with the gap in available states between bands 3 and 4.

Lasing occurs at a wavelength of 1005 nm as the pump power is increased (Figure 21(a)). The lasing peak occurs from distributed feedback and corresponds well with the bending of bands at the M point (Figure 21(b)).

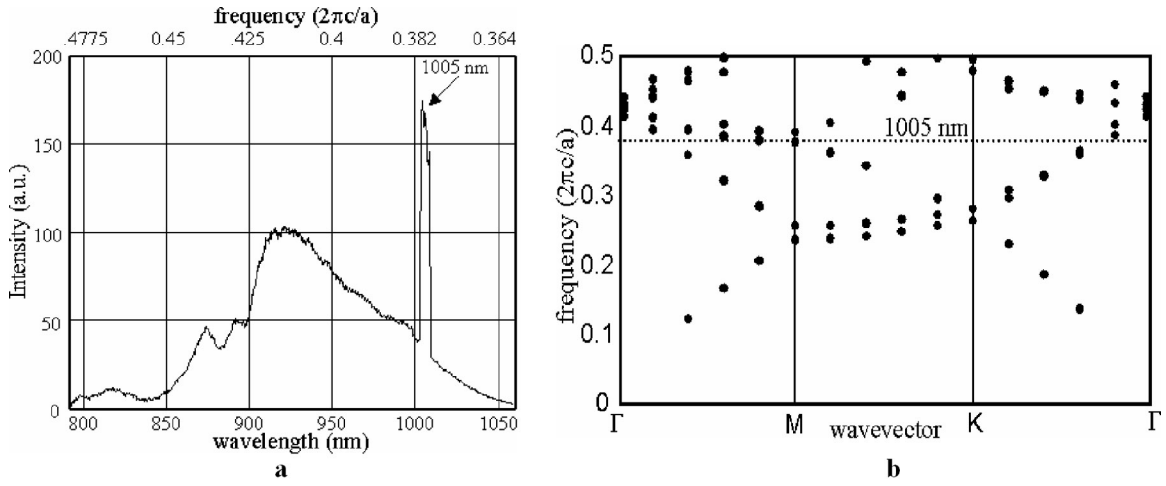

Fig. 21: a) Lasing spectrum. b) Calculated band structure showing band folding near M point.

Fabrication of 3-D Photonic Bandgap Structures

Personnel
M. Qi, J. Joannopoulos and H. I. Smith

Sponsorship
NSF

Three-Dimensional (3D) Photonic BandGap (PBG) Structures offer opportunities for miniaturizing a variety of conventional optical devices. The structure under investigation consists of a stack of alternating "hole" layers and "rod" layers, which themselves are 2D PBG structures (Figure 22). Consequently, result most results in 2D structures can be ported to the 3D design with minimal modification. Compared to other 3D structures in the literature, this design has the unique advantage that each layer is highly symmetric so that optical devices, such as cavities and waveguides can be realized by modifying only one layer. From the fabrication point of view, the rod layer is a byproduct of etching holes into the previous hole layer, which effectively cut the fabrication steps by one half.

The structure has been fabricated in a layer-by-layer approach using e-beam lithography and spin-on-dielectrics planarization. E-beam lithography has the advantages that it allows design flexibility, controlled introduction of defects and robust overlay alignment. Figure 23 shows the SEM micrographs of the final structure. Seven functional layers can be seen clearly.

With the success of the pilot process, two efforts are ongoing simultaneously. One is to fine-tune the structure and process, and the other is to demonstrate the capability of large area, low-cost fabrication of 3D PBG structures. The structure shown in Figure 22 is suboptimal because the effective radius of the rod layer is dependent on the hole size. The bandgap can increase from 21% (measured as a percentage of the midgap frequency) to 27.3% if the shape and size of the rods can be varied (in this case reduced) independently from those of the holes. However this will require that the rod layer being fabricated in a separate step. A balance can be found by changing the shapes of the holes as shown in Figure 24(a). In this way the rod

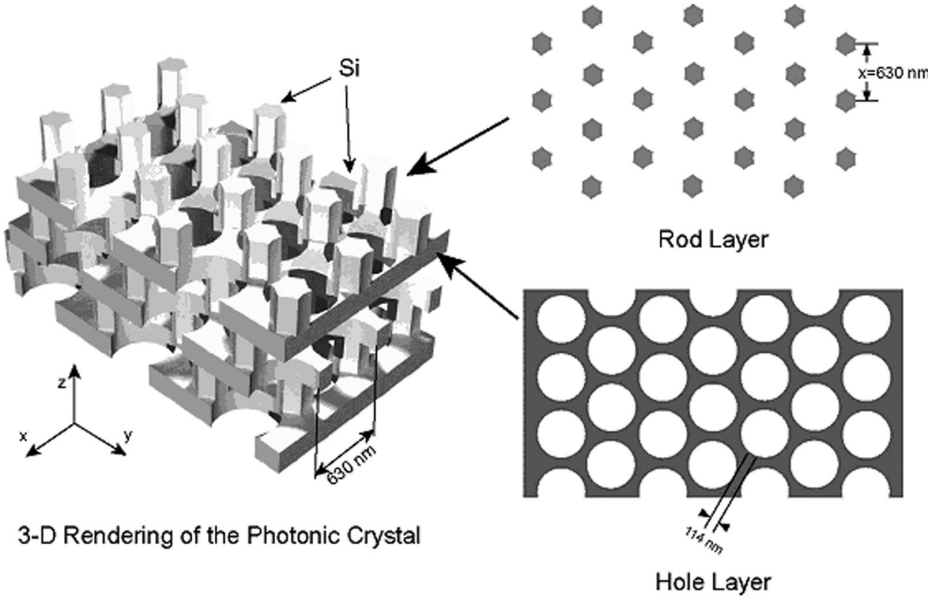

Fig. 22: A schematic of the MIT 3D photonic crystal.

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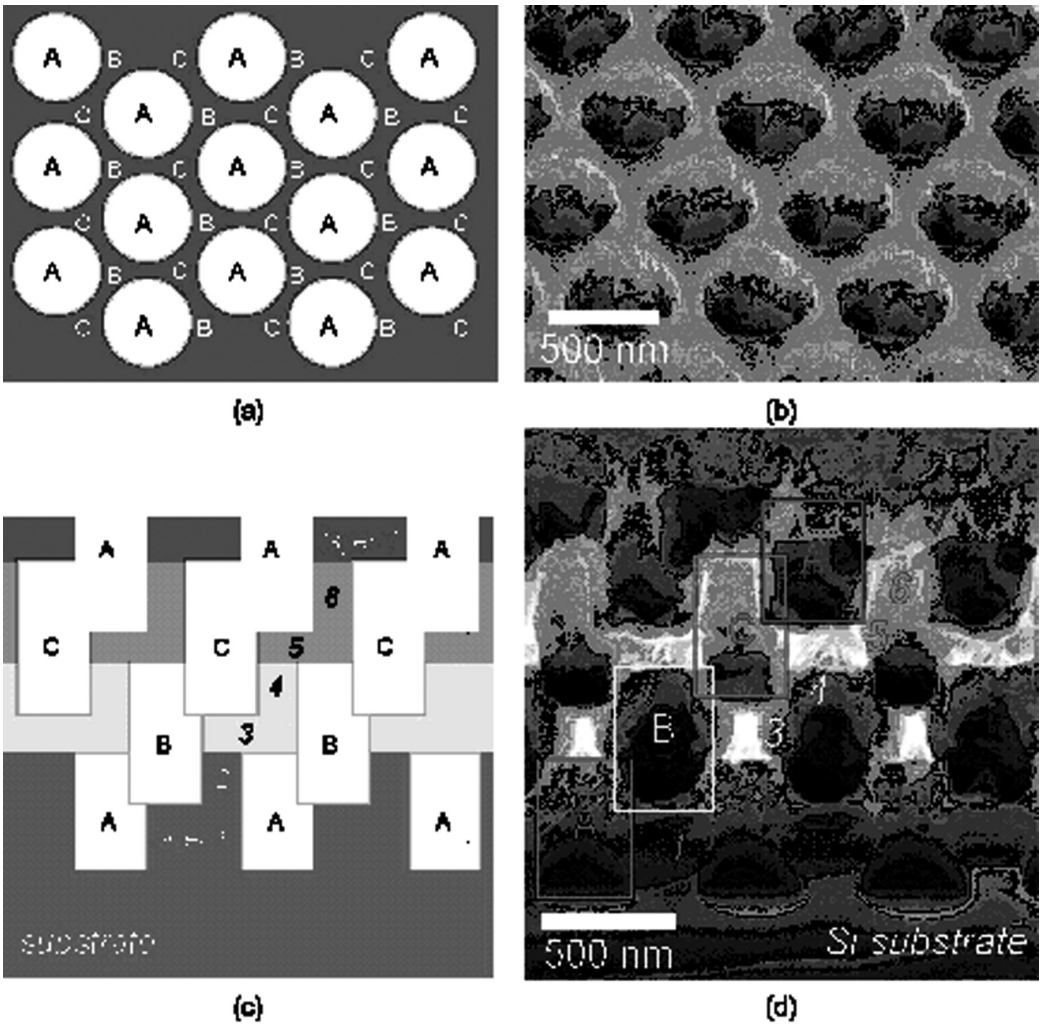

Fig. 23: (a) Schematic of the 3D photonic crystal viewed from the top, showing the hexagonal array of holes. The points marked "B" and "C" designate the centers of holes in layers beneath, as depicted in cross section in (c). (b) Scanning-electron micrograph of the seventh layer of the photonic crystal. The sixth layer can be seen through the holes. (c) Cross-sectional schematic of the photonic crystal. Different colors correspond to different process cycles. (d) A cross-sectional view of the 3D photonic crystal cleaved with a diesaw. The functional layers are marked by numbers, while the etched holes are outlined with rectangles.

continued

continued

size will be reduced due to the extra semicircular holes at the six corners of the main holes. Meanwhile the change of the effective hole size is minimal because the holes are much larger than the rods. Simulation shows that a complete bandgap of 25% can be achieved, which is a 19% increase over the original 21% gap. The fabrication of such a structure will be no different than the pilot process since the e-beam lithography can pattern virtually any shapes. A larger bandgap is highly desirable because it displays the biggest optical effects, allows the widest bandwidth for optical devices, and most importantly, is robust in the presence of fabrication imperfections.

In order to realize real-world applications of 3D PBG structures, large area and spatial coherence are required. Interference lithography can easily pattern a hexagonal lattice of holes (or rods) by a double exposure with the second exposure rotated 60 degrees from the first. However, the holes obtained are elliptical. Such elliptical shape breaks the hexagonal symmetry of the lattice, and simulation shows that the bandgap will be reduced by a factor of two. Last year we proposed a set of new techniques which overcame such difficulty via a combination of interference lithography and tilted X-ray lithography. The method is ideally suited to low-cost, large-area 3D fabrication of periodic structures. This year we set up the equipment and demonstrated the synthesis of a hexagonal array of circular holes (Figure 25). The staging that we build for exposure is shown in Figure 26.

By combining this tilting technique and an overlay alignment technique, such as Interferometric Broad-Band Imaging (IBBI), it should be possible to fabricate large area 3D photonic crystal.

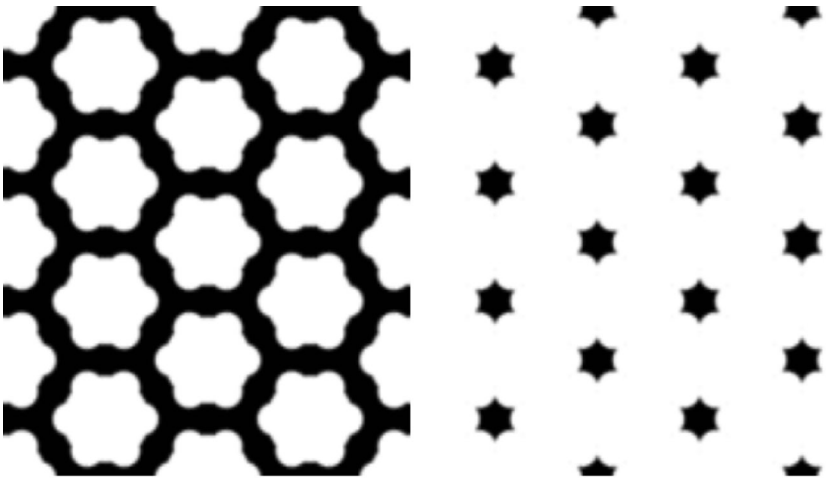

Fig. 24: Schematics of the improved 3D PBG design. (a) The "hole" layer. (b) The "rod" layer.

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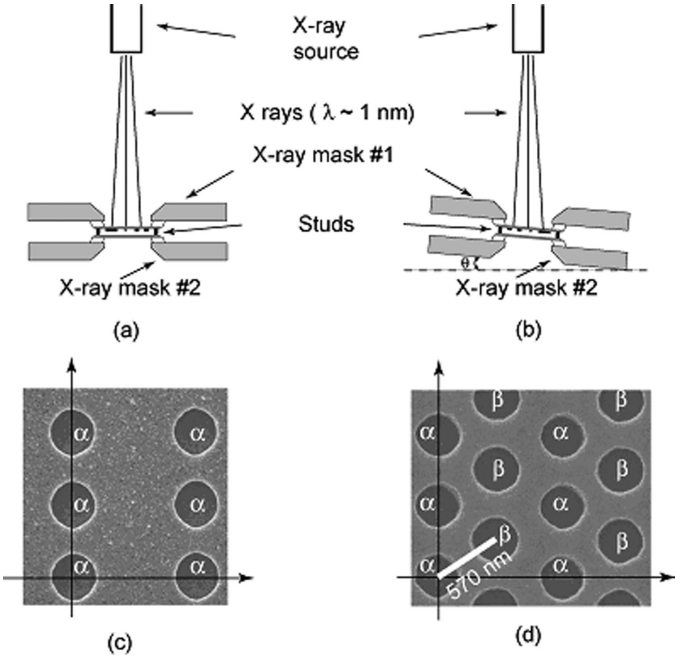

Fig. 25: Synthesizing a hexagonal lattice of circular holes with tilted X-ray exposure. (a) Schematic of proximity X-ray exposure. (b) After the first exposure, a second one is carried out with the mask-substrate assembly tilted with an angle q=G/V, where G is the gap between the mask and substrate and V is the image shift vector, in this case it is set to 570nm. (c) Pattern on X-ray mask #1. (d) Pattern on the substrate after the double exposure (in this case the substrate is a wafer).

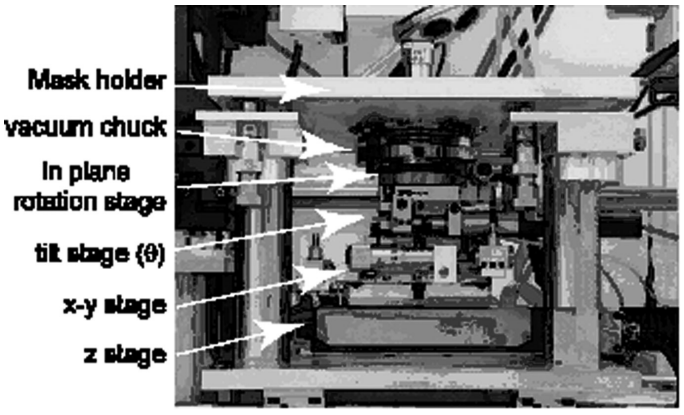

Fig. 26: Photograph of the stage for tilted X-ray exposure. The X-ray source, which is not shown, is above the mask holder.

Guiding Light Through Sharp Bends Using Two Dimensional Photonic Crystals

Personnel

S. Assefa, A. A. Erchak, P. Rakich, S. G. Johnson, M. Mondol, P. Bienstman, and G. S. Petrich (H. I. Smith and L. A. Kolodziejski in collaboration with E. P. Ippen, and J. D. Joannopoulos)

Sponsorship

NSF

Large-scale photonic integrated circuits require guiding light around sharp bends with a radius of curvature on the order of a wavelength. In conventional index-guided waveguides, light is confined as a result of total internal reflection at the interface between the high refractive index waveguiding layer and its low index surroundings. However, bends in index-guided waveguides are susceptible to large optical losses as the radius of curvature decreases. Photonic Crystals (PCs), which consist of a periodic arrangement of high- and low-dielectric constant material, have been proposed as a potential solution in order to guide light around corners, including 90° bends, with near perfect transmission.

One such Two-Dimensional (2D) photonic crystal consists of an array of cylindrical rods of high dielectric material above a low dielectric material. Introducing a line defect, such as a row of smaller diameter cylinders into the 2D photonic crystal, results in a linear waveguide. The 2D periodic arrangement of dielectric rods, surrounding the line defect, contains a Photonic Band Gap (PBG), i.e. a range of frequencies in which light can not propagate. Thus, an optical signal with a frequency inside the PBG has its energy confined within the line defect and is evanescent within the photonic crystal. The diameter of the cylinders in the line defect remains large enough to provide index guiding in the third dimension (normal to the plane of periodicity). The localization of a mode inside the line defect can be utilized to guide light around sharp corners, including a 90° bend, with low optical loss.

Nevertheless, the practical use of photonic crystal waveguides is limited due to the poor coupling efficiency between the photonic crystal waveguide, and the conventional index-guided waveguide. Coupling poses a challenge because the photonic crystal waveguide exhibits a significantly different mode profile and propagation mechanism as compared to traditional waveguides that use index confinement. In the conventional waveguide, the field has only forward propagating components, while the field in the photonic crystal waveguide has both forward and backward propagating components due to scattering. Furthermore, guiding in the conventional waveguide is in the high index core that is surrounded by a low index material; in the photonic crystal waveguide, guiding is in a low effective index core that is surrounded by two photonic crystal mirrors.

Three different designs for coupling into the defect photonic crystal waveguide are being investigated. In the first design, the waveguide abruptly terminates prior to the photonic crystal region. This design suffers from Fabry-Perot reflection at the edges of the photonic crystal region, which makes the transmission of the waveguide dependent on the photonic crystal waveguide length. In the second design, the input and output ends of the index waveguides are tapered, which reduces the reflections. In the third design, the input waveguide is adiabatically converted into a strongly coupled cavity waveguide. This adiabatically transforms the forward propagating component of the field into both forward and backward propagating components before reaching the photonic crystal. Also, the photonic crystal cladding is introduced slowly from the edge, thereby, adiabatically transforming the mode from high-index guiding to gap guiding. 2D simulations show that this third coupling scheme results in almost 100% transmission through the photonic crystal waveguide.

The cylindrical rods of the photonic crystal consist of a high-index, 830nm thick epitaxial GaAs layer sandwiched between a 100nm thick SiO_2 cap layer and a 600nm thick low-index Al_xO_y layer. An additional 900nm thick Al_xO_y layer is below the cylindrical rods isolating the GaAs guiding layer from the GaAs substrate. The structures are fabricated using gas source

continued

molecular beam epitaxy, hard etch mask deposition, direct-write electron beam lithography, Ni lift-off, reactive ion etching, and AlAs oxidation. Figure 27 shows Scanning Electron Microscope (SEM) images of the three designs at various stages of fabrication. Figure 28 shows a side view of the bulk photonic crystal.

Currently, the photonic crystal devices are being tested. The band gap is being mapped first by varying the number of columns in a bulk photonic crystal. Also, the three coupling mechanisms are being compared by measuring the transmission through the photonic crystal waveguide.

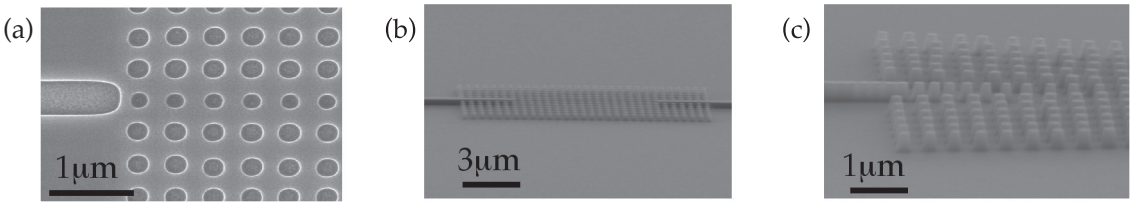

Fig. 27: Top view SEM image of (a) the first coupling design after electron-beam lithography, (b) the second coupling design after a hard mask etch, and (c) the third coupling design after a hard mask etch.

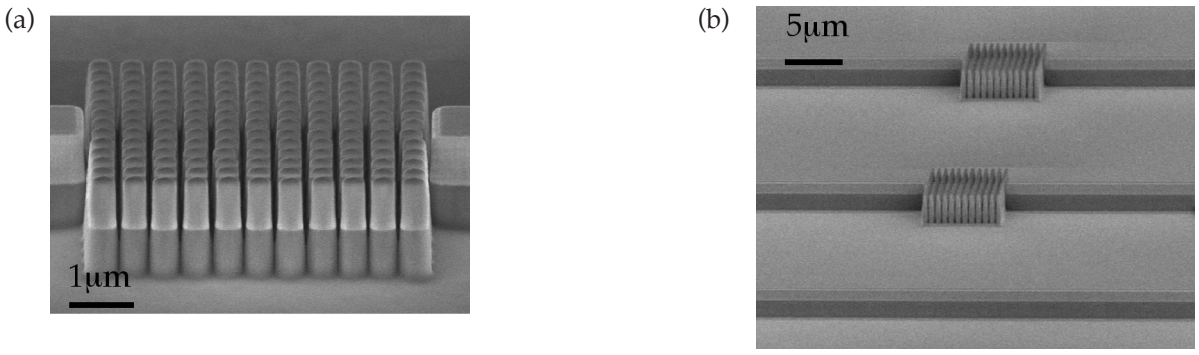

Fig. 28: (a) Side view SEM image of a bulk photonic crystal. The period is 500nm and the diameter of the pillars is 300nm. The input and output waveguides are 1.5μm wide. (b) Photonic crystal devices on a single chip. The design contains a straight waveguide for normalization purposes.

GaAs Superprism Using Two-Dimensional Photonic Crystals for Enhanced Beam Steering

Personnel

S. Tandon, C. Luo, M. Soljacic, M. E. Walsh, and G. S. Petrich
(H. I. Smith and L. A. Kolodziejski in collaboration with J. D. Joannopoulos)

Sponsorship

DARPA and Rockwell Scientific Corporation

A superprism is an optical device similar to a conventional prism only with two enhanced properties: (1) super-dispersion; and (2) ultra-refraction. Just as a conventional prism separates light into multiple wavelengths, a superprism separates these wavelengths over wider angles--termed "super-dispersion." A superprism can also be used to magnify the angle of propagation of a single wavelength of light to steer the beam over a wide range of angles--termed "ultra-refraction." Photonic crystals form the essence of the superprism effect. Being able to realize these superprism effects would be very useful for a number of applications ranging from enhanced devices for Wavelength-Division-Multiplexed (WDM) systems to a new class of ultra-refractive optical elements for beam manipulation.

The device consists of a two-dimensional photonic crystal with a square lattice of cylindrical air holes in a high index material such as silicon or gallium arsenide. The device is hexagonal-shaped with the Photonic Crystal (PC) occupying a square region in the center. The initial design has focused on realizing ultra-refraction such that an input angular sweep of approximately +/- 2 degrees is amplified to about +/- 30 degrees at the output for a wavelength of 3.2 μm. A thick low index layer is used to minimize radiation loss into the high index substrate.

The feature sizes of the photonic crystal can be scaled depending on the wavelength of operation. The desired wavelengths of 3.1μm and 1.55μm imply lattice constants of 750nm and 372nm, and hole radii of 300nm and 150nm, respectively. The total thickness of the device (excluding the substrate) is about 3.5 microns (460nm GaAs, 3μm Al_xO_y) while the top surface will have an area of about 2 x 2cm.

The hexagonal device shape is patterned using photolithography; while the photonic crystal holes are patterned using interference lithography. Figure 29(a) shows a digital photograph of the patterned hard mask layers on a silicon substrate. Two hard mask layers have been used: 50nm chromium on top of 250nm HSQ (spin-on oxide). The chromium layer is patterned with the superprism hexagonal shape, while the open square area is patterned with the ~780nm period photonic crystal in HSQ. The diffraction pattern from the PC can be seen as the streak across the square area. Figure 29(b) shows a microscope image (100x magnification) of the corner region of the photonic crystal area. The unit cell of the PC is rotated 45 +/- 1 degrees with respect to the square region. The alignment accuracy between the photonic crystal orientation and the square region is critical for superprism performance.

Future work includes calibrating the photonic crystal hole size during the interference lithography exposure, determining a more robust hard mask layer other than chromium due to post-wet etch residue, and reactive ion etching of the silicon substrate material via reactive ion etching.

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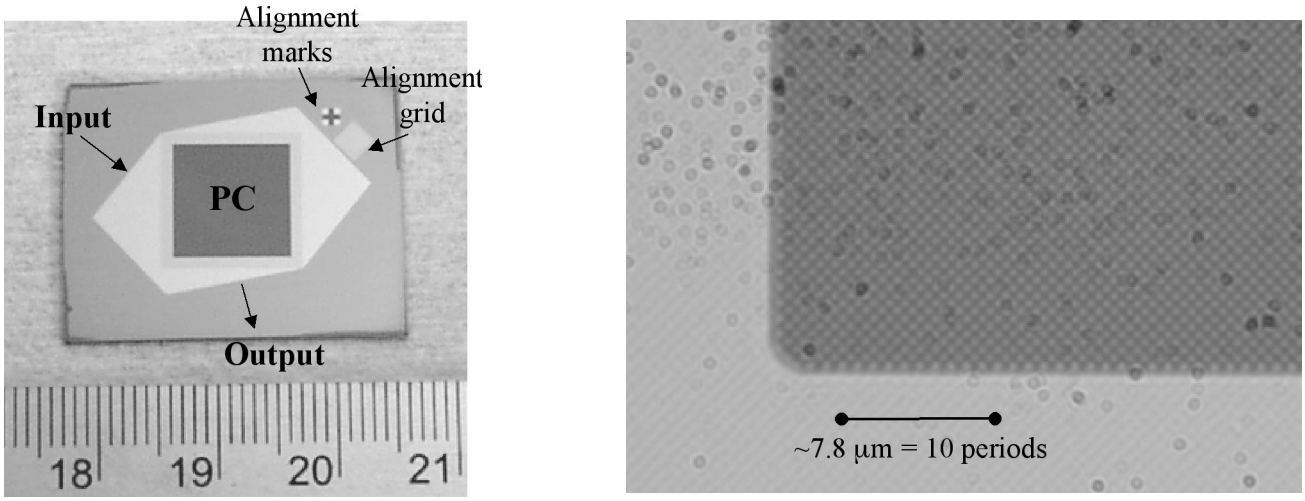

(a) *(b)*

Fig. 29: (a) Digital photograph showing a top view of the superprism hard mask layers on a silicon substrate. (b) Microscope image of the corner area of photonic crystal region. Please note that the microscope lens has dust particles that can not be removed.

Application of RM³ Integration to Optical Clock Distribution on Si-CMOS

Personnel

E. Atmaca and W. Giziewicz (C. G. Fonstad, Jr. in collaboration with D. Boning, MIT, and Y. S. Fatt, Nanyang Technological University, Singapore)

Sponsorship

MARCO Focused Research Center on Interconnect (MARCO/DARPA) and National Science and Engineering Research Council of Canada Postgraduate Scholarship

One of the most significant factors limiting future microprocessor performance and consumers of microprocessor power is the clock distribution network. As clock rates continue to rise, the design of the clock distribution network will assume an increased importance. From the power point of view, the H-tree or other networks that distribute the global clock to functional subunits are continually growing and must be charged and discharged during each cycle. From the performance point of view, as die sizes and clock rates increase, clock skew becomes very significant.

Optical clock distribution could address most of these problems. Depending on the scheme in use, deterministic skew may be significantly reduced. A global optical clock would also decrease power consumption as large metal lines (designed for high current-carrying capacity) would no longer require charging at each clock cycle. Optical distribution would also avoid a good deal of random skew for the same reason. Random skew in this design would be contributed by process variations affecting the performance of the optical receivers of the global clock. Circuit techniques to perform compensation of this sort of variation are being investigated and developed by Prof. Boning and his group at MIT. In a collaborative effort to study optical clock distribution, we are using our RM³ (recess mounting with monolithic metallization) technology to integrate high performance III-V photodetectors on CMOS integrated circuit chips designed by Prof. Boning's group.

In this work, InP-InGaAs PiN diodes are to be integrated with Si-CMOS electronics to provide efficient, high speed photodetectors to receive the optical clock signals. As shown in Figure 30, diode heterostructures (grown by MBE in Prof. Yoon Soon Fatt's laboratory at Nanyang Technological University in Singapore) are being bonded to 0.18um Si-CMOS test chips designed by Prof. Boning and his students, and fabricated by a foundry, in this case, Taiwan Semiconductor Manufacturing Company. Following bonding, the diode heterostructures will be processed in place on the chip with the deposition of ohmic contacts, a mesa etch to control dark current, passivation dielectric material, and a metal line to join the diode ohmic contacts with Metal-7 V_{dd} lines.

We have, recently, also entered discussions with Profs. David Miller and Mark Horowitz of Stanford University regarding the use of our recess mounting technology to realize their direct input (no amplifier) optical clock distribution proposals to overcome process-related skew and to significantly reduce latency. A key requirement of their approach is that the capacitance seen at the output node of the photodiode, which in their approach is loaded by the junction capacitance of two photodiodes, the input to an inverter stage, and any associated parasitic capacitances, must be 10 fF, or less. We have proposed a RM³-integrated device design that, in theory, achieves this level of performance, something that is not possible using other technologies they have considered. We expect to begin an effort to demonstrate this experimentally in the coming year.

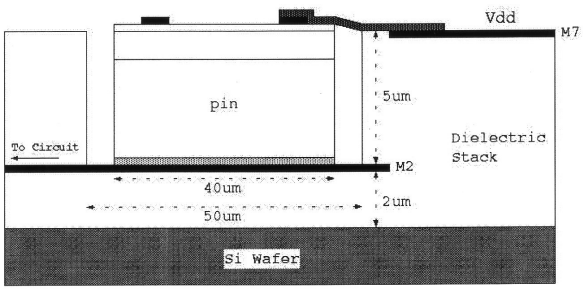

Fig. 30: Cross-sectional drawing illustrating a InP-InGaAs PiN photodiode ABP integrated on a CMOS integrated circuit chip for use in optical clock distribution studies.

Aligned Pillar Bonding Technology for RM^3 Integration

Personnel
E. Atmaca and W. Giziewicz (C. G. Fonstad, Jr.)

Sponsorship
NSF and MARCO Focused Research Center on Interconnect (MARCO/DARPA)

A new heterogeneous integration technique is under development which uses aligned, selective-area bonding to integrate III-V heterostructure devices, such as laser diodes and p-i-n detectors, with commercially-processed Electronic Integrated Circuits to create OptoelEctronic Integrated Circuits (OEICs) with VLSI levels of density and complexity. This technique has been named Aligned Pillar Bonding (APB); it is illustrated in Figure 31. The APB technique is similar in function to the Epitaxy-on- Electronics (EoE) technique in which III-V device heterostructures are first grown epitaxially in dielectric growth windows exposing the substrate surface in selected areas on fully-processed GaAs integrated circuit wafers. The APB process used bonding rather than direct selective area epitaxy to add heteostructures to processed IC wafers. It is compatible with any VLSI process on wafers that match the thermal expansion coefficient of the heterostructure wafer, meaning that GaAs-based heterostructures can be APB-integrated on both GaAs IC wafers and on silicon-on-sapphire IC wafers.

In the APB technique, the heterostructure for an optoelectronic device, such as a laser diode, is first grown under optimal conditions on the optimal substrate. The heterostructure is then patterned into pillars, which are in turn bonded into dielectric windows on a suitably prepared integrated circuit wafer (i.e., into the same windows that would be used for epitaxy in the Epitaxy-on-Electronics process). Doing this requires something more complex than encountered in previous III-V bonding experiments, namely alignment. The wafer on which the device heterostructure is grown and the pillars are formed, called the "source" wafer, must be aligned with the dielectric windows on the integrated circuit wafer onto which the devices are to be bonded. This wafer is called the "target wafer.

We have developed techniques using equipment developed originally for MEMS processing for achieving this alignment, and several years ago, demonstrated the successful aligned fusion of III-V pillars in dielectric windows on a GaAs IC chip. We, then, also demonstrated the subsequent removal of the substrate of the source

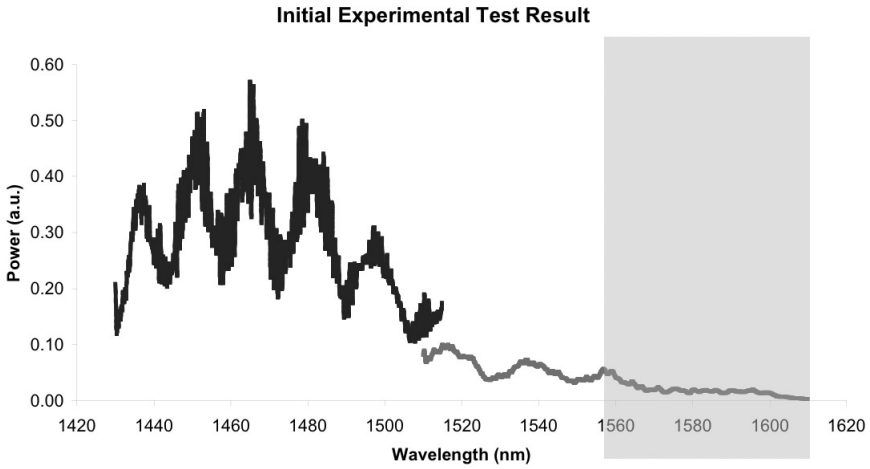

Fig. 31: The APB process: (a) the processed IC wafer as received from the manufacturer, and (b) the heterostructure wafer with pillars etched to match the windows on the IC wafer; (c) after bonding of the heterostructure and IC wafer; (d) after removal of the substrate of the device wafer leaving heterostructures bonded in the windows; and (e) after completing device processing and integration.

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wafer to complete the transfer of the pillars to the target wafer. That initial work involved direct semiconductor-to-semiconductor bonding and required substantial pressure to achieve contact and bonding. Subsequent work has investigated layered Au/Sn alloy-to-Au/Sn alloy, palladium-to-GaAs, and layered tin and palladium-to-GaAs bonding. Non-aligned bonding has been demonstrated using all three systems, and work on aligned bonding is continuing, with out current emphasis being on the first system. A major difficulty we have experienced recently, however, is accessing suitable aligned bonding equipment. Equipment in the MIT Microsystems Technology Lab does not currently have fixtures for work with partial wafers, an economic necessity when dealing with processed circuits. We have been using a bonder at Northeastern University with limited success.

Optimization of Cells for Microscale Themophotovoltaic Energy Conversion

Personnel

M. Masaki (C. G. Fonstad, Jr in collaboration with R. DiMatteo of C.S. Draper Laboratory, Inc., and P. Haglestein)

Sponsorship

C. S. Draper Laboratory, Inc.

In 2000, we succeeded in our effort to provide the first experimental demonstration that a significant increase in the rate of ThermoPhotoVoltaic (TPV) energy conversion (5 to 10 times) is obtained by positioning the active diode surface in extreme close proximity to the radiator (on the order of a tenth of the wavelength of the radiation, or less). The demonstration of this proximity effect, which we have earlier shown theoretically is due to enhanced evanescent coupling of radiation for the radiator to the cells, is the first step in the creation of a new class of Microscale ThermoPhotoVoltaic (MTPV) devices which promise to make the extraction of electrical energy from a wide variety of heat sources practical and to provide a new class of compact, portable sources of electricity. Moreover, MTPVs will be able to utilize thermal energy, now discarded as waste heat, and will enable increases in the overall efficiency of many complex systems.

The initial demonstration devices were InAs cells grown and fabricated at MIT. InAs cells are ideally suited for the applications ultimately envisioned for MTPV, but are less readily available than wide bandgap InGaAs diodes; so the Draper experimental work has continued using InGaAs cells obtained through their government sponsors. They have, recently, also begun procurement of cells with all of the contacts made to the epitaxial side of the wafer and designed to be "illuminated" through the substrate. Recalling that the proximity effect is due to enhanced evanescent coupling of light between the high refractive index radiator into the high refractive index cell, one realizes that the active junction need not be in close proximity to the source of radiation, making this substrate illumination geometry very attractive; because it places the temperature sensitive junction much further away for the high temperature source and significantly reduces the thermal management problem.

At MIT, we have concentrated on modeling and understanding how best to optimize the basic TPV device

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structure. An important aspect of our modeling effort has been directed at understanding the impact of the proximity effect on overall system efficiency. To the first order, one would expect that while the output level of a cell increases due to the proximity effect, the cell efficiency remains the same. Closer consideration, however, reveals that while the efficiency of the cell in converting absorbed photons to junction current will not increase, the overall power conversion efficiency will increase because of the concentrator effect. That is to say, because the diode characteristic is exponential, and the output power depends on the maximum of the product of the cell current and cell voltage, the power conversion efficiency of a TPV cell increases as one drives it harder, i.e., with more intense illumination and therefore, larger short circuit current. The parameter that matters in this situation is the ratio of the short circuit photocurrent to the reverse saturation current of the diode. The larger this ratio, the better, particularly when the ratio is relatively low. That is to say, if the ratio is already very high, as it is in the case of a silicon solar cell illuminated by sun light, for example, then increasing it by a factor of 10 improves the power conversion efficiency only a few percent, and it must increase by several orders of magnitude to have an appreciable effect. When this ratio is low (10^1 to 10^4, for example), however, as it is in the present case because we have narrow bandgap diodes (i.e. large saturation current) and weak illumination (i.e. small photocurrent), then increasing the ratio by even a factor of 10 can have a meaningful effect and can increase the efficiency 15 to 20%. Thus, the proximity effect has a dual impact on TPV cells. It significantly increases their rate of thermal-to-electrical energy conversion, and it increases the efficiency of this conversion.

In the past year, we have also participated in extensive discussions looking at other proximity effects that can be exploited to further increase the efficiency of the thermal-to-electrical energy conversion process.

Recess Mounting with Monolithic Metallization (RM^3) Polylithic Integration Technology

Personnel

E. Atmaca, E. Barkley, W. Giziewicz, J. Perkins, and J. Rumpler (C. G. Fonstad, Jr.)

Sponsorship

NSF , MARCO Focused Research Center on Interconnect (MARCO/DARPA) , SRC, and Singapore-MIT Alliance

Heterostructure devices, such as laser diodes and high electron mobility transistors, play an increasingly important role in our lives, and are key, enabling components of such common items as compact disk players, cellular telephones, fiber communication links, and direct broadcast television receivers. Their impact would be even greater, however, if a technology existed which could integrate heterostructure devices with silicon VLSI circuitry, using the same monolithic wafer-scale batch processing techniques that are largely responsible for the continuing Moore's Law growth of integrated circuit performance and functionality. Addressing this bottleneck, our research group in the MIT Microsystems Technology Laboratory and Center for Materials Science and Engineering has made significant advances in integrating complex compound semiconductor heterostructure devices with commercial VLSI (Very Large-Scale Integration) electronic circuits.

We refer to the general integration methodology we are pursuing as Recess Mounting with Monolithic Metallization, or RM^3 (i.e., "RM-cubed") integration, for short. This is a name introduced last year to more clearly indicate the common unifying themes of the several integration techniques we are studying: the mounting of the devices, or device material, to be integrated in shallow recesses formed in the surface of processed integrated circuit wafers, followed by continued monolithic processing to complete the devices, processing their electrical interconnection with the pre-existing circuitry using monolithic metallization.

Our Epitaxy-on-Electronics (EoE) and Aligned Pillar Bonding (APB) processes have been developed to integrate state-of-the-art heterostructure devices on commercially-processed GaAs and Silicon-on-Sapphire VLSI-level integrated circuits. Recently, we have initiated two new collaborative research programs in which we are integrating optoelectronic devices on custom designed silicon CMOS ICs for three quite different

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applications: optical clock distribution on CMOS chips, diffuse optical tomography subsurface imaging in living tissues, and free-space parallel optical signal processing. We have also continued our efforts to improve our techniques for heterogeneous integration, and to this end, we are researching a novel technique we call Magnetically-Assisted Statistical Assembly (MASA). In MASA, we form heterostructure nanopills and physically place them directly into the recesses on an IC wafer surface, exploiting statistics and magnetism.

Our successful Silicon-on-Gallium Arsenide (SonG) program has shifted from a program directed solely at providing wafers for optoelectronic integration to one also investigating three-dimensional integration of GaAs- and Si-based electronics. Most recently, we have begun investigating the use of the CMP (chemical-mechanical polish) techniques we have developed for this work to fabricate planar dielectric optical waveguides on the surface of processed Si wafers, in effect, adding additional optical "metal" layers to the normal backend process. These waveguides will be designed to couple directly to RM^3 integrated in-plane laser diodes and photodiodes, providing a total optical interconnect fabric for the electronics and optoelectronics communities.

More extensive descriptions of the individual projects within Professor Fonstad's RM^3 research program can be found in subsequent abstracts in this section.

Magnetically-Assisted Statistical Assembly

Personnel

J. Perkins and J. Rumpler (C. G. Fonstad, Jr.)

Sponsorship

Singapore-MIT Alliance and SRC

We have recently proposed a radically new approach to the heterogeneous integration of compound semiconductor devices, such as laser diodes with silicon integrated circuits, and have begun an experimental program to develop this technique. Our new approach, called Magnetically-Assisted Statistical Assembly (MASA), uses statistical self-assembly to locate compound semiconductor device heterostructures in shallow recesses patterned into the surface of an integrated circuit wafer, and short-range magnetic attractive forces to keep them there. When all of the recesses on the wafer are filled with heterostructures, the wafer is processed further to transform the heterostructures into devices monolithically integrated with the underlying circuitry. The process is summarized in Figure 32.

During statistical assembly, the surface of a wafer prepared with recesses will be flooded with several orders of magnitude more nanopills than are needed to fill its recesses. The large number of pills will mean that there are many pills in the vicinity of each of the recesses, and the highly symmetric nature of the pills and recesses will result in a high probability that a pill in the vicinity of a recess will fall into it. The strong short-range magnetic attractive force, which will come into play when a pill settles into a recess, will keep the pill from being removed from the recess by gravity or by another nanopill or by the fluid used to flood the surface with nanopills. The process can be favorably compared to carrier trapping by deep levels in semiconductors, and the probability that a given recess is filled will be one. Once the nanopills are assembled on the circuit wafer, they will be fixed in position using a polymer, which will also fill in any voids on the surface surrounding the pills and planarize the surface. Processing of the heterostructures to convert them into devices and integrate them with the underlying electronics then proceeds, using standard monolithic photolithographic processes.

With the help of Professor Zahn (MIT), we have analyzed the magnetic retention concept. Analysis of pat-

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terned hard magnetic layers, having both in-plane and out-of-plane magnetization, has been performed. The results suggest that both of these magnetization orientations will exert sufficient attractive force on nanopills coated with a permeable magnetic layer. This attractive force is very short range and for separations less than the nanopill thickness, far exceeds the force of gravity. The preliminary models showed an order of magnitude reduction in force using in-plane magnetic fields. However, the fabrication simplicity of in-plane hard magnetic material makes the reduced attractive force manageable.

Experimental work this past year has resulted in the refinement of the nanopill process and the target substrate process. Specifically, a ferromagnetic nickel layer has been successfully integrated with GaAs optoelectronic diode material. This process involves sputter depositing nickel and using a sputter etching technique to directionally etch the nickel layer. The GaAs/AlGaAs diode material is, then, reactively ion etched, using a BCl_3/Ar etch chemistry. The nanopills are, then, freed from their substrate by a backside substrate etch. The pills themselves are protected in a wax. The surrounding wax is dissolved in TCE. The solution is, then, centrifuged and decanted several times. This procedure produces a concentrated pellet of pills to be assembled. Optoelectronic pill yields were improved dramatically using these refined processing techniques.

The target substrate process involves the patterning of a cobalt hard magnetic film that has been deposited on a silicon substrate. Silicon dioxide is, then, deposited on top of this hard magnetic patterned media. Then 5.5 μm deep, 50 um diameter recesses have been reactively etched in this oxide. The etch stops on the patterned cobalt layer. We have also had collaboration with Dr. Chong Tow Chong of the Data Storage Institute in Singapore. Dr. Chong and his staff have prepared 250 period Co/Pd multi-layer films that have been patterned into a 5 μm period stripe pattern. These magnetic films along with the magnetic films fabricated at MIT have been characterized using a vibrating sample magnetometer.

The assembly technique has also been investigated and is being refined. Currently, a recirculating pump is being used in our system, enabling efficient use of pills. Further study of the assembly still needs to be done beyond these initial runs. Magnetic characterization of the magnetic material within the recesses must also be preformed. We will continue to investigate patterning techniques in order to obtain regular patterned material with 5-micron periods at the bottom of existing 5-micron deep recesses. With the successful development of the assembly process, our program will expand to encompass the use of this technology in a variety of applications.

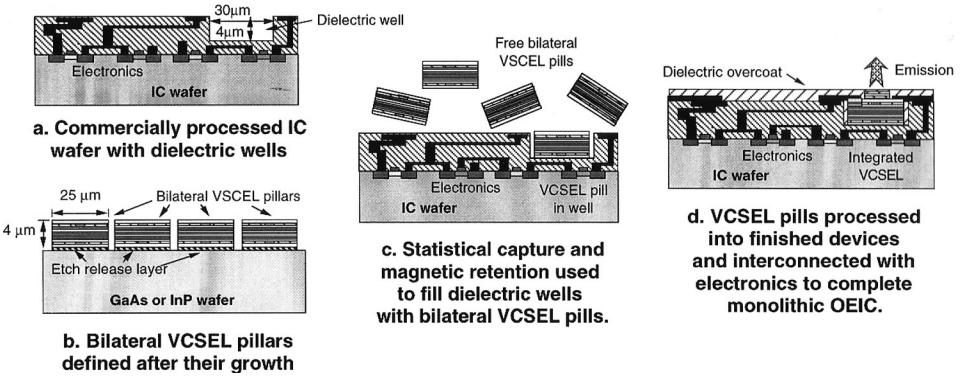

Fig. 32: The MASA process: (a) the processed IC wafer with the recesses prepared, and (b) the p-side down VCSEL wafer with pillars etched in a close-packed array; (c) statistical assembly of the freed nanopills in the recesses on the IC wafer; and (d) after completing device processing and integration.

Large Scale Oxidation of AlAs Layers for Broadband Saturable Bragg Reflectors

Personnel

S. N. Tandon, A. A. Erchack, J. T. Gopinath, T. Schibli, and G. S. Petrich
(L. A. Kolodziejski in collaboration with F. X. Kaertner and E. P. Ippen)

Sponsorship

ONR

Semiconductor saturable Bragg-reflectors (SBRs) are important components for the generation of femtosecond pulses from ultrafast laser systems. In order to create shorter pulses, it is necessary to use mirrors with a wider bandwidth. An alternative to GaAs/AlAs mirrors is to monolithically integrate absorbers onto broadband GaAs/Al_xO_y Bragg-mirrors, created by the steam oxidation of GaAs/AlAs dielectric stacks. The AlAs is converted to Al_xO_y using a wet oxidation system. Figure 33(a) and (b) show top and side views of a 500μm diameter SBR with a GaAs/Al_xO_y mirror stack. The top view shows a fully-oxidized 500μm diameter SBR. However, oxidation at 435°C for 3.5 hours resulted in delamination between the layers as shown in the side view. This delamination is possibly due to a number of factors; one of which is the weak bonding between GaAs and Al_xO_y.

By using low Al content AlGaAs layers instead of GaAs, the bonding between the layers can be strengthened, resulting in a stable mirror stack after oxidation. Figure 34(a) and (b) show top and side views of an SBR design that uses $Al_{0.3}Ga_{0.7}As/Al_xO_y$ layers. The top view shows a fully-oxidized 500μm diameter SBR that has not experienced delamination. The cross-section shows the absorber layers consisting of an InGaAs quantum well between two GaAs buffer layers, and a 7 pair mirror stack of $Al_xO_y/Al_{0.3}Ga_{0.7}As$. For oxidation temperatures between 415°C and 435°C, the mirror stack was successfully oxidized without delamination. At higher temperatures, oxidation of the structure was limited by delamination of the absorber layer at the SBR edges, possibly due to interfacial strain. At 420°C, the mirror was completely oxidized in 4 hours without absorber delamination. Using $Al_{0.3}Ga_{0.7}As$ as the mirror's high index layer strengthens bonding between layers upon oxidation, while preventing significant oxidation of this layer.

In conclusion, saturable absorbers can be integrated with broadband Bragg-mirrors using epitaxial growth and the steam oxidation of AlAs layers. By using low Al content AlGaAs layers as the high index material in the dielectric stack, interfacial bonding is strengthened permitting the stable oxidation of large areas.

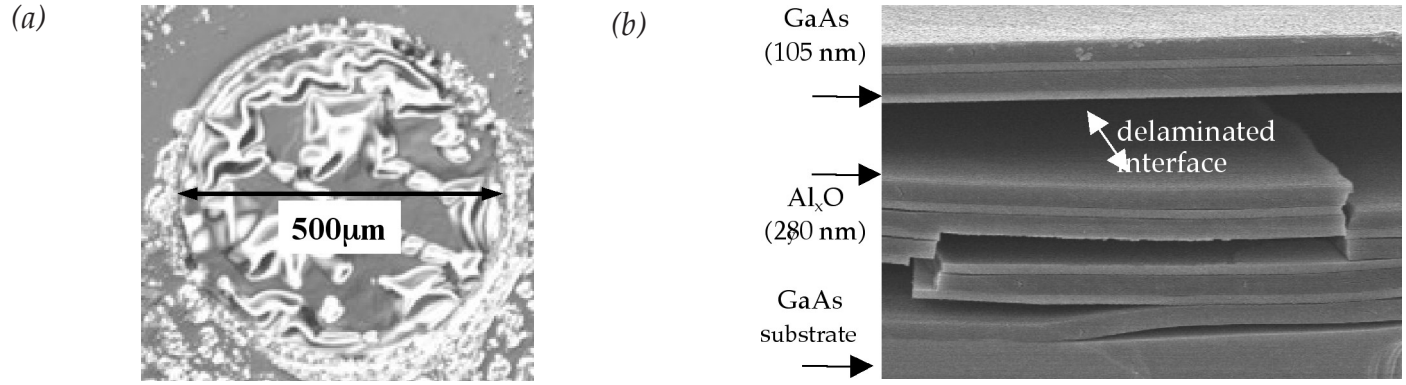

Fig. 33: (a) Top view SEM image of mesa structure oxidized at 435C for 3.5 hours.
(b) Cross-sectional SEM image showing the GaAs/Al_xO_y layers with delaminated interfaces.

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Variable Amplitude Optical Fourier Filtering Using Controlled Thickness Metal Structures

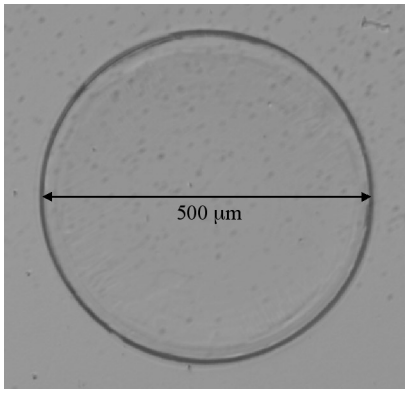
Personnel

H. Iwai, L. DeFlores, G. Popescu, C. M. Fang-Yen, R. R. Dasari, and M. Feld

Sponsorship

NIH and Hamamatsu Co, Japan

(a)



(b)

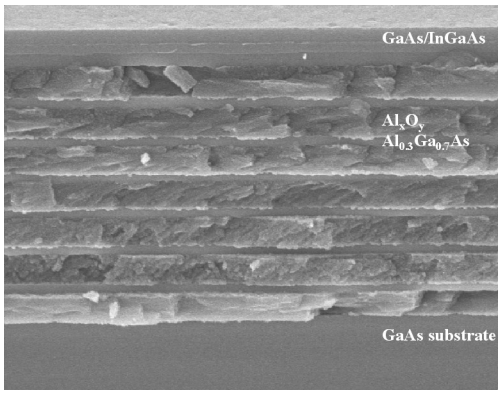


Fig. 34: (a) Nomarski image of fully-oxidized SBR. (b) SEM image of SBR cross-section showing 67 nm GaAs, 40nm InGaAs, 67 nm GaAs absorber with a 7 pair $Al_xO_y/Al_{0.3}Ga_{0.7}As$ mirror stack (~180nm/92nm).

Intense research efforts have been devoted at the Spectroscopy Laboratory towards investigating biological systems at the sub-micron level. Optical interference provides access to the phase information, which in turn allows obtaining information on a much smaller scale than the wavelength of light. In addition, using optical fields of <1mW power, the phase images are obtained in a completely non-invasive fashion. Thus, the technique we are developing has a great potential for the study of living biological samples, such as cultured cells, in their unperturbed environment. This opens the door for a whole new class of biological applications related to the nanometer dynamics of cells and organelles.

An important obstacle in obtaining high-contrast phase images from a confluent monolayer of living cells in the reflection geometry is represented by the strong specular reflection that takes place at the glass surface on which the cells are growing. This specular signal is characterized by a low-spatial frequency and can be labeled as "dc spatial component". This effect has two implications. First, even with AR coated cell wells, this signal is many times stronger than the light scattered from the cells themselves and tends to fill the well depth of the CCD used for imaging. Second, the specularly reflected field and the field backscattered by the cells are coherent and, thus, interfere, producing a total optical field characterized by a new phase, which can be quite different from the phase associated with the sample. In order to alleviate this difficulty, we used a traditional Fourier filtering arrangement to attenuate the spatial dc component. In the Fourier plane of a convergent lens, the specular reflection is focused onto a spot on axis. Thus, using a strong attenuator that covers this area, the dc component can be drastically limited. The obvious choice for the attenuator material was a thin metal film. Aluminum spots of different sizes and thickness have been deposited using the MTL facilities at MIT. The size of the attenuator dictates the "bandwidth" of the spatial filter, while its thickness determines the absolute attenu-

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continued

ation provided. The initial desired attenuation factor was 100 (2 OD), which corresponds to an aluminum film of 35 nm. Various spot diameters, ranging from 25 microns to 150 microns, have been deposited on glass substrates. For a better flexibility, filters of different thickness have also been deposited. Preliminary results show that the quality of the images can be significantly improved by this filtering procedure, but the improvement varies from sample to sample. Thus, further analysis to find the most suitable metal structure properties is to be performed in the near future.

Towards Optical Logic

Personnel

A. Markina, S. J. Rodriguez, and G. S. Petrich
(L. A. Kolodziejski in collaboration with E. P. Ippen)

Sponsorship

DARPA and Lincoln Laboratory

Currently, network services impose bottlenecks on optical fiber communications. While network management complexity increases with the number of wavelengths that the fibers carry, most signal processing operations, such as switching and routing, are still performed electronically after Opto-Electronic (OE) conversion. An average internet packet transverses 16 nodes, with OE-EO conversions for electronic switching at each node. The development of ultrafast all-optical logic would make it possible to avoid multiple opto-electronic conversions and to distribute low-level network functionality in the optical core. High-level slow electronic processing would, then, be pushed to network edges. Desired functionality of all-optical signal processing includes routing, synchronization, and header processing. Developing a family of optical logic with complete Boolean functionality (an optical equivalent of Transistor-Transistor Logic) will be an important step in this direction.

This project includes the design of epitaxially-grown heterostructures that will form the basis for the optical logic, the optimization of passive components as well as the semiconductor optical amplifiers, a discussion regarding the issue of integrating active and passive components together on a single platform, and the design and analysis of an optical logic "unit cell". The proposed optical logic unit cell is based on an integrated Mach-Zehnder interferometer with a Semiconductor Optical Amplifier (SOA) in each arm. The unit cell will be designed for ultrafast 2x2 crossbar operation with an ideal extinction ratio and will be capable of performing a complete set of Boolean operations (AND, INV and XOR). Although the basic implementation does not address the issues of timing, reflections, and separating multiple co-propagating wavelengths, resolving these issues is crucial in order to ensure cascadability of individual unit logic cells.

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A schematic illustration of cascading three Mach-Zehnder interferometer-based "unit cells" together is presented in Figure 35. However, in order to operate properly, this optical circuit requires a number of additional devices. Time delays are used in order to equalize the optical path lengths in order to control the timing; while filters remove unwanted wavelengths, such as those used for the clock signal or control signals. Additionally, wavelength converters can be employed to resolve ambiguity between the data and the control signals. Absorbers can be inserted to eliminate the back reflections into the logic stages. Multiple wavelength clocks/control signals are required for cascading optical logic elements into larger functional blocks.

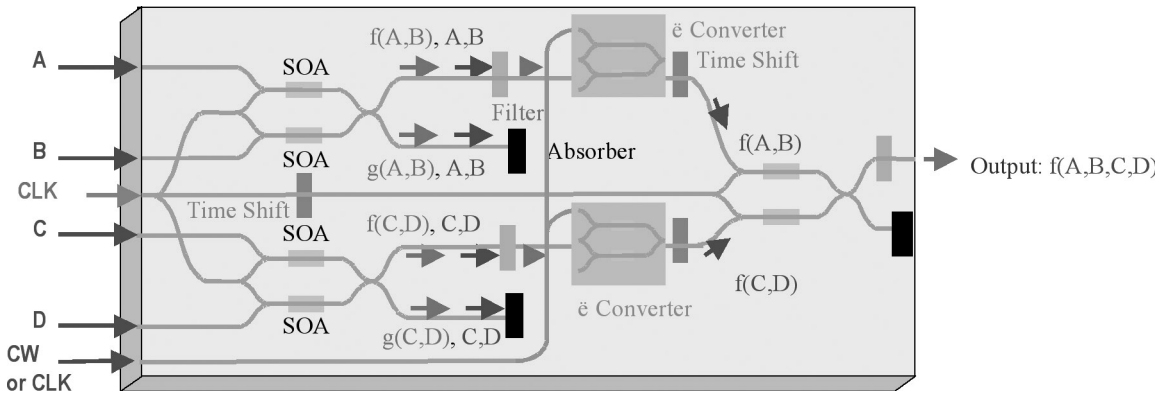

Fig. 35: Three unit cells cascaded on a chip with additional components that enable proper signal processing.

Design and Variation Analysis of an On-Chip Optical Clock Receiver Circuit

Personnel

N. Drego (D. Boning and M. Perrott)

Sponsorship

MARCO Focused Research Center on Interconnect (MARCO/DARPA)

As deep sub-micron CMOS technology continues to scale, decreasing gate lengths and line widths introduce greater variation, propagation delay, crosstalk, and other parasitics into clock distribution networks. Typical H-Tree and other balanced clock distribution schemes are becoming increasingly vulnerable to these effects, particularly to line-width variation and increased propagation delay. Often, buffers are inserted into the network so the total load seen at any segment of the network is decreased. However, buffers cannot compensate for line-width variation and crosstalk. Furthermore, power dissipation in the clock distribution network is becoming a significant fraction of the overall power budget.

An alternative to balanced electrical clock distribution networks is the use of an optical distribution network at the global level (See Figure 36). Light can be distributed to multiple receivers across the chip with low skew. If this light can be efficiently converted to an electrical signal and locally distributed using typical balanced networks, this idea becomes a viable alternative. Variation in the optical network can and will affect the optical signal received at the receiving photodetector. The extent to which this variation will affect the received signal is yet to be fully characterized. Thus, variation-robust optical receiver circuit design and analysis is a critical step toward implementation of on-chip optical clocks.

Two generations of receiver circuits have been designed with the intention of reducing the effects of variation. However, skew remains high (~200ps for a 1GHz clock). A third-generation receiver circuit (See Figure 37) has been designed using a fully-differential architecture. The advantages of differential signaling are primarily common-mode and power-supply rejection, enabling high-bandwidth amplifiers. Mismatch in differential circuits is a large problem in deep submicron processes. As such, offset compensation circuitry is employed to counteract mismatch effects. In addition to replica feedback biasing, a process-compensated current reference developed elsewhere has also been incorporated. Using such techniques, simulated skew due to process variation has been reduced to ~80ps, while clock frequency has been increased to 2GHz. Skew, however, is only one parameter that is characterized in a clock distribution network. Jitter is becoming more significant as clock frequencies scale upward. With circuit techniques such as active deskewing and those mentioned above, jitter is the dominant source of concern in clock distribution today. It is primarily the result of noise, particularly power-supply noise, and is not deterministic. Since noise tends to affect both signals in a differential circuit, it appears as a common-mode variation to differential amplifiers and is rejected. Mismatch can reduce common-mode and power-supply rejection, and thus, noise analysis must be done.

More work remains to be done in studying variation in the optical network as well as determining how further CMOS scaling will affect variation. Furthermore, it remains to be seen whether the optical alternative will prove as advantageous to clock distribution as previously hoped for.

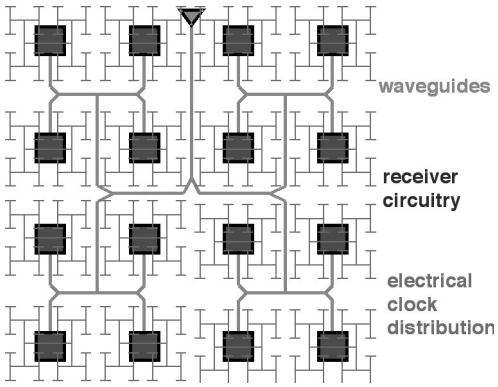

Fig. 36: Global optical clock with local electrical clock distribution.

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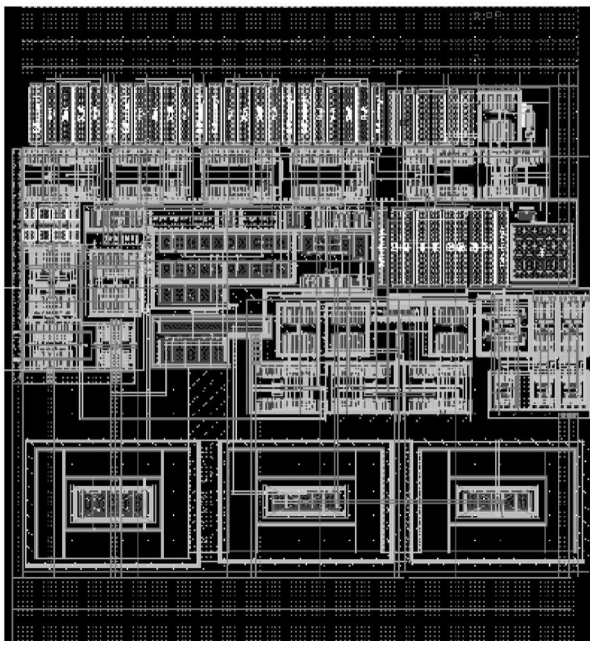

Fig. 37: Third generation clock receiver circuit.

Optical Nano-Electromechanics

Personnel

R.E. Bryant, S. Assefa, P. Rakich, M.L. Povinelli, S. G. Johnson, and G.S. Petrich, (H.I. Smith and L.A. Kolodziejski in collaboration with E.P. Ippen, and J.D. Joannopoulos)

Sponsorship

NSF

A major focus of optical engineering research is to bring optical systems to the large-scale functionality of electrical systems. Striving to reach this objective, a variety of optical devices are currently being developed in an aluminum gallium arsenide III-V material system. The III-V material system is the choice optical bench in which these optical devices are being developed due to advances in material engineering, which allows nanometer precision of high index contrasting layers, ranging from oxidized aluminum arsenide to gallium arsenide. As a result of such precision, a variety of optical manipulations can be carried out with nanometer-sized devices at micron-sized wavelengths. Presently, the focus has been set upon the deployment of nanometer-sized electromechanical-actuated waveguide devices with the prospect of broadening the functionality of integrated optical systems. These devices are termed Optical NanoElectroMechanical devices (ONEM devices).

The ONEM device that is currently being developed, routes optical energy between two adjacent waveguides by lateral coupling after an electrostatic mechanical deflection of the waveguides from an applied voltage. Initially, in a ground state (zero applied voltage), a distance of g_o separates the waveguides. The initial g_o separation is defined using electron beam lithography and is set as to not allow for any lateral coupling between the two adjacent waveguides. A potential difference is then applied to both waveguides, which then reduces the separation of the waveguides.

The initial separation of g_o and the deflected separation of g_{couple} are determined from optical simulations and electromechanical simulations of the two-waveguide system. The separations g_o and g_{couple} are contingent upon the width, thickness, length, and geometry of the two waveguides. Due to the dynamic relation arising from the optics and the electromechanics of the ONEM device, iterations of both types of simulations are being done for a variety of configurations in order to optimize design trade-offs between the optical and electromechanical operations. Figure 38 shows some prototypes of the ONEM device.

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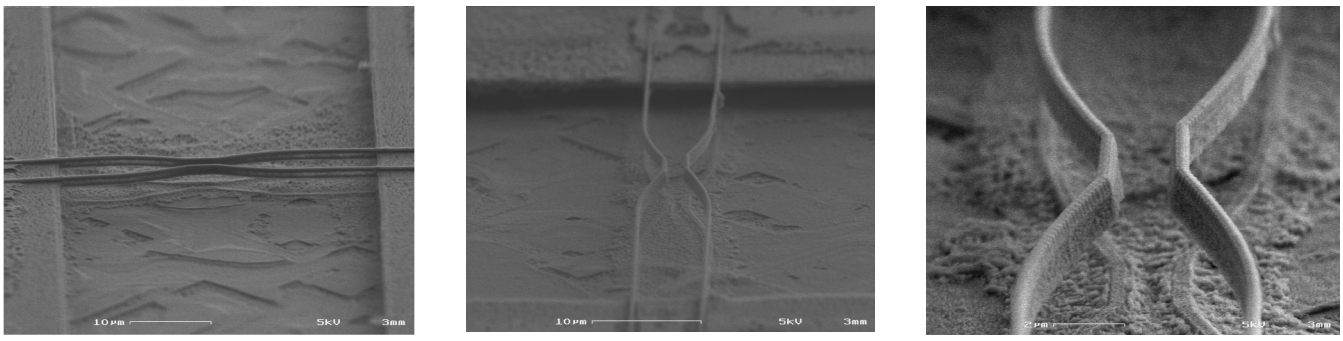

Fig. 38: SEM images of a fabricated ONEMS device in a gallium arsenide-based material system with an exponentially tapered geometry.

Optoelectronic Integrated Circuits for Diffuse Optical Tomography

Personnel

W. Giziewicz (C. G. Fonstad, Jr. in collaboration with S. Prasad and D. Brooks, Northeastern University)

Sponsorship

NSF

Diffuse Optical Tomography (DOT) is an emerging medical imaging technique in which tissue is illuminated by near-infrared light. The multiply-scattered light which emerges is observed with an array of detectors, and then, a model of the propagation physics is used to infer the localized optical properties of the illuminated tissue. The primary absorbers at the wavelengths of interest (approximately from 780 nm to 830 nm), water and both oxygenated and de-oxygenated hemoglobin, all have relatively weak absorption but strong scattering characteristics. The most important current applications of DOT are detection of tumors in breast tissue and imaging of the brain.

The current state of the art in DOT systems involves light sources and detectors coupling to the measured tissue through optical fibers. The resulting systems are quite large and complex. An optoelectronic circuit that would integrate light emission, detection, and signal amplification on-chip would provide a drastic reduction in size, cost, and complexity. It would also open new applications for this technique, potentially including implantable devices. An illustration of how the DOT OptoElectronic Integrated Circuit (OEIC) might be used for subsurface imaging *ex-situ* is presented in Figure 39.

The OEIC will be fabricated in a 1.5 μm low-noise analog process by AMI Semiconductor, through MOSIS. The design of the circuitry is under way, and the layout will be submitted in mid-2003. An important part of the design process was verification of length-scales for the design. On-chip, detector, and emitters will be separated by between one and four optical scattering lengths. Monte Carlo simulations were performed to confirm that a diffuse optical field would be seen at such small separations. The effect of intensity on angle of incidence of the light was also investigated, and it was found that with separations above approximately one scattering length, the diffusely reflected light behaves as desired.

Once returned from fabrication, MBE-grown LEDs will be integrated into the chip using a metal-semiconductor Aligned Pillar Bonding (APB) technique. The devices will be tested with the help of Prof. Brooks at Northeastern University and his collaborators at Massachusetts General Hospital.

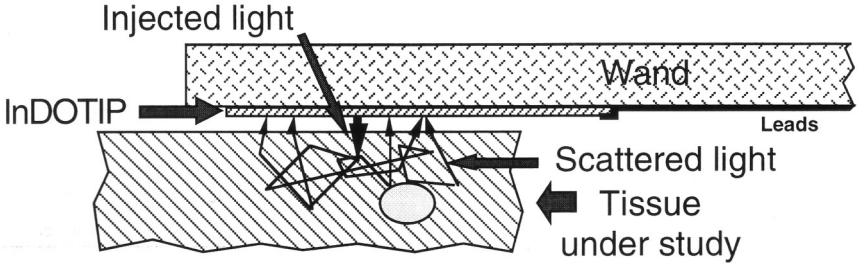

Fig. 39: An illustration of one way the DOT OEIC die might be mounted on the end of a wand and used for DOT subsurface imaging of soft body tissue. In use, each VCSEL is illuminated in turn (the figure shows one turned on) and the pattern of scattered light seen by the detector array is recorded. With this information, an image of the sub-surface structure can be constructed.

Investigation of Dark Line Defects in Semiconductor Laser Diodes

Personnel
K. H. Choy (C. G. Fonstad, Jr.)

Sponsorship
Singapore-MIT Alliance

Heteroepitaxial growth of gallium arsenic (GaAs) and indium phosphide InP-based materials on silicon has been studied for over 20 years. The large differences in lattice constants between silicon and the III-V materials useful for optical devices is the most critical hurdle which has beset the development of this technology. When these materials are epitaxially growth on Si directly, dislocations of great density were found to thread through the films. These dislocations act as sites for nonradiative recombination of electron and holes, lowering the performance of the devices. Furthermore, such electron-hole recombination events drive the expansion of these threading dislocations in the active region of the devices, causing more nonradiative recombination; the devices degrade quickly in the process.

Such degradation also occurs in devices grown on lattice-matched substrates, due to the small but finite number of dislocations inevitably existing there, or induced during the processing of the devices. It has been found that when the GaAs quantum wells in GaAs/AlGaAs lasers are replaced with strained InGaAs ones, this elongation process of the threading dislocations can be significantly retarded, and lifetimes of the devices are enhanced. The origin of this retardation is still in dispute, and it is not clear to what extent this technique can assist the epitaxial growth of III-V materials on silicon, when the density of dislocations is very large.

The core of this thesis will be to carry out a systematic study of this effect; (1) by deliberately generating a known density of dislocations in layers grown on GaAs substrates, (2) by controlling the amount of strain in InGaAs quantum wells through which these dislocations will thread, and (3) by observing their degradation. The structures will be grown in a solid source molecular beam epitaxial system. They will be started with thin layers of mismatched materials that generate approximately known amounts of threading dislocations. Then, InGaAs relaxed graded buffers with different final compositions will be grown. The subsequent parts of the growth, including the claddings of the lasers, will be grown lattice matched to the top of the graded buffer layers. The InGaAs quantum wells, however, will all have identical composition, regardless of the lattice constants of the claddings sandwiching them. By doing so, the quantum wells will be set in different states of strain, depending on the differences between the lattice constants of the quantum wells and those of the final compositions of the graded buffers, which will be different from sample to sample. The goal is to isolate and investigate the factors contributing to the significant suppression of laser degradation, resulting from the use of strained InGaAs quantum wells. Hopefully, it will also add to the understanding of the laser degradation process itself.

Compact Optoelectronic Neural Co-processor Project

Personnel
B. Rudlinger (C. G. Fonstad, Jr. and C. Warde)

Sponsorship
National Science Foundation

We have just initiated a research program to develop algorithms and architectures, and to fabricate and demonstrate a rugged, compact, modular, versatile, Optoelectronic, Integrated-Circuit (OEIC) neural network and fuzzy logic co-processor system that would work in conjunction with the standard PC microprocessor. This OEIC co-processor will perform sophisticated parallel and/or fuzzy processing operations more efficiently than the standard PC microprocessor. The proposed OEIC co-processor will be about the size of a CD-ROM drive, and thus, would fit easily inside the case of a conventional personal computer. Another important goal of the program is that this compact OEIC co-processor be amenable to mass manufacturing.

The key feature (and advantage) of the proposed class of OEIC co-processors is that they combine the parallel processing and longitudinal (inter-plane) free-space communication strengths inherent in optics with the transverse (intra-plane) communication and computation strengths of electronics to realize extremely powerful and versatile machines. This work distinguishes itself from earlier attempts in that: (1) for the first time in history all of the needed components are available with sufficient performance to demonstrate the co-processor, and (2) we have a unique design and packaging technology that takes care of the alignment, compactness, and ruggedness issues.

To demonstrate the feasibility of the co-processor, the proposed hardware development tasks include: (1) design, fabrication, and characterization of novel 2-D arrays of GaAs-SOS (silicon-on sapphire) OEIC cascadable smart pixels with a detector, integrated-circuit logic, and a light source in each pixel (Resonant Cavity Light-Emitting Diodes (RCLEDs) in the first two years of the program, and Vertical-Cavity Surface-Emitting Lasers (VCSELs) replacing the RCLEDs in the third year), (2) design, fabrication, and characterization of novel reconfigurable optical interconnection elements based on arrays of Bragg-holographic phase gratings, (3) alignment (with the help of a mask aligner) and gluing of all the components of the co-processor (OEICs, interconnection elements, and output photodetector array) together into a rugged, compact, modular multi-layer sandwich configuration so as to permanently solve any micro-optics alignment problems, and (4) characterization of the resulting high-speed, multilayer optoelectronic co-processor.

In addition to the above-mentioned fabrication tasks, another early focus of the program will be on neural network configurations. We will carry out the following theoretical, modeling and simulation tasks related to this aspect of the program: (a) develop algorithms, especially those suitable for programmable nearest-neighbor interconnections (e.g. pulse-coupled networks) to solve a large class of multi-dimensional information processing problems, and (b) explore the application of these novel co-processors to three different types of problems: (i) associative-memory-based pattern recognition, (ii) medical image segmentation, and (iii) fusion of a set of low-contrast spectro-polarimetric infrared images into a single high-contrast image.

Terahertz Quantum Cascade Lasers

Personnel

B. Williams, H. Callebaut, S. Kumar, and S. Kohen (Q. Hu in collaboration with Dr. J. Reno at Sandia National Lab)

Sponsorship

National Science Foundation, NASA, and AFOSR

Semiconductor quantum wells are human-made quantum mechanical systems in which the energy levels can be designed and engineered to be of any value. Consequently, unipolar lasers based on intersubband transitions (electrons that make lasing transitions between subband levels within the conduction band) were proposed for long-wavelength sources as early as the 1970s. However, because of the great challenge in epitaxial material growth and the unfavorable fast nonradiative relaxation rate, unipolar intersubband-transition lasers (also called quantum-cascade lasers) at mid-infrared wavelengths were developed only recently at Bell Laboratories. This achievement paved the way for development of coherent laser sources at customized frequencies ranging from THz to near-infrared. However, compared to the infrared QCLs, THz QCLs at much longer wavelengths face unique challenging issues. First, the energy levels corresponding to THz frequencies (1 THz = 4 meV) are quite narrow, thus, it is very challenging to design quantum well structures for selective injection to the upper level and selective depopulate electrons from the lower level. The requirements for fabrication of such quantum-well structures with adequate accuracies are also demanding. Because of the narrow separation between subband levels, heating, and electron-electron scattering will have a much greater effect. Also, the small energy scales of THz photons make the detection and analysis of spontaneous emission (a crucial step toward developing lasers) quite difficult. Second, mode confinement, which is essential for any laser oscillation, is difficult at longer wavelengths. Conventional dielectric-waveguide confinement is not applicable because the evanescent field penetration, which is proportional to the wavelength and is on the order of several tens of microns, is much greater than the active gain medium of several microns. Recently, we have made breakthroughs in developing quantum-cascade lasers at 3.4 THz (corresponding to 87 μm wavelength), and more recently, at an even longer wavelength of 100 μm. In both laser structures, population inversion was achieved with resonant phonon scattering for the depopulation of the lower level. Key results are summarized in the following sections.

THz quantum cascade lasers based on resonant phonon scattering for depopulation

The direct use of LO-phonon scattering for depopulation of the lower state offers several distinctive advantages. First, when a collector state is separated from the lower state by at least the phonon energy $h\omega_{LO}$, depopulation can be extremely fast, and it does not depend much on temperature or the electron distribution. Second, the large energy separation provides intrinsic protection against thermal backfilling of the lower radiative state. Both properties are important in allowing higher temperature operation of lasers at longer wavelengths.

The present design combines advantages of our two previously investigated THz emitters. As shown in Figure 40, the radiative transition between levels 5 and 4 is spatially vertical, yielding a large oscillator strength. The depopulation is highly selective, as only the lower level 4 is at resonance with a level 3 in the adjacent well where fast LO-phonon scattering takes place. The four-well structure inside the dashed box is one module of the structure, and 175 such modules are connected in series to form the quantum cascade laser.

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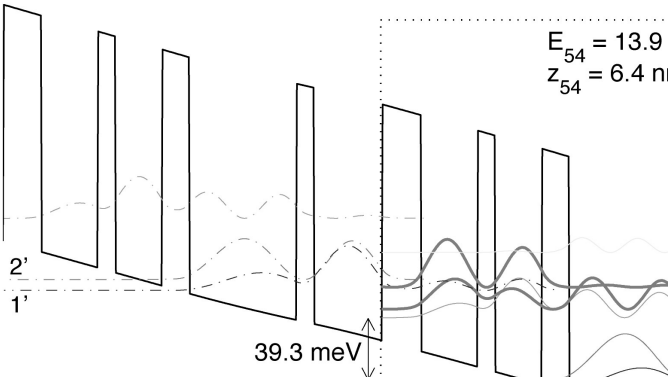
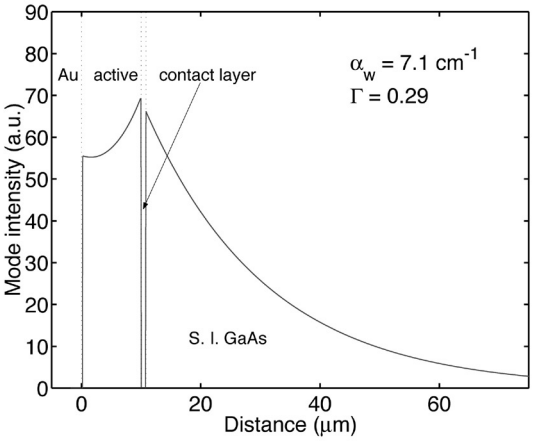


Fig. 40: Conduction band profile calculated using a self-consistent Schrödinger and Poisson solver (80% conduction band offset) biased at 64 mV/module. Beginning with the injector barrier, the layer thickness in Å are 54/78/24/64/38/148/24/94. The 148-Å well is doped with Si at 1.9×10^{16}/cm^3, yielding a sheet density of 2.8×10^{10}/cm^2.

Mode confinement in this laser device was achieved using a surface plasmon layer grown under the active region. The schematic of the device structure and the calculated mode profile and waveguide loss are shown in Figure 41. The calculated waveguide loss of 7.1 cm^{-1} and mode confinement factor $\Gamma \approx 29\%$ are quite favorable compared to the calculated gain of our laser device.

Lasing at 3.437 THz (λ = 87.2 μm) was obtained in this device at a threshold current density of 840 A/cm^2 at 5 K. Typical emission spectra above threshold are shown in Figure 42. The emission frequency corresponds to an energy of 14.2 meV, close to the calculated value of 13.9 meV. For much of the bias range, the emission is dominated by a single mode, although the spectrum shifts toward a higher mode with increasing bias due to the Stark shift.

Measured optical power versus current (*P-I*) curves at low duty cycle are plotted in Figure 43(a). Lasing is observed up to 64 K (72 K in a more recent measurement) with a power level of 25 μW, compared to the 2.5 mW observed at 5 K. Figure 43(b) displays the voltage versus current, as well as several *P-I* curves taken for pulses of increasing width. Even at a high 50% duty cycle, the laser still produces 0.5



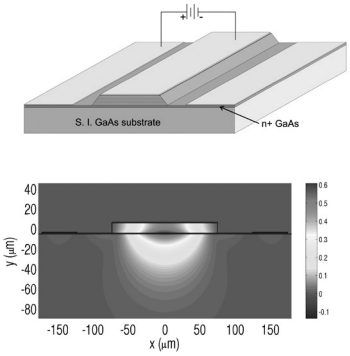


Fig. 41: Schematic of the THz laser ridge structure, calculated two-dimensional mode profile using FEMLAB (on the left), and one-dimensional mode profile, confinement factor, and waveguide loss (on the right).

continued

continued

mW of peak power, indicating its robustness. The result of this initial success is quite promising. We are confident that improvement in injection efficiency, mode confinement, and fabrication process will readily lead to CW operation of THz quantum cascade lasers at liquid-nitrogen or higher temperatures, and at even longer wavelengths where electronic devices, such as transistors, have been the only functional solid-state devices. Clearly, such a development will have a qualitative impact on science and technology in the THz frequency spectra.

THz quantum cascade lasers using metal waveguides for mode confinement

After our initial success in the development of 3.4-THz quantum cascade laser, one of the improvements was made in the mode confinement. As shown in Figure 41, the mode confinement using surface plasmon layer yields a relatively low mode confinement factor of $\Gamma \approx 0.29$. This mode confinement is sufficient for lasing at 3.4 THz. However, as we are developing even longer wavelength quantum cascade lasers, the mode confinement will become much worse or even unconfined at frequencies lower than 2 THz for the carrier concentration in our laser structures. An alternative method for mode confinement is to use metal waveguides. As shown in Figure 44(a), the mode is now tightly confined between the top and bottom metal contacts, yielding a confinement factor close to 100%. Figure 44(b) shows the process of wafer bonding and selective etching to fabricate such a metal waveguide structure. This process was developed by a former student Bin Xu in 1997.

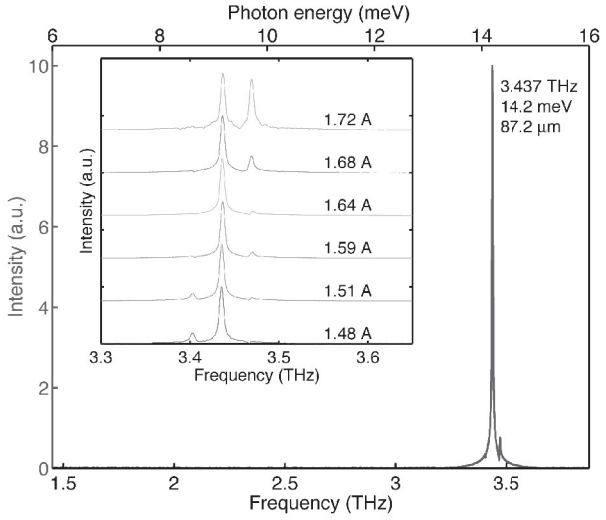


Fig. 42: Emission spectrum above threshold biased at 1.64 A at 5K heat sink temperature. The inset shows an expanded view of spectra at various bias points, offset for clarity.

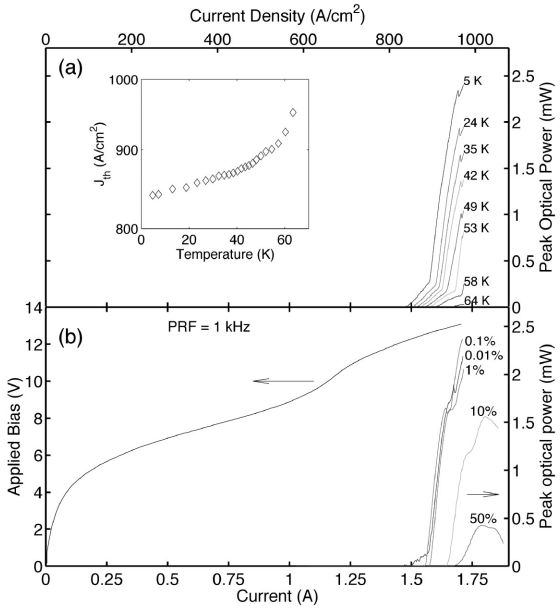


Fig. 43: (a) Emitted light versus current at various temperatures. The inset is a semi-log plot of the threshold current density J_{th} as a function of temperature. (b) Applied bias voltage and peak optical power versus current, collected at various duty cycles.

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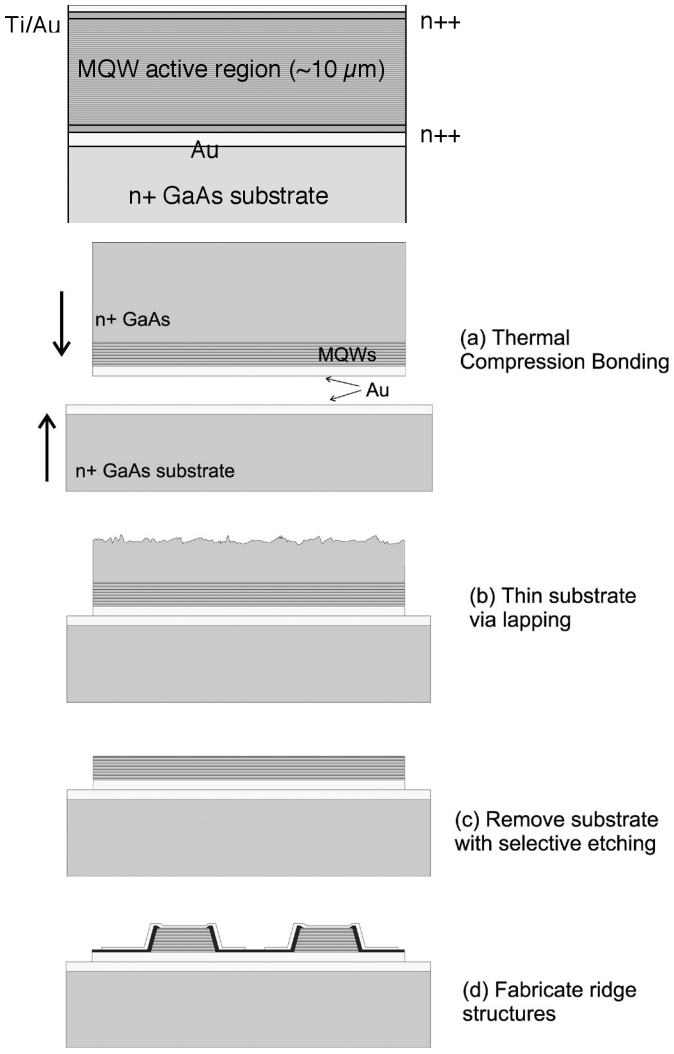

Fig. 44: Top: Side view of a metal waveguide structure for THz mode confinement. Right: Fabrication process of the metal waveguide structures.

Using this novel mode confinement structure, we have recently developed a quantum cascade laser at 100-μm wavelength. The power-current relation and emission spectrum of this laser are shown in Figure 45. The laser operates up to 70 K, and the wavelength of 100 μm is among the longest achieved in QCLs. This is the first successful demonstration of using metal waveguides for mode confinement at THz frequencies. In fact, devices fabricated from exactly the same wafer but using the surface plasmon layer for mode confinement did not achieve lasing, which demonstrates a clear advantage of the metal waveguide over that of surface plasmon layer in mode confinement. As we proceed towards even longer wavelengths, to approach the ~300-μm range where electronic devices such as transistors function, this advantage will become more significant and even crucial.

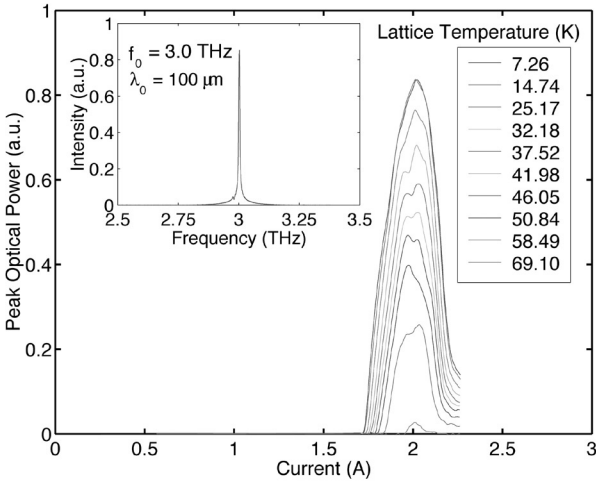

Fig. 45: Power-current relations of a laser device using metal waveguide for mode confinement, measured at heat sink temperatures up to 70 K. Inset: Emission spectrum taken at a bias voltage 11.4 V and current 1.8A. The spectrum is single-mode, and the wavelength is among the longest achieved in QCLs.

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Analysis of transport properties of THz quantum cascade lasers

Even though mid-infrared and THz quantum cascade lasers operate on the same principle, that is, intersubband transition in semiconductor heterostructures, they show a qualitative difference in the dynamics of electron transport. For mid-infrared QCLs, the subband separations exceed the LO-phonon energy $h\omega_{LO}$, and electron transport is dominated by LO-phonon scattering. For THz QCLs, many subband separations are smaller than $h\omega_{LO}$, only the high-energy tail of a hot electron distribution is subject to the LO-phonon scattering, which results in a significantly higher temperature sensitivity for the electron transport and a far greater importance of electron-electron (e-e) scattering. The long delay in the development of THz QCLs is testimony to the difficulty of achieving population inversion involving these complicated transport mechanisms. It is, thus, important to quantitatively model these transport processes to extend the operation of THz QCLs to broader frequency ranges and higher temperatures.

Our transport analysis is based on Monte Carlo (MC) simulations, which have been used to analyze and design mid-infrared and THz QCLs. Compared to conventional rate-equation analysis, the MC method is especially useful for THz QCLs, as it does not rely on a specific model for carrier distributions and can easily handle temperature- and density-dependent scattering times. Figure 46 illustrates the flow chart of our Monte Carlo simulation scheme. It follows a conventional scheme for an ensemble of particles, in our case 10^4 particles, with a focus on e-e and e-phonon interactions involving the electrons in one module of the device under study. An electron that scatters out of a module is reinjected with identical in-plane *k*-vector into a subband equivalent to its destination subband, in accordance with the spatial periodicity of QCLs.

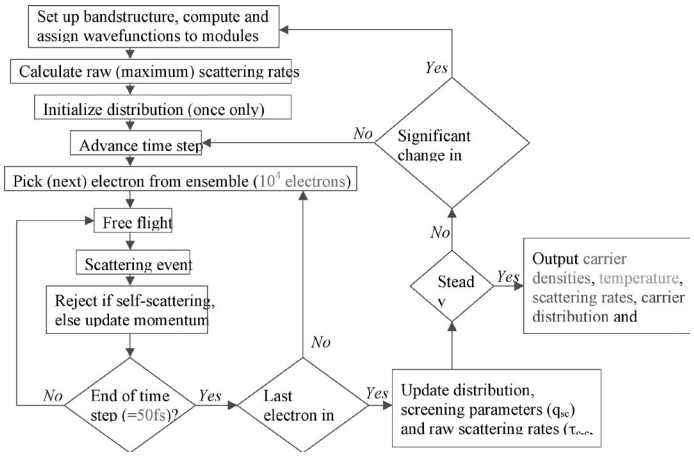

Fig. 46: Flow chart of our ensemble Monte Carlo simulation scheme.

The results of the Monte Carlo simulations, focused on the 3.4-THz laser structure shown in Figure 41, are summarized in Figure 47. All simulations assumed a lattice temperature of 25 K, corresponding to a 10 K heat sink temperature. In Figure 47(a), the calculated I-V relation qualitatively resembles that of measured one, with the calculated peak current density is noticeable lower. This discrepancy suggests the scattering processes in the MC simulations are slower than in actual devices. The slower scattering processes yielded a higher calculated peak gain than inferred from experiments, as shown in Figure 47 (d). The two horizontal lines are calculated total cavity losses with one facet Au coated and without any facet coating. Our device lased only with one facet coating, thus the two lines define the range of material gain in our laser device. The qualitative agreement between the MC and experimental results indicate the usefulness of MC simulation as a design tool. The discrepancy requires further investigation of all important scattering channels.

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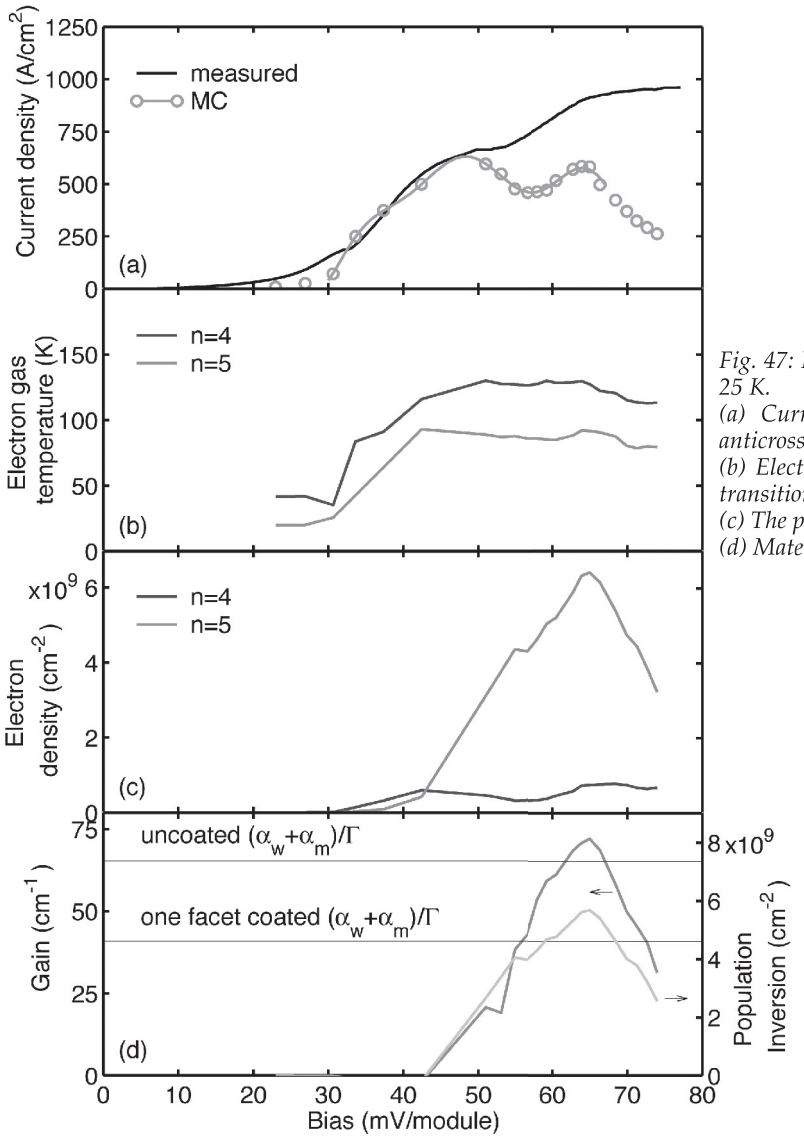


Fig. 47: Key results of the MC simulation for a lattice temperature of 25 K.
(a) Current density for a range of bias voltage. The injection anticrossing occurs at 65 mV/module.
(b) Electron temperature for the subbands involved in the radiative transition, n = 4 and n = 5.
(c) The population density in n = 4 and n = 5.
(d) Material gain and population inversion for different biases.

Development of Bipolar Cascade Lasers

Personnel

R. D. Williams, A. Markina, and G. S. Petrich (R. Ram and L. A. Kolodziejski)

Sponsorship

DARPA-OptoCenter

The bipolar cascade laser design aims to combine two or more lasing active regions in epitaxial series. Previous work realized room temperature, continuous wave, and bipolar cascade lasers at 980 nm. Currently, the work has focused on transitioning the design from using quantum wells that emit at 980 nm to quantum dots that emit at 1300 nm, as well as, improving the characteristics of the reverse-biased tunnel junction which connects the consecutive active regions.

As 1300 nm is an important wavelength in telecommunications, recent work has focused on obtaining InAs quantum dots on GaAs substrates. InAs quantum dots extend the range of achievable emission wavelengths of GaAs-based active devices well into the functional telecommunications regime. Furthermore, quantum dots allow for the realization of ultra-low laser threshold currents, narrow emission spectra, improved gain properties, and increased temperature stability. Photoluminesence studies have shown strong emission between 1250-1300 nm. Careful control of the growth conditions, such as the substrate temperature and deposition rate, has allowed precise control over the emission wavelength and intensity. Atomic force microscopy has been used to confirm the presence of quantum dots and has shown their average diameter to be around 20 nm as shown in Figure 48.

The introduction of indium into the GaAs tunnel junction material is theorized to improve the differential resistance of the junction and thereby, increase the tunneling current, resulting in improved quantum efficiency for the laser. Samples have been grown by gas source molecular beam epitaxy and processed to examine the effects of indium-incorporation and are currently undergoing electrical testing. Bipolar cascade lasers using 980 nm emitting quantum wells have been integrated with indium containing tunnel junctions and are undergoing processing.

The current aim of the project is to produce a bipolar cascade laser on a GaAs substrate containing quantum dot active regions and operating at 1300 nm. Laser structures have been grown and are currently undergoing processing and testing.

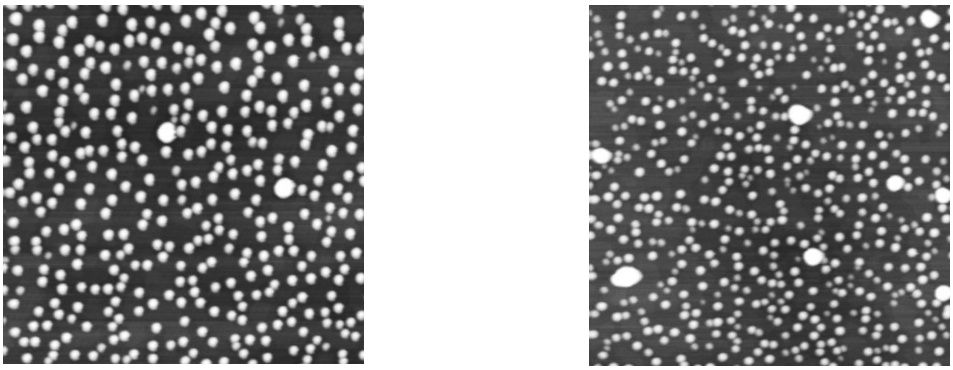


Fig. 48: Atomic force micrographs of 1 μm x 1 μ m square areas. a) With the arsine flow =0.1 sccm, the density of InAs quantum dots is 4 x 10^{10} cm^{-2} and the average diameter is 23 nm. b) With the arsine flow =1.0 sccm, the density of InAs quantum dots is 6 x 10^{10} cm^{-2} and the average diameter is 21 nm.

Design and Fabrication of a Superprism Using Two Dimensional Photonic Crystals

Personnel

S. Tandon, C. Luo, M. E. Walsh, and G. S. Petrich (L. A. Kolodziejski, H. I. Smith, and J. D. Joannopoulos)

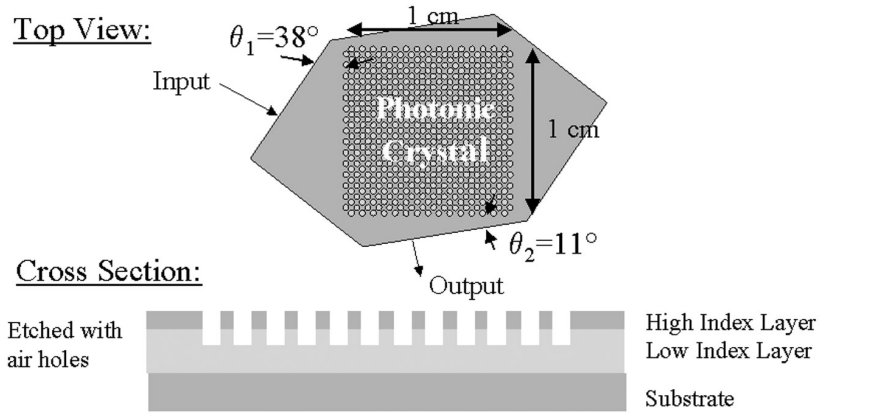
Sponsorship

DARPA/Rockwell Scientific Corp.

A superprism is an optical device similar to a conventional prism but with two enhanced properties: (1) super-dispersion and (2) ultra-refraction. Just as a conventional prism separates light into its component wavelengths, a superprism separates these wavelengths over wider angles--termed "super-dispersion." A superprism can magnify the angle of propagation of a single wavelength of light to steer the beam over wide angles--termed "ultra-refraction." Photonic crystals are responsible for the superprism effect. Superprism effects would be useful in a number of applications, ranging from enhanced devices for Wavelength-Division Multiplexing (WDM) to a new class of ultra-refractive optical elements for beam manipulation.

Our superprism consists of a 2D photonic crystal with a square lattice of cylindrical air holes in a high index material such as silicon or gallium arsenide. The top view schematic of the device shape is shown in Figure 49. The device is hexagonal shaped with the Photonic Crystal (PC) occupying a square region in the center. The initial design has focused on realizing ultra-refraction such that an input angular sweep of approximately +/- 2 degrees is amplified to about +/- 30 degrees at the output for a wavelength of 3.2 μm. A thick low-index layer is used to minimize radiation loss into the high index substrate.

The feature sizes of the photonic crystal can be scaled depending on the wavelength of operation as shown in Figure 49. Our desired wavelengths of 3.1μm and 1.55μm imply hole lattice constants of 750nm and 372nm, and hole radii of 300nm and 150nm. The total thickness of the device (excluding substrate) is about 3.5 microns (460nm GaAs, 3μm Al_xO_y), while the top surface will have an area somewhat larger than 2x2cm.



	GaAs Substrate		Si Substrate	
	λ=~3.1 μm	λ=~1.55 μm	λ=~3.1 μm	λ=~1.55 μm
PBG Lattice Constant	750 nm	372 nm	750 nm	372 nm
PBG Hole Radius	300 nm	150 nm	300 nm	150 nm
High Index Thickness	450 nm	223 nm	700 nm	205 nm
Low Index Thickness	3000 nm	1500 nm	3000 nm	3000 nm

Fig. 49: Superprism device design showing top and side views of the device.

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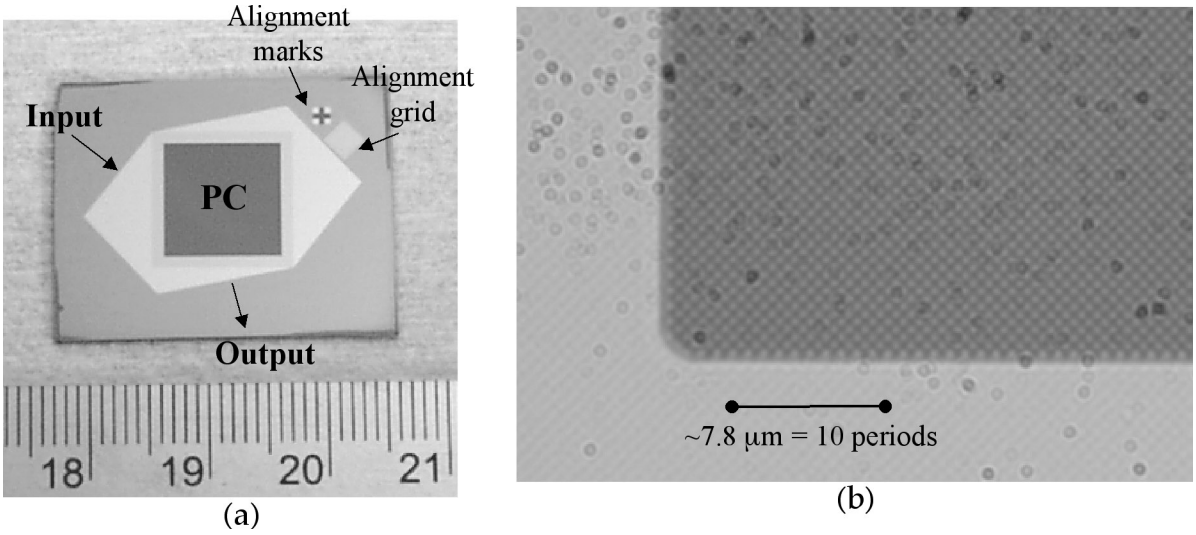

Fig. 50: (a) Photograph showing a top view of the superprism hard mask layers on a silicon substrate. (b) Microscope image of the corner area of the photonic crystal region shown in Fig 48(a). The defects in the photograph are due to dust particles in the microscope optics that could not be readily removed.

The hexagonal device shape is patterned using photolithography, while the photonic crystal holes are patterned using interference lithography and a tri-layer resist process. After each lithography step, patterns are etched into hard-mask layers via Reactive Ion Etching (RIE). The fully-patterned hard-mask layers are then used to etch the substrate material via another RIE step. Figure 50(a) is a photograph of the patterned hard-mask layers on a silicon substrate. Two hard-mask layers have been used: 50nm chromium on top of 250nm HSQ (spin-on oxide). The chromium layer is patterned with the superprism hexagonal shape, while the open square area is patterned with the ~780nm period photonic crystal in HSQ. The diffraction pattern from the PC can be seen as a blue streak across the square area.

Figure 50(b) shows a microscope image (100x magnification) of the corner region of the photonic crystal area. The square grid of the PC is rotated 45 degrees with respect to the square region. The alignment accuracy between the photonic crystal orientation and the square region is critical for superprism performance. Figure 50(b) shows how a line of PC holes is aligned to the square edge with accuracy of less than one degree, thus, achieving our required tolerance.

Future work will include: calibrating the photonic crystal hole size during the interference lithography, finding a better hard-mask layer than chromium (which leaves behind post-wet-etch residue), and employing reactive ion etching of the silicon substrate material.

Coupling into Photonic Crystal Waveguides

Personnel

S. Assefa, P. Rakich, P. Bienstman, S. G. Johnson, and G. S. Petrich (J. D. Joannopoulos, L. A. Kolodziejski, E. P. Ippen, and H. I. Smith)

Sponsorship

Center for Material Science and Engineering and NSF

Large-scale photonic integrated circuits require a capability of guiding light around sharp bends with a radius of curvature on the order of the wavelength. In conventional index-guided waveguides, light is confined as a result of total internal reflection at the interface between the high-refractive-index waveguiding layer and its low index surroundings. However, conventional high-index-contrast waveguides are susceptible to large optical losses as the bend's radius of curvature decreases. Photonic crystals (PCs), which consist of a periodic arrangement of high and low-index dielectric material, have been proposed as a potential solution for guiding light around corners, including 90° bends, with near perfect transmission.

The 2D photonic crystal consists of an array of cylindrical rods of high-dielectric material above a low dielectric material. Introducing a line defect, such as a row of smaller radius cylinders, into the 2D photonic crystal results in a linear waveguide. The forest of periodic dielectric rods surrounding the line defect creates a Photonic Band Gap (PBG), i.e. a range of frequencies over which light cannot propagate. Thus, an optical signal with a frequency inside the PBG has its energy confined within the line defect and becomes evanescent into the photonic crystal. The radius of the cylinders in the line defect remains large enough to provide index guiding in the third dimension (normal to the plane of periodicity). The localization of a mode inside the line defect can be utilized to guide light around sharp corners. This is illustrated in Figure 51.

The practical use of photonic crystal waveguides is limited due to the poor coupling efficiency between the photonic crystal waveguide, and conventional index-guided input and output waveguides. Coupling poses a challenge because the photonic crystal waveguide exhibits a significantly different mode profile and propagation mechanism compared to traditional waveguides that use index confinement. In the conventional waveguide, the field has only forward propagating components, while the field in the photonic crystal waveguide has both forward and backward propagating components. Furthermore, guiding in the conventional waveguide is in high index surrounded by low index; in the photonic crystal, guiding is in low index surrounded by two photonic crystal "mirrors".

Figure 52 compares three different designs for coupling into the photonic-crystal waveguide. The design in Figure 53(a) suffers from Fabry-Perot reflection at the edges of the photonic crystal region, which makes the transmission of the waveguide dependent on the waveguide length. By tapering the end of input and output index waveguides as shown in Figure 53(b), the reflection can be somewhat reduced. In the third design, the input waveguide is adiabatically converted into a strongly Coupled-Cavity Waveguide (CCW).

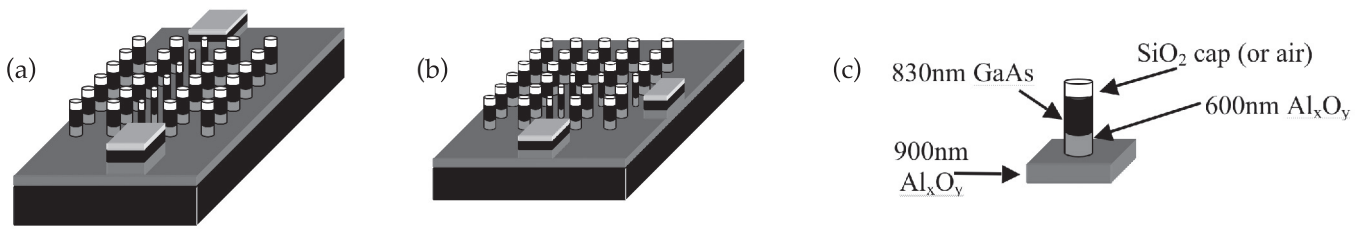

Fig. 51: (a) Schematic of a linear PC waveguide. (b) Schematic of a 90° bend PC waveguide. (c) Schematic of a cylindrical pillar structure. For the bulk photonic crystal, the pillar diameter is 300nm; for the defects, the diameter is 250nm.

continued

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This adiabatically transforms the forward propagating component of the field into both forward and backward propagating components before reaching the photonic crystal. Also, the "cladding" is introduced slowly from the edge, thereby adiabatically transforming the mode from high-index guiding to gap guiding. 2D simulations show that this coupling scheme results in almost 100% transmission through the photonic crystal waveguide.

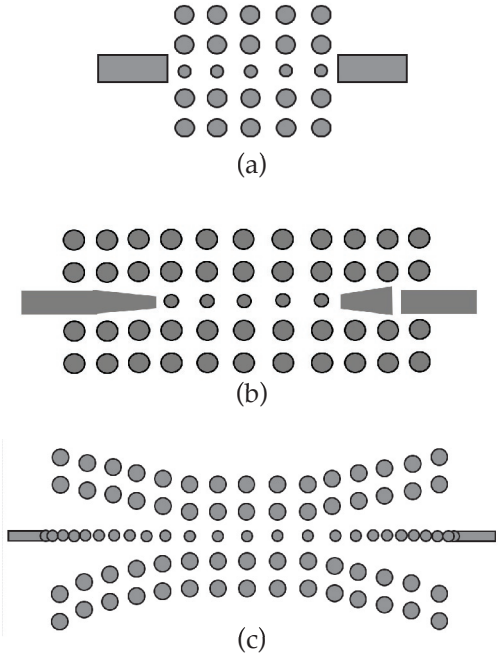

Fig. 52: a) Schematic of coupling from untapered dielectric waveguide. b) Schematic of coupling from a tapered dielectric waveguide. c) Schematic of adiabatic transition from a dielectric waveguide into strongly coupled cavities and tapered cladding.

The cylindrical rods of the photonic crystal consist of a high-index, 830nm epitaxial GaAs layer sandwiched between 100nm-thick SiO_2 cap layer and a 600nm-thick low-index Al_xO_y layer. An additional 900nm thick Al_xO_y layer is below the cylindrical rods, isolating the GaAs guiding layer from the GaAs substrate. The heterostructure is grown using gas-source molecular-beam epitaxy on a (100) GaAs substrate. The Al_xO_y is initially grown epitaxially as $Al_{0.9}Ga_{0.1}As$ and subsequently, converted (See Figure 52).

The fabrication process commences by sputtering 400nm thick SiO_2 on the sample. Next, the waveguide and photonic crystal are defined using direct-write scanning-electron-beam lithography. Each sample is coated with polymethylmethacrylate (PMMA) electron beam resist, and each cylinder is defined by exposing a square pattern (See Figure 53). The finite width of the beam rounds-off the corners of each square yielding a circular hole upon development. Simulations show that the largest band gap is obtained from a periodic arrangement of rods with diameter of 300nm. Exposure-dose experiments are done to find the optimal parameters for the exposures. A dose of 536 mC/cm^2, current of 250pA, and clock frequency of 0.20 MHz gave hole diameters close to the desired values. The input and output coupling waveguides and different-sized arrays of holes are written by stitching together 250μm fields.

A 50nm-thick nickel film is evaporated on the sample after the PMMA is developed, and a liftoff process is performed. The pattern is transferred to the SiO_2 by Reactive-Ion Etching (RIE) in a CHF_3 plasma after which the nickel mask is removed using nickel etchant. Using the SiO_2 mask, the cylindrical rods are created by etching the GaAs and the AlGaAs to a total depth of 1.5 μm in a BCl_3/He plasma. Experiments were done using various metal masks as an alternative to the SiO_2 mask. However, the metal masks sputtered or degraded during the long duration of the GaAs/AlGaAs etch. Next, each sample is lapped and cleaved in order to create a smooth input facet to promote the efficient coupling of a test signal of 1.55μm wavelength. Finally, the AlGaAs is transformed into Al_xO_y using a wet thermal oxidation process.

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Currently, the photonic crystal devices are being tested. The band gap is being mapped first by varying the number of columns in a bulk photonic crystal. Also, the three coupling mechanisms are being compared to confirm the best transmission through the photonic crystal waveguide (See Figure 54).

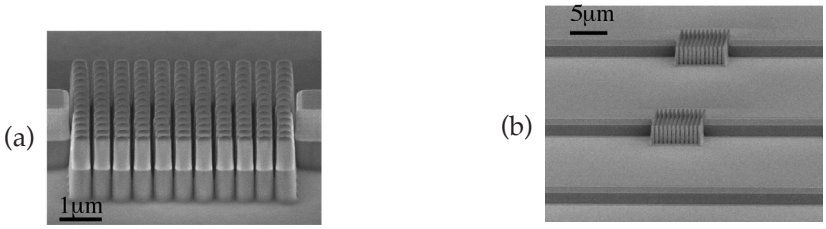

Fig. 53: a) Side view SEM of a bulk photonic crystal etched in GaAs/AlGaAs using BCl_3/He plasma. The AlGaAs is oxidized into Al_xO_y. The period is 500nm and the diameter of the pillars is 300nm. The input and output waveguides are 1.5μm wide. b) Photonic crystal devices on a single chip. The design contains a straight waveguide for normalization purposes.

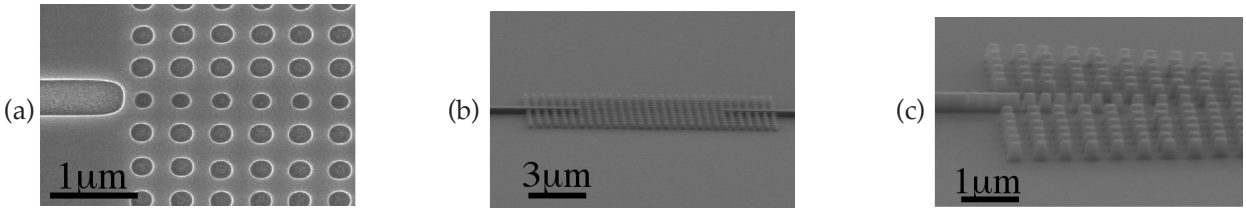

Fig. 54: a) Top view SEM of coupling design from Figure 51(a) after e-beam lithography in PMMA. The bulk photonic crystal has hole diameter of 307nm, while the defect has diameter of 244nm. b) Top view SEM of coupling designs from Figure 51(b) after SiO_2 etch. c) Top view SEM of coupling design from Figure 51(c) after SiO_2 etch.

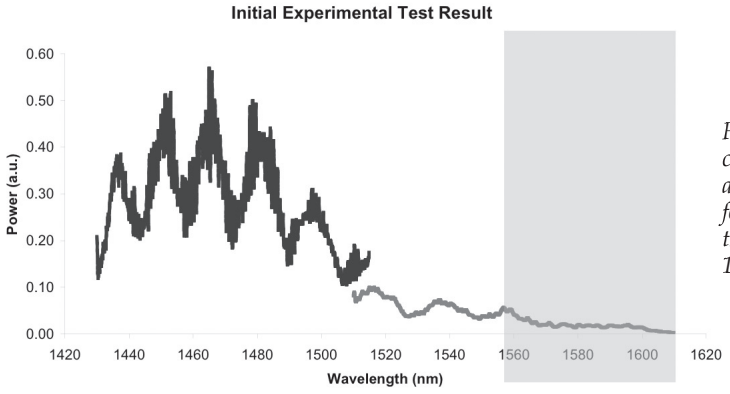

Fig. 55: Initial experimental data of a bulk photonic crystal with 7 columns and 13 rows of dielectric pillars. The darker grey data is for a tunable laser source of 1410nm-1510nm. The lighter grey data is for source wavelength of 1510-1610nm. The shaded region indicates the band gap covered by the tunable range. The band gap extends to 1725nm.

Development of Birefringence-free Ridge Waveguides for Waveguide Isolators

Personnel
X. Guo and T. Zaman (R. Ram and H.I. Smith)

Sponsorship
Walsin-Lihwa Corporation

An optical isolator is a device to transport light in only one direction. They are required in optical communication systems to protect laser sources from reflections. Nowadays, microoptic isolators are available, but they are bulky and require expensive alignment. In contrast, a waveguide isolator which can be integrated with the source and other waveguide devices will be necessary for highly integrated photonics circuit, and may be much cheaper. The goal of this project is to develop an integrated waveguide isolator.
A nonreciprocal polarization rotation is the key to an isolator's performance. Faraday rotation is a well-known nonreciprocal polarization rotation. We have observed Faraday rotation in magnetically doped InP with F=6°/mm, and a loss of α=0.2cm^{-1} at 1550nm.The coupling ratio is calculated as below in a Faraday rotation;

$$R = \frac{F^1}{F^1 + (\Delta\beta/2)^1}$$

where R is the conversion ratio between TE and TM, F is the Faraday constant, and $\Delta\beta = \beta_{TE} - \beta_{TM}$ is the difference of propagation constants between TE and TM. In a waveguide with linear birefringence, the incomplete conversion of TE and TM will limit the polarization rotation to a small angle. Thus, a waveguide is required to have the same propagation constant for both TE and TM in order to have pure nonreciprocal polarization rotation. Linear birefringence arises from various sources including: stress, waveguide geometry, photoelastic effect, etc.

We have developed techniques for fabricating birefringence-free ridge waveguides for integrated waveguide isolators. The waveguides consist of a INGaAsP core layer and cladding layers of magnetically doped InP. Both stress-induced birefringence and photoelastic birefringence are negligibly small. To eliminate the shape birefringence, the ridge waveguide is designed to have a certain width and depth. The calculation of parameters for a birefringence-free waveguide is shown in Figure 56 from a program developed by Mike Watts and Prof. Hermann Haus.

In our process, a high-index-contrast mesa is used. The etched depth is 2.0-2.5μm and the width 1-1.5μm. The etching mask is 100 nm of Ti. The ridge waveguide is etched using reactive ion etching with a mixture of hydrogen and methane. An SEM micrograph of the etched ridge waveguide is shown in Figure 57.

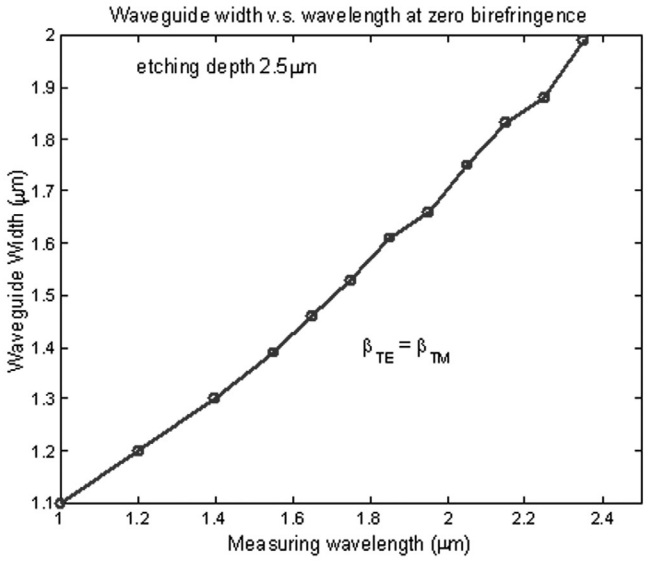

Fig. 56: Calculation of zero birefringence for different waveguide widths and measuring wavelengths (2.5 μm etch depth for all waveguides)

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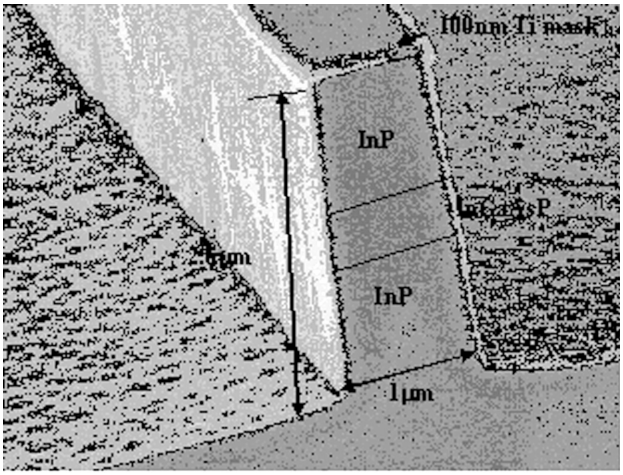

Fig. 57: Scanning-electron micrograph of a RIE etched ridge waveguide

Educational Activities

- ***Adding Device Simulation to the MIT Microelectronics WebLab***
- ***Microfabrication Project Laboratory (6.151)***
- ***Microelectronics Fabrication Technology (6.152J)***

Adding Device Simulation to the MIT Microelectronics WebLab

Personnel:
A. O. Solis (J. A. del Alamo)

Sponsorship:
I-Campus (Microsoft)

The MIT Microelectronics WebLab (or "WebLab" for short) is an online laboratory for characterizing microelectronic devices. Through only a Java-enabled web browser, users all over the world can characterize transistors and other microelectronic devices by means of an Agilent 4155B semiconductor parameter analyzer located at MIT.

We are currently enhancing WebLab by adding simulation capabilities to the system. Integrating experiments and simulations is a powerful way to learn about a device. Students appreciate the applicability of idealized device models better when they compare the predictions of these models with actual measurements. In addition to allowing users to perform repeated measurements while varying a particular voltage or current, the simulation component will also let students run repeated simulations while varying a given model parameter. Examining how changes in a model parameter affect device characteristics helps students better understand how the device operates. Moreover, a simulation environment allows students to explore certain device behaviors that would be unfeasible or unsafe to examine otherwise; for example, a voltage condition that leads to destructive transistor breakdown.

In our architecture, the WebLab client applet views the simulator as another server to which it can send an experiment to be performed. Along with the usual test vector, the client specifies the parameters required by the device model. On the server side, the simulator mimics the behavior of the Agilent 4155B semiconductor parameter analyzer by generating a sequence of voltages and currents. For each stimulus in the sequence, the simulator solves the model equations to determine the DC response of the device to those conditions. The simulator then returns the results to the user. The system allows the user to perform a simulation alone, or combine the simulation with a concurrent measurement.

A prototype simulator has been developed and integrated with the WebLab 4.2 client applet. The simulator has been used with several simple devices, including a resistor, an ideal pn diode, and a pn diode with non-zero series resistance. Figure 1 shows the WebLab client applet graphing the measured and simulated response of a pn junction to an applied voltage. We are currently working on improving the WebLab simulation system by developing models for other devices (e.g. BJTs and MOSFETs), improving the robustness of the numerical algorithms, and implementing an administrative interface.

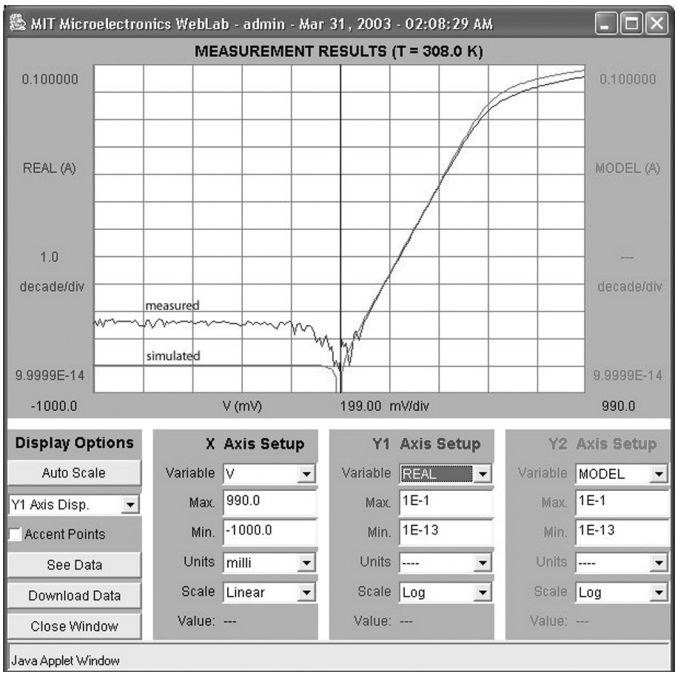

Fig. 1: Measured and simulated response of a pn junction to an applied voltage, plotted in the WebLab client applet.

Microfabrication Project Laboratory (6.151)

Technical Instructor
Li-Wen Wang

This laboratory course is offered in the spring semester for students that have already completed 6.152J. The course is designed to teach experimental microfabrication process design. The students of this subject are given a broad process goal, namely to build a device, and they are challenged to design and develop a process sequence. Typically, the entire class (4-6 students) works on one device, and they partition the integrated process into a set of unit process sequences. Work proceeds first, on the development of the unit processes, and then, on the integrated process. In recent years, the students have succeeded in microfabricating micromachined contactors for integrated circuit testing, flexible electrode arrays for retinal implants, and microcantilevers for AFM applications.

Microelectronics Fabrication Technology (6.152J)

Technical Instructor
Li-Wen Wang

This combination laboratory and lecture course is offered and taught jointly by the Department of Electrical Engineering and Computer Science and the Materials Science and Engineering Department. The course includes weekly lectures on all aspects of microfabrication technology with design problems to teach process design. Additionally, the course includes 10 four-hour laboratory sessions conducted in the MTL. During these sessions, each student fabricates a wafer of poly-silicon gate MOS devices and test structures. The devices and structures are tested at the end of the semester. A final report correlating the test results with theoretical expectations culminates the education experience. The course is offered every semester, and a laboratory-only version of the course is offered 3-4 times/year. Last year, approximatley 100 students were educated in microfabrication technology through this course.

MTL Research Centers

- *MIT - MicroChemical Systems Technology Center*
- *Center for Integrated Circuits & Systems*
- *Intelligent Transportation Research Center (ITRC)*
- *MEMS@MIT*

MIT - MicroChemical Systems Technology Center

Prof. Klavs F. Jensen, Director

This is a multidisciplinary Center focused on design and fabrication of new integrated microchemical systems for discovery, synthesis, and development of chemicals and processes relevant to chemical and pharmaceutical industries. Microfabrication techniques and scale-up by replication have fueled spectacular advances in the electronics industry, and they rapidly revolutionizing biological research and drug discovery. Microfabrication offers a similar potential for faster, cheaper, better chemical product research and development. Microchemical systems combined with instrumentation in small bench top units would clearly require less fume hood space, utilities, produce less waste, and offer safety advantages. Moreover, they would greatly enhance research and development productivity through high-throughput screening of catalysts and process chemistries, as well as efficient data integration.

Microreaction technology has several potential advantages for chemical production. The high heat and mass transfer rates possible in microfluidic systems allow reactions to be performed under more aggressive conditions with higher yields than can be achieved with conventional reactors. More importantly, new reaction pathways deemed too difficult in conventional macroscopic equipment would be pursued. The inherent safety characteristics of the technology suggest that production scale systems of multiple microreactors should enable distributed point-of-use synthesis of chemicals with storage and shipping limitations, such as highly reactive and toxic intermediates. Scale-up to production levels by replication of microreactor units used in the laboratory would eliminate costly redesign and pilot plant experiments, thereby shortening the development time from laboratory to commercial production. The approach would be particularly advantageous for the fine chemical and pharmaceutical industries, where production amounts are often small. The strategy would also allow for scheduled, gradual investment in new chemical production facilities without committing to a large production facility from the outset, thus reducing risks and high capital costs.

In developing microreaction technology, it will be essential to focus on systems where microfabrication can provide unique process advantages. Such advantages could be derived from increased mass and heat transfer, leading to improved yield and safety for an existing process. The real value of the miniaturization effort, however, would be in exploring new reaction pathways and finding economical and environmentally benign solutions to chemical manufacturing. It will be important to exploit characteristics resulting from the small dimensions beyond the high transport rates, specifically forces associated with high surface area-to-volume ratios. In order for microreactors to move beyond the laboratory into chemical production, they must also be integrated with sensors and actuators, either on the same chip, or through hybrid integration schemes. The integration of chemical systems with sensors in μTAS is already rapidly expanding the field, and cross-fertilization with microreactors for chemical synthesis will ultimately result in integrated chemical processors. The packaging of multiple reactors presents significant challenges in fluid handling, local reactor monitoring, and control.

Research in the Center addresses the above issues through innovations in microreactor technology and applications. A partial list of focus areas includes:

- Evaluation of the value of the microreaction technology to the chemical and pharmaceutical industry by testing many different chemical systems in microreactors, emphasizing those chemical systems that would be difficult or impossible to do at larger scales, *i.e.* less controlled conditions.

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- Operation of integrated systems (for single and multistage synthesis)
- Reaction engineering design strategies (including economic considerations) and tools for microchemical systems.
- Versatile microreactor designs integrating fluid, electrical, and optical distribution systems that are applicable to a broad range of chemical systems.
- Microreactor packaging strategies allowing easy interchange of reaction units and integration with microfluidics and control systems.
- Microfabrication methods with a broad range of materials (polymers, metals, and ceramics) compatible with chemical processes and establish criteria for materials selection.
- Microscale separation techniques that are analogs or replacements of distillation, extraction, and chromatographic techniques used in conventional laboratory synthesis.

The center currently involves eight chemical, fine chemicals, and pharmaceutical companies. The Center conducts semiannual reviews of research progress. The advisory board meets after these reviews and provides feedback and advice to MIT participants on research targets and progress. Research collaborations and visit from member companies are actively pursued.

Center for Integrated Circuits and Systems (CICS)

Prof. Hae-Seung Lee, Director

The Research Center for Integrated Circuits and Systems (CICS) is a form of an industrial consortium created to promote new research initiatives in circuits and systems design, as well as to promote tighter technical relation between MIT's research and relevant industry. Four faculty members, Hae-Seung Lee, Anantha Candrakasan, Michael Perrott, and Charles G. Sodini participate in the Center for Integrated Circuits and Systems. We have been investigating a wide range of circuits and systems related to wireless communication, optical communication, microsensor/actuator systems, imagers, digital and analog signal processing circuits, dc-dc converters, and many other systems.

We strongly believe in the synergistic relation between the industry and academia, especially in practical research areas of the integrated circuits and systems. We are convinced that the Center for Integrated Circuits and Systems is the conduit for such synergy. The Center currently has twelve member companies. The Center includes all research projects that the three participating faculty members conduct regardless of the sources of funding. There are two different forms of technical interaction between the member companies and the Center. The broad interaction occurs through research reviews held twice a year open to member companies. These are technical reviews where technical representatives from member companies can critique the projects. In each full day review, we present as many projects as possible. The more intimate interaction happens at a more personal level with graduate students who are working on projects of member company's particular interest. The member company may invite them to give presentations at their site.

At biannual research reviews we have received valuable technical feedback as well as suggestions for future research. There has been close interaction between member companies and the Center personnel through company visits, summer employments, and personal

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Intelligent Transportation Research Center (ITRC)

Dr. Ichiro Masaki, Director

interactions. We believe such an interaction has given very positive results for both MIT and member companies. We are hoping to continue to expand the Center in the future.

Transportation is an important infrastructure for our society. The U.S. interstate highway network, for example, contributes significantly to improving our standard of living. On the other hand, current transportation systems have serious problems including congestion, safety, and environmental issues. While the problems are becoming more serious, the conventional solutions such as building new roads are getting more difficult. It is now time to propose a new transportation scheme for solving those increasing problems. Fortunately, we have a technical foundation to propose Intelligent Transportation Systems (ITS) for improving the existing transportation systems by utilizing microsystems and other related technologies.

ITS includes various systems for private and public transportations and also for roadside functions. Some early systems are already commercially available but significant research is needed for more advancement. Examples of commercially available systems include intelligent cruise control for controlling the distance to the car in front, intelligent traffic lights which give a high priority to buses and emergency vehicles, and smart roadside cameras for detecting accidents. Furthermore, ITS has possibilities of becoming the first large-scale application of the next generation communication networks.

In responding to those social needs, MITs Microsystems Technology Laboratories has established the Intelligent Transportation Research Center (ITRC) in September 1998 as a contact point of industry, government, and academia for ITS research and development. The emphasis of the center is the integration of component technology research and system design research. The integration of technical possibilities and social needs is another focus of the center. Multidisciplinary teams are working on various aspects of ITS to find real solutions.

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I. Masaki leads the center, and the faculty collaborators include B. K. P. Horn, H.-S. Lee, T. B. Sheridan, C. G. Sodini, J. M. Sussman, and J. L. Wyatt. Five companies have joined the center as members, and some of them have their representatives staying at MIT as visiting scientists. Research projects range from custom chips for wide-dynamic imaging and array processing to sensor-fusion, real-time stereo vision, three-dimensional image compression, recognition of compressed image without decompression, internet-based network architecture, and the next of the next generation internet.

MEMS@MIT

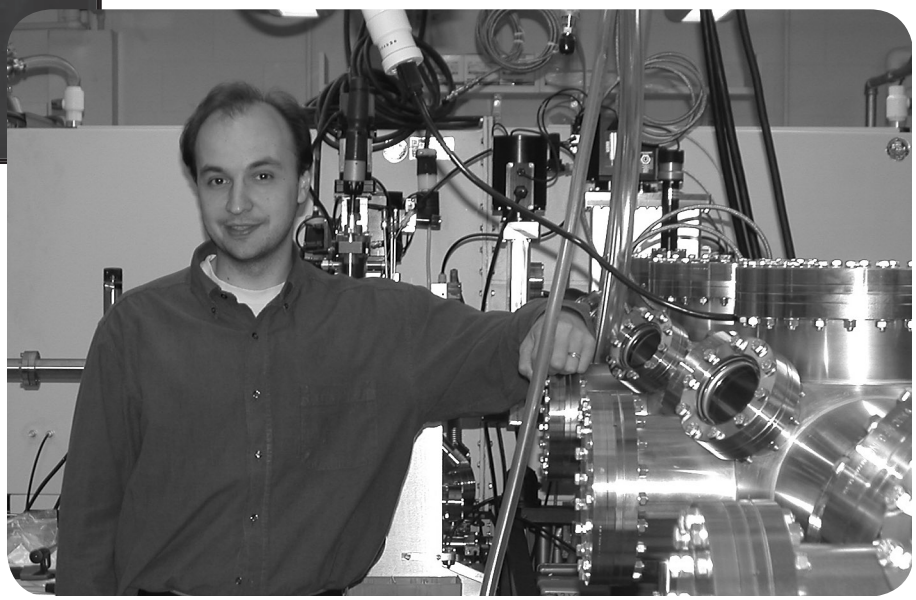
Prof. Martin A. Schmidt, Director

The newly-formed MEMS@MIT Center is being established to promote stronger industrial interactions with the MEMS community at MIT, and to support the central needs of the MEMS community. This Center is comprised of 26 faculty investigators, drawn from 8 academic departments. This highly collaborative group conducts research in four primary areas: materials, technology, CAD, and applications. In addition, we support a broad agenda of educational activities. The contracted research volume in MEMS exceeds $12M/year, supporting approximately 130 students and staff, with funding derived from industry and government agencies.

The Center offers member companies the opportunity to participate in focused research briefings, to gain access to the personnel and knowledge base of the MIT MEMS efforts, and to access intellectual property on member-funded research projects. The resources from the Center are deployed to support experimental infrastructure, research staff, and focused research initiatives that are aligned with the member companies interests. At biannual research reviews we receive valuable technical feedback as well as suggestions for future research.

Faculty, Research Staff and Publications

Professor Michael Perrott



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Publications
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Publications

Yang, V.K., M.E.G., G. Taraschi, C.W. Leitz, A.J. Pitera, M.T. Currie, Z. Cheng, and E.A. Fitzgerald, "Monolithic Integration of III-V Optical Interconnects on Si Using SiGe Virtual Substrate", Journal of Materials Science: Materials in Electronics, 2002. 13(7): p. 377-380.

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Publications
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Mabboux, P.-Y. and K.K. Gleason, "^{19}F NMR Characterization of Electron Beam Irradiated Vinylidene Fluoride/Trifluoroethylene Copolymers." J. Fluorine Chem., 2002, 113: p.27-35 .

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Publications

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Student Theses Awarded

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Student Theses Awarded

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Blaha, D. (D. Boning), EECS, "Outsourcing Model for Semiconductor Fabrication Equipment," May 2002 (also used for SM in Management).

Calhoun, B. (A. P. Chandrakasan), "Circuit Techniques for Subthreshold Leakage Reduction in a Deep Sub-Micron Process", May 2002

Coe, S (V. Bulovic), "Efficient Light Emitting Devices Utilizing CdSe (ZnS) Quantum Dots in Organic Host Matrices," M.S. Thesis, Department of Electrical Engineering and Computer Science, June 2002.

Drego, N. (D. Boning), EECS, "Variation-Aware Design of On-Chip Optical Clock Receiver Circuits," expected May 2003.

Gonzalez-Valentin, K. (D. Boning), EECS, "Extractions of Variation Sources Due to Layout Practices," May 2002.

Ickes, N. (A. P. Chandrakasan), "Hardware and Software for a Power Aware Microsensor Node," May 2002.

Ingham, D. (D. Boning), EECS, "Modeling the Cost of Quality in PC Assembly," May 2002 (also used for SM in Management).

Kelly, R. (D. Boning), EECS, "Visualization Tools in Semiconductor Strategic Capacity Planning," May 2002 (also used for SM in Management).

Konstantakopoulos, T. (A. P. Chandraksan), "Implementation of Delay and Power Reduction Techniques in Deep Sub-Micron Buses," May 2002.

continued

continued

Student Theses Awarded

Master of Science (S.M.)

Lee, F. (A. P. Chandrakasan), "Analysis, design, and prototyping of a narrow-band radio for application in wireless sensor networks," May 2002.

Lin, Y. (J.A. del Alamo), "A Collaboration System and a Graphical Interface for the MIT Microelectronics WebLab," EECS, June 2002.

Lisuwandi, E (V. Bulovic), "Feedback Circuit for Organic Light Emitting Device Active Matrix Display Drivers," M.S. Thesis, Department of Electrical Engineering and Computer Science, June 2002 (co-supervised with C. Sodini).

Madigan, C. (V. Bulovic), "Aspects of Exciton Behavior in Amorphous Organic Thin Films," M.S. Thesis, Department of Electrical Engineering and Computer Science, June 2002.

Montoya, J. (Q. Hu), thesis title, "THz Transceiver/Two-Photon Absorption Autocorrelator," August, 2002.

Noonan, E. (S.M. Spearing), "Failure Analysis of the MIT Microrocket", S. M. June 2002

O'Halloran, M. (R. Sarpeshkar), "A Clock Based Analog Memory Element for Integrated Circuits," Master of Science thesis, Department of Electrical Engineering and Computer Science, MIT, 2002.

Phanaphat, P. (A. P. Chandrakasan), "Protocol Stacks for Power-Aware Wireless Microsensor Networks," May 2002.

Ponchner, K. (D. Boning), Chem. Eng., "Feedback Control of Polysilicon Patterning in Semiconductor Manufacture," May 2002, (also used for SM in Management).

Samuels, M. (D. Boning), EECS, "PC Assembly Factory Siting," May 2002 (also used for SM in Management).

Scholtz III, R.L. (J.A. del Alamo), "Strategies for manufacturing low-volume semiconductor products in a high-volume manufacturing environment," LFM, June 2002.

Scott, M. (D. Boning), EECS, "Material Handling Systems in Semiconductor Manufacturing," May 2002 (also used for SM in Management).

Shaw, R. (A. P. Chandrakasan), "Hardware Implementation of a Low-Power Two-Dimensional Discrete Cosine Transform," May 2002.

Sit, J-J. (R. Sarpeshkar), "A Low Power Analog Logarithmic Map Circuit with Offset and Temperature Compensation for use in Bionic Ears," Master of Science thesis, Department of Electrical Engineering and Computer Science, MIT, 2002.

Smith, E. (D. Boning), EECS, "Advanced Visualization for Shop Floor Management in Semiconductor Manufacturing," EECS, expected May 2003 (also used for SM in Management).

Simpkins, T. (A. P. Chandrakasan), "Active Optical Clock Distribution", May 2002.

Sohn, C. (V. Bulovic), 1. , "Commercialization Potential of Quantum Dot Light Emitting Devices," M.S. Thesis, Department of Material Science and Engineering, June 2003.

Stuart, E. (L. Kimerling), ME, Sloan, "The Decision and Implementation of a Supply Chain Management System at Giga APS, an Intel Company," June 2002.

Tanasa, C.E. (D. A. Antoniadis), EECS, "Hole Mobility and Effective Mass in SiGe Heterostructure-Based PMOS Devices," September 2002. - Antoniadis

Young, D. (M.A. Schmidt), "Simple Package for Resistive-pulse Sensing with a Silicon Pore," August 2002.

continued

continued

Student Theses Awarded

Doctoral (Ph. D.)

Acosta-Serafini, P. (C.G. Sodini), "A Programmable Wide Dynamic Range Image Sensor with Automatic Pixel-by-Pixel Exposure Control", expected May 2003.

Ajmera, S. (K.F. Jensen and M.A. Schmidt), "Microreactors as a Laboratory Testing Platform," May 2002 (Chemical Engineering).

Bulzacchelli, J.F. (H.-S. Lee) , "A Superconducting Bandpass Delta-Sigma Modulator for Direct Analog-to-Digital Conversion of Microwave Radio", April, 2003
Cronin, S. (M. Dresselhaus), Ph.D. Thesis, June 2002

Chen, C.G. (M.L. Schattenburg), "Beam Alignment and Image Metrology for Scanning Beam Interference Lithography – Fabricating Gratings with Nanometer Phase Accuracy," Ph.D. Thesis, Department of Electrical Engineering and Computer Science, expected April 2003.

Cho, S.-H. (A. P. Chandrakasan), "Energy Efficient RF Communication System for Wireless Microsensor System," May 2002.

Djomehri, I. (D. A. Antoniadis), EECS, "Comprehensive Inverse Modeling for the Study of Carrier Transport Models in Sub-50 nm MOSFETs," September 2002.

Duerr, E.K. (Q. Hu), thesis title, "Distributed Photomixers," August, 2002.

Erchak, A.A. (L.A. Kolodziejski and H.I. Smith) "Enhanced Performance of Optical Sources in III-V Materials Using Photonic Crystals", Ph.D. Thesis, Department of Materials Science and Engineering, June 2002.

Fiorenza, J. (J.A. del Alamo), "Design and Fabrication of an RF Power LDMOSFET on SOI", EECS, September 2002.

Fujimori, I. (C.G. Sodini), "CMOS Passive Pixel Design Techniques", February 2002.

Gbondo-Tugbawa, T. (D. Boning), EECS, "Chip-Scale Modeling of Pattern Dependencies in Copper Chemical Mechanical Polishing Processes," May 2002.

Goodlin, B. (D. Boning and H. Sawin), Chem. Eng., "Multivariate Endpoint Detection of Plasma Etching Processes," May 2002.

Groenert, M.E. (G. Fitzgerald),, "Monolithic Heteroepitaxial Integration of III-V Semiconductor Lasers on Si Substrates", September 2002

Hitko, D. (C.G. Sodini), "Circuit Design and Technological Limitations of Silicon RFICs for Wireless Applications", June 2002.

Konkola, P.T. (M.L. Schattenburg), "Design and Implementation of a Scanning Beam Interference Lithography System for Patterning Gratings with Nanometer-Level Distortion," Ph.D. Thesis, Department of Mechanical Engineering, expected April 2003.

Lee, B. (D. Boning), EECS, "Modeling of Chemical Mechanical Polishing for Shallow Trench Isolation," May 2002.

Leitz, C. (G. Fitzgerald), "High Mobility Strained Si/SiGe Heterostructure MOSFETs: Channel Engineering and Virtual Substrate Optimization", June 2002

Lim, M. (H.I. Smith), "Development of x-ray Lithography and Nanofabrication techniques for III-V Optical Devices", Ph.D. Thesis, Department of Electrical Engineering and Computer Science, MIT, February 2002.

Luschas, S. (H.-S. Lee), "A Radio Frequency Digital-to-Analog Converter," May 2003.

continued

continued

Student Theses Awarded

Doctoral (Ph. D.)

McMahill, D. (C.G Sodini), "Automatic Calibration of Modulated Fractional-N Frequency Symthesizers", June 2001

Moon, H.-S. (S.M. Spearing and M.A. Schmidt), "Design of Si/SiC Hybrid Structures for Elevated Temperature MicroTurbomachinery," May 2002 (Aero/Astro).

Narendra, S. (A. P. Chandrakasan), "Effect of MOSFET Threshold Voltage Variation on High-Performance Circuits," January 2002. (co-supervised with Prof. Dimitri Antoniadis)

Nayfeh, H.M. (D. A. Antoniadis and J. L. Hoyt), EECS, "Investigation of the Electron Transport and Electrostatics of Nanoscale Strained Si/SiGe Heterostructure MOSFET Transistors," March 2003.

Park, T. (D. Boning), EECS, "Characterization and Modeling of Pattern Dependencies in Copper Interconnects for Integrated Circuits," May 2002.

Peng, M. (H.-S. Lee), "Study of Substrate Noise and Techniques for Minimization," February, 2003

Roberts, D. (M.A. Schmidt), "Development of Piezoelectric-MEMS-Microhydraulic Energy Harvesting Technology," January 2002 (Mechanical Engineering).

Rose, A. (V. Bulovic), "Optimizing the Excited State Processes of Conjugated Polymers for Improved Sensory Response," Ph. D. Thesis, Chemistry Department, February 2003 (co-supervised with T. Swager).

Smith, A.L. (L. Kimerling), MSE, "Transition Metal Gettering Studies and Simulation for the Optimization of Silicon Photovoltaic Device Processing," June 2002.

Sotiriadis, P.P. (A. P. Chandraksan), "Interconnect Modeling and Optimization in Deep Sub-Micron Technologies", May 2002

Wang, C.-C. (C.G. Sodini), "A Study of CMOS Technologies for Image Sensor Applications", August 2001.

Yang, V.K.F. (G. Fitzgerald), "Integration of III-V Optical Devices and Interconnects on Si Using SiGe Virtual Substrates", June 2002

Opposite Page:

Process engineer at wafer cleaning station, Technology Research Laboratory.

Microsystems Technology Laboratories

MIT Microsystems Technology Laboratories (MTL) Organization and Administration

Background

MIT's Microsystems Technology Laboratories (MTL) was founded in the early 1980s to provide a complex of modern microelectronics fabrication laboratories, ultraclean rooms, and materials processing facilities. At the present time, MTL is as an Interdepartmental Laboratory (IDL) of the Institute reporting to the Dean of the School of Engineering.

Mission Statement

MTL's primary mission is to enable research through the support of an intellectual and physical environment that makes possible education through teaching and research in areas that require or that may benefit from microelectronic/microfabrication technology. The microfabrication, testing, and computational facilities of the MTL are open to the entire MIT community and researchers from other university or government laboratories, as well as limited industrial participation.

The facilities of the MTL consist primarily of clean-room microfabrication laboratories and associated design, simulation, testing, and characterization equipment and expertise, as well as an extensive computer network.

Over the period of its existence, the MTL has committed significant resources to the maintenance and acquisition of capital equipment. These capital improvements, upgrades, and purchases allow us to serve an increasing user base, to decrease experiment turnaround (cycle) time resulting from lowered equipment "down-time". MTL recently completed a major capital program (~$12.8M) that upgraded our process facilities from 100-mm to 150-mm diameter substrates. This plan was supported through industrial funding and equipment donations, institutional funding, and the MTL reserve fund.

The Sponsored Research Volume supporting MTL's research activities is approximately $40 million annually, from which the laboratory recovers ~$2.0 million annually to offset operating expenses (staff and consumables) of approximately $3.0 million. The remainder of operating expenditures are underwritten through the generous support of the Microsystems Industrial Group (MIG) who are listed in the Acknowledgments section of the report.

Administrative Structure

MTL is administered through the Office of the Director, Professor Martin A. Schmidt, who has overall responsibility for the operations of the MTL. Reporting to Professor Schmidt is Mr. Samuel Crooks, MTL Associate Director for Administration and Administrative Officer. Reporting to Mr. Crooks are a Fiscal/Contract Administrator, Personnel Officer, Media Specialist, Fiscal Assistant, and Account Assistant. Mr. Crooks and his staff have responsibility for the non-technical operations of the MTL. Reporting directly to Professor Schmidt is Ms. Anne Wasserman, Assistant to the Director.

Fabrication Facilities

MTL technical resources are managed by a professional technical staff. MTL facilities are open to all MIT faculty and students as well as users from other academic institutions and government agencies. Reporting directly to Professor Schmidt, Dr. Vicky Diadiuk, MTL Associate Director for Operations, manages the day-to-day technical operations of the MTL. Dr. Diadiuk has a staff of eleven research engineers and three research technicians.

Researchers planning to utilize the process facilities of the MTL submit a process description to the Process Technology Committee (PTC) The PTC, made up of faculty, students, and technical staff, reviews the process to ensure that it does not compromise or contaminate any of the tools. The PTC may recommend alternative process steps or disallow certain uses of materials, etc. Once

continued

the process application request has been approved, users may begin utilizing the labs. All users are required to successfully complete a safety and orientation course prior to their use of MTL facilities and must receive training from a research specialist for each piece of laboratory equipment they plan to operate.

MTL also maintains a comprehensive Computation Infrastructure, providing a broad array of services to the community. Professor Duane Boning (Electrical Engineering), MTL Associate Director, has responsibility for this activity. Users of MTL's fabrication facilities interface with the MTL's newly-installed Common Object Representation for Advanced Laboratories (CORAL) to perform their processes (e.g., reserve machines). The user log is coupled to a sophisticated charging algorithm which calculates a user fees on a monthly basis. CORAL, a major upgrade of CAFE is currently under development in collaboration with Stanford University.

Policy recommendations within the MTL are developed by a working group made up of Professors Martin Schmidt, Duane Boning, Anantha Chandrakasan, and Judy Hoyt, as well as Dr. Vicky Diadiuk and Mr. Samuel Crooks. The directors receive significant input from the faculty who make up the MTL and those whose research is closely coupled with the MTL. Recommendations from this working group may be presented to faculty during a weekly luncheon (Microlunch), or may be brought to the MTL Faculty Policy Board. Twice annually policy issues and decisions are reviewed with the MTL Microsystems Industrial Group (MIG) Advisory Board, whose members represent MTL's sponsor companies, and who provide advice and counsel on issues concerning the operations and research directions of the MTL.

Personnel involved in ongoing research activities at the MTL include over 80 faculty, 18 senior research staff, 375 graduate students, 150 undergraduate students, 20 postdoctoral associates, 15 visiting scientists, 60 research affiliates, 28 technical support staff, and 23 administrative and support staff. During the 2002-2003 academic year, approximately 31 Ph.D. and 43 S.M. and M. Eng. degrees were awarded in conjunction with research activities whose primary area of focus was microelectronics and which were strongly coupled to the facilities of the MTL.

For information regarding MTL's technical operations and capabilities, contact Dr. Vicky Diadiuk, MTL Associate Director, Operations, telephone (617) 253-0731, e-mail diadiuk@mtl.mit.edu. For information regarding MTL programs and other general information, please contact Mr. Samuel Crooks, Associate Director, Administration, telephone (617) 253-3978, e-mail crooks@mtl.mit.edu. You may also wish to visit our Web Site at: http://www-mtl.mit.edu.

Personnel

Microsystems Technology Laboratories Administrative Service

The Microsystems Technology Laboratories (MTL), which include the Integrated Circuits Laboratory (ICL), and the Technology Research Laboratory (TRL), and the Exploratory Materials Laboratory (EML) are managed by the MTL Director, Professor Martin Schmidt, Electrical Engineering and Computer Science.

Administrative Personnel

S. Crooks, Associate Director, Administration, and Administrative Officer

D. Hodges-Pabon, Personnel Officer

C. Jung, Fiscal Officer and Grant and Contract Manager

M. Karapetian
Media Specialist

A. Adams-Heath
Account Assistant (Billing)

D. Moore
Accounts Payable

Microsystems Technology Laboratories Fabrication Facilities

Fabrication Operations Personnel
Dr. V. Diadiuk, Associate Director, Operations, Principal Research Engineer

P. Varley
Clerical Assistant

Fabrication
D. Adams, Research Specialist, Techn. Supervisor
D. Terry, Technician A
T. Turner, Technician B

Diffusion and Device Characterization
B. Alamariu, Research Engineer

Vacuum Etching
J. Walsh, Research Engineer
R. Bicchieri, Research Specialist
D. Jameson, Research Specialist

Vacuum Deposition
P. Zamora, Research Specialist

TRL Processes
K. Broderick, Research Associate

Facilities
P. McGrath, Research Specialist

Equipment Maintenance
B. McKenna, Research Specialist

CORAL and Web Applications
Ike Lin, Research Specialist

Photolithography
P. Tierney, Research Specialist

Project Processing
G. Donahue, Research Specialist

continued

Personnel

Microsystems Technology Laboratories Computational Facilities

D. Boning, Associate Professor
Electrical Engineering and Computer Science
Associate Director
Computation and Information Systems

D. E. Troxel, Professor
Electrical Engineering and Computer Science
Technical Advisor
Computation and Information Systems

T. Lohman, Research Specialist
System/CIM Manager

M. Hobbs, Research Specialist
System Manager

W. Maloney, Research Specialist
System Manager

Michael McIlrath, Research Specialist
System/CAD Manager

Microsystems Technology Laboratories Operating Committees

Process Technology Committee (PTC)
A. Akinwande, Associate Professor, EECS
J. del Alamo, Professor, EECS
V. Diadiuk, MTL Associate Director, Operations (Chair)
J. Lang, Professor, EECS
J. Hoyt, Associate Professor, EECS
S. Akiyama, DMSE
G. Nielson, MechE
A. Ritenour, EECS
L. Velasquez, Aero-Astro

Computer Systems Committee
Duane Boning, Professor, EECS (Chair)
Charlie Sodini, Professor, EECS (Chair)
Mike Perrott, Assistant Professor, EECS
Don Troxel, Professor, EECS
Tom Lohman, System/CIM Manager
Mike McIlrath, CAD Manager
Acia Adams-Heath, Recording Secretary, MTL
Mike Hobbs, Systems Manager, MTL
Bill Maloney, Systems Manager, MTL
Isaac Lauer, Ph.D. Candidate
Myron Freeman, Systems Manager, EECS
Bernard Alamariu, Research Engineer, MTL
Sam Crooks, Associate Director, MTL
Shamik Das, Ph.D. candidate
Brian Lee, Ph.D. candidate

MTL Faculty Policy Board
D. Antoniadis, Professor, EECS
D. Boning, MTL Assoc. Director and Professor, EECS
A. Chandrakasan, Professor, EECS
J. del Alamo, Professor, EECS
J. Hoyt, Associate Professor, EECS
R. Reif, Professor, EECS
M. A. Schmidt, MTL Director and Professor, EECS (Chair)
C. G. Sodini, Professor, EECS
S. Crooks, Associate Director (ex-officio)
V. Diadiuk, Associate Director (ex-officio)

Research Laboratories and Facilities

The Microsystems Technology Laboratories Facilities

MTL is located in the Gordon Stanley Brown Building (Building 39). Administratively, the MTL is an Interdepartmental Laboratory (IDL) of the Institute reporting to the Dean of the School of Engineering. In accordance with the multidisciplinary nature of microsystems technology, the faculty, staff, and students using MTL are affiliated with the many schools, departments, and centers of MIT. The following is a brief description of the MTL research facilities:

The Integrated Circuits Laboratory (ICL)
7,910 sq-ft integrated circuit fabrication facility comprised of:
- 2,800 sq.-ft Class 10 clean space
- 4,000 sq.-ft support space
- 460 sq.-ft characterization space
- 650 sq.-ft electrical testing and parametric characterization (ICs and devices)

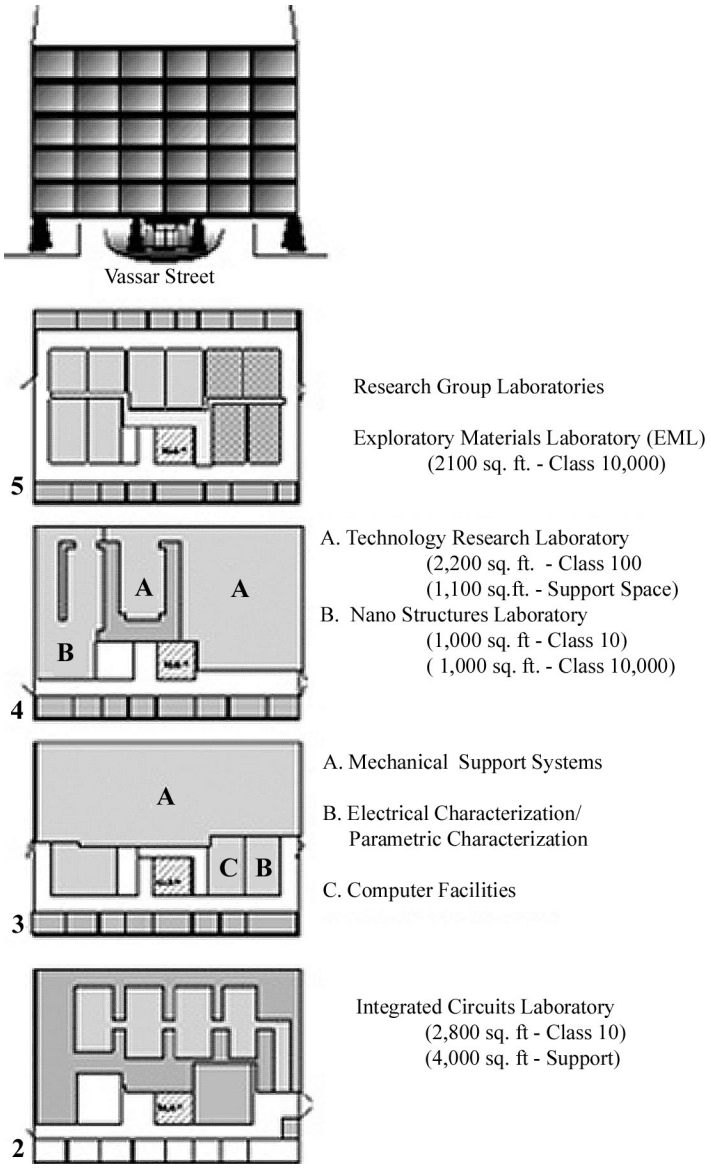
The Technology Research Laboratory (TRL)
3,600 sq-ft of laboratory space comprised of:
- 2,200 sq.-ft class 100 clean space
- 1,400 sq.-ft support space

The Exploratory Materials Laboratory (EML)
This is a flexible thin film deposition lab, with photolithography, etching and metrology capabilities.
- 2,100 sq.-ft class 10000 clean space

The Research Group Laboratories (RGL)
3,000 sq.-ft of laboratory space divided into six laboratory rooms assigned to individual research groups who are the principal users of ICL, TRL, and EML, and the NanoStructures Laboratory (NSL).

An additional 4,000 sp-ft of MTL office and laboratory space are located adjacent to Building 39 in Building 38.

Gordon Stanley Brown Building (Building 39) Microsystems Technology Laboratories



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MTL Fabrication Laboratories

Process research and device fabrication at MTL are primarily conducted in three laboratories, the Integrated Circuits Laboratory (ICL), the Technology Research Laboratory (TRL) and the Exploratory Materials Laboratory (EML). The ICL is designed, equipped and staffed to serve as a highly advanced silicon integrated circuit, device, structures, and process research facility. The laboratory houses a complete four inch silicon IC fabrication line. Cassette-to-cassette transfer techniques are employed extensively, and VLSI discipline is maintained throughout the facility.

The TRL has two primary functions:

- To support the development of novel process technologies
- To provide facilities for the fabrication of novel circuits and microstructures

The EML is a highly flexible microfabrication resource with all the basic fabrication capabilities and few limitations, beyond those called for by safety protocols, on substrate and source materials

The TRL and ICL are complementary laboratories. Since the ICL is designed to permit fabrication of complex integrated circuits and devices, by necessity it must be operated under the strict discipline that is required for state-of-the-art silicon device and circuit research. The TRL is designed to make up for any loss of flexibility that this discipline imposes. Similarly, fabrication of devices in the ICL can readily take advantage of new technologies that have been developed in the TRL. Examples of such technologies include deep reactive ion etching and wafer bonding. The Class 100 clean room environment and clean room procedures employed in the TRL assure that wafers can move between the ICL and TRL without compromising either the wafers or the facilities.

EML provides an additional degree of flexibility for samples that do not require strict cleanliness or contamination control. Samples that have been in EML cannot be transferred into ICL or TRL.

Over the last few years, we have committed significant resources to the maintenance and acquisition of capital equipmentto allow us to serve an increasing user base, to decrease equipment "down-time", and to integrate new or improved process technologies or capabilities into the facility. During the past year several major tools capable of handling 6" wafers were added to the facilities, and are now on-line. We also partnered with Applied Materials to obtain a full service contract covering our four AMAT tools to realize high equipment uptime improvements.

We have completed our plan to convert the labs from 4" to 6" wafer diameter. This conversion allows us to improve our process capabilities and makes MTL compatible with nearby fabs at Lincoln Lab and Analog Devices. The installations in ICL of the Thermco furnace banks and the Nikon i-line stepper, donated by Intel, were completed in 2001, providing a full 6" toolset. In 2002, the AME5000 etcher was converted to 6" capability, indicating the end of full 4" process capability in ICL. Process transfer by individual users, assisted by the technical staff is in progress. TRL has benefitted from an infusion of metrology and wet processing tools released by the 6" conversion in ICL.

MTL has continued to serve the microfabrication needs of the MIT community, working on projects from an ever-larger variety of academic departments (e.g., Biology, Chemical Engineering, Mechanical Engineering, Physics). As a result, lab activity continued to increase, as evidenced by both the number of students using the labs, and the amount of processing carried out. Once more, the Process Technology Committee served MTL

continued

Computation and Communications

well in carefully scrutinizing the increasing variety of new processes submitted, to ensure the integrity of all processes.

As indicated on the building schematic on the previous page, the building also houses the critical support facilities required to maintain the clean room conditions stated and provide for leading-edge process-related research. These include an air handling and conditioning system capable of maintaining the class 10 or 100 conditions at a temperature of ± 70 F. Liquid gas sources (nitrogen, oxygen, and argon) are used to supply ultrapure gases to the laboratories; ultrapure hydrogen gas is also supplied from a central source. The building also houses a sophisticated DeIonized (DI) water system and a modern waste water treatment plant. The DI water system capacity was increased in 1997 from 20 to 100 gpm of 17 M-ohm water and the total organic compounds reduced by an order of magnitude to 2ppb. The waste water treatment plant is monitored for full compliance with state and Federal environmental rules. The MIT administration provided support for these upgrades as well as funding for the cleanroom expansion necessary to accommodate the tools donated towards the 6”-conversion.

Data communication is essential to any modern laboratory. An extensive data communications network is installed in the Gordon Stanley Brown Building. The entire building is also served by a high-speed ethernet connected to the MIT computer network, and consists of a fiber optic backbone for the major subnet with multiple dedicated 10 Mb/second ethernets for each floor and major computer server. Terminals and workstations connected by way of these facilities can access the central computers in the building and, through a series of networks, computers all over the MIT campus as well as in universities, government, and industry throughout the United States and abroad.

Strasbaugh 6EG metal CMP

MTL Services

Process Development/Consultation

The MTL staff is available to assist users in developing new processes or process steps. This assistance ranges from casual consulting on a process problem, to joint user/staff development activities, to a staff-performed effort guided by the user. In addition, the staff frequently will develop new processes or unit steps which are deemed to be useful to the majority of the user community. Recent examples include the development of a nitrous oxide-based thin gate oxide process, CMP planarization, and several reactive ion etch/plasma etch processes both in Si and compound semiconductors.

In addition to these services, the staff is available to assist in a processing sequence defined by the user. This assistance ranges from performing a particular unit step or series of steps, all the way to processing an entire lot to completion. This can be done with the user's involvement and direction, or completely independently, in which case the completed lot is delivered to the user for evaluation.

A library of standard process recipes is maintained and checked routinely. These recipes include those used in the diffusion, oxidation, etch, photolithography and metallization areas. These documented steps greatly simplify and shorten the process development cycle, since frequently a new process can be "developed" by combining a series of these unit steps. Often, however, it becomes necessary to develop a new step or series of steps, or to employ materials, procedures or techniques not previously used in MTL. If a user encounters this situation, the proposed process must be submitted to the Process Technology Committee (PTC, composed of four faculty members, four student or postdoctoral users, and the Assistant Director of Operations) for review and approval prior to proceeding. This procedure has been adopted to insure that a.) no materials are inadvertently introduced into the facility which would compromise the research of other users, and b.) to guard against the possibility of machine use in a parameter range which might prove harmful to the equipment or the user. The PTC meets weekly to ensure rapid response to requests for new process activities.

Thermco Furnaces - cleanroom view, ICL

continued

MTL Services

Training

The MTL staff provides training to all new users of the facility to ensure safe and competent operation of MTL equipment. This training begins with an on-line orientation session, in which the user is introduced to MTL facilities, policies and procedures. Safety is stressed in this material, which includes proper procedures and techniques for handling the various acids, solvents, and gases employed in the facility, as well as a description of the alarms and various other systems that enable MTL to operate safely. Proper clean room procedures and techniques are also covered, as is a demonstration of CAFE, the computer system used to operate and monitor MTL facilities.

Following the MTL orientation and successful completion of Hazardous Waste and Chemical Hygiene training, individual training and instruction is given on each piece of equipment required by the user in his/her research project. The training consists of a series of "hands-on" sessions and continues until the user is comfortable with the equipment and the staff member is convinced that the user can safely and effectively operate the piece of equipment in question. Standard Operating Procedures are available for each piece of equipment, so users can refer to them conveniently.

Semiconductor Information Services

The Microsystems Technology Laboratories provides electronic information resources to the semiconductor research community by way of the World Wide Web. These services include extensive information about the people, facilities, and research of MTL. In addition, MTL makes available and coordinates access to information of value to the larger semiconductor community.

MTL-specific information is available at www-mtl.mit.edu. Through this page, one can

- Learn about the students, staff, and faculty associated with MTL
- Scan the facilities and equipment in MTL
- Find a detailed list of equipment and the cost of using it
- Read standard operating procedures for most machines
- See updates to the MTL VLSI Seminar Series schedule
- Keyword search through on-line versions of the MTL Annual Report
- Learn more about MTL research programs
- Link to additional research organizations at MIT

The "University Microfabrication Laboratory Network" (or Labnetwork) page is an informal focal point for discussion on topics of mutual interest to research and teaching microfabrication facilities. Records of past meetings and an archive of the labnetwork@mtl.mit.edu mailing list can be found at www-mtl.mit.edu/labnetwork/labnetwork.html.

Finally, the "Semiconductor Subway" provides links to semiconductor and microsystems-related information, including: fabrication facilities, technology, computer-aided design, manufacturing, microelectro-mechanical systems, professional societies and other organizations and a spectrum of other information. This page is highly popular, and has been averaging nearly 2,000 accesses per week. It can be accessed at www-mtl.mit.edu/semisubway.html.

Equipment

Integrated Circuits Laboratory (ICL)

Lithography
- Wafer Stepper
  GCA Corporation Model 6300 DSW
  Nikon NSR-2005i9
- Photoresist Coater Developer
  SSI 150
- Bake Oven/Vapor Prime
  Yield Engineering Systems, Inc., Model 3/10
- Photoresist Stripper
  Matrix 106 Plasma Asher
- Inspection Microscope
  Nikon OPTIPHOT 88
- Polyimide Coater
  MTI Flexi Fab
- Wet Chemical Process Station (2)
  Semifab Inc., Model WPS-400
- Wet Chemical Process Station
  Semifab Inc., Model WPS-800

Diffusion, Oxidation, and Chemical Vapor Deposition
- Furnaces
  Thermco 10K 4 Furnace Systems
  (4 atmospheric tubes, 4 LPCVD)
- Vertical Thermal Reactor
  SVG/Thermco 7000 Series
- Suspended Loading System
  Heraeus-Amersil, Inc. SLS-125 Diffusion
- Gas Cabinets
  Veriflow Corp. Toxic Gas Delivery Systems
- Wet Chemical Process Station
  Semifab Inc. Model WPS-400
- Tube Cleaner
  Reynolds Tech
  6" Horizontal Quartz Cleaning System
- Toxic Gas Monitor
  MDA Scientific, Inc. PSM-8e & 16 Multipoint Monitoring Systems
- Rapid Thermal Processes
  AG Associates Heatpulse 410
  AG Associates 8108
- Surface Charge Analyzer
  Semi Test SCA

Metal and Dielectric Deposition
- Electron-Beam Evaporator
  Temescal Semiconductor
  Model VES 2550 Products
- Sputtering System
  Applied Materials Endura
- Dielectric PECVD System
  Novellus Concept 1
- Leak Detector
  Varian Turbomolecular 979
  Model MS-170
- Wet Chemical Process Station
  Semifab Inc., Model WPS 400
- Gas Cabinets
  Veriflow Corp. Toxic Gas Delivery Systems
- Toxic Gas Monitor
  MDA Scientific, Inc., Model 7100

Etching
- Polysilicon/Oxide Dry Etch
  AME Model P5000
- Polysilicon/Nitride Dry Etch
  Lam Research Model 490B
- Metal Dry Etch
  Lam Research Model Rainbow 9600
- Wet Chemical Process Stations
  Semifab Inc., Model WPS-400

continued

continued

Equipment

Integrated Circuits Laboratory (ICL)

Metrology

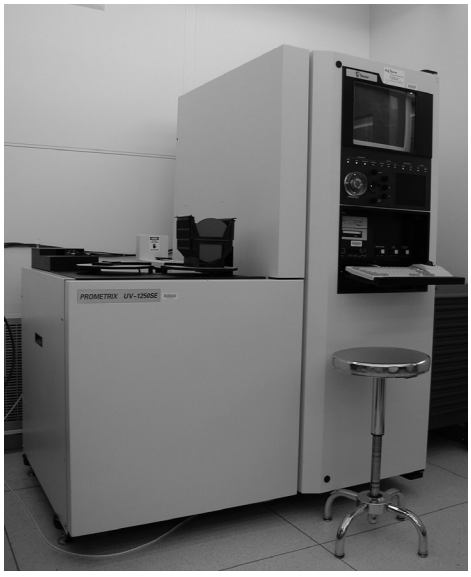
- Spectroscopic Ellipsometer
  KLA-Tencor-Prometrix UV-1280
- Surface Profilometer
  KLA-Tencor-Prometrix P10
- CV Plotter
  Materials Development Corporation
  Model CSM-16 Advanced Semiconductor
- Ellipsometer
  Gaertner Scientific Corporation
  Model L116BLC-26A
- Automatic Wafer Inspection System
  Aeronca Electronics Inc. WIS 150
- Automatic Four-point Probe
  Prometrix Corporation Omnimap 111B
  Resistivity Mapping System
- Inspection Microscope
  E. Leitz Inc. Ergolux Microscope/
  Camera System
- Low Voltage Scanning Electron Microscope
  Hitachi Model S-806
- Critical Dimension Scanning Electron Microscope
  Hitachi Model S-6000

Polishing/Etching

- Chemo-mechanical Polishing
  Strasbaugh 6EC dielectric CMP
  Strasbaugh 6EG metal CMP
- Wafer Cleaner
  SSEC Evergreen
- KOH Wet Etch Station
- Cu-plating Wet Station
- Film-thickness measurement system
  KLA-Tencor-Prometrix SM-300

Inspection and Test

- Non-Contact Surface Profiler
  WYKO Corporation, TOPO - 2D, TOPO - 3D
- Spreading Resistance Probe
  Solid State Measurements, Inc.
  Model ASR-100C/2
- Scanning Electron Microscope
  Hitachi Model S-800
- Electrical Measurements
  Hewlett-Packard Model HP 4062B
  Keithley Model 450 S
- Probers
  Electroglas Model 2001X
  Rucker/Kolls Model 1032



KLA-Tencor UV1280 film thickness measurement system

continued

continued

Equipment

Technology Research Laboratory (TRL)

Lithography
- Mask Aligners
  - Karl Suss Model MA6
  - Electronic Visions EV620
- Manual Photoresist Coater Solitec Inc.
  - Model 5110
- Bake Ovens
  - Blue M Model DDC-146C
- Wet Processing Station
  - Semifab Inc. Model WPS 800
- Inspection Microscope
  - Nikon Nomarski Microscope
- Surface Profilometer
  - Sloan Technology Corporation Dektak II
- Plasma Resist Stripper Branson IPC
- Wafer Aligner/Bonder Electronic Visions 620/501
- Photomask Contact Printer
  - Oriel Corporation Model 850202
- Measuring Microscope Nikon Model MM-1

Diffusion and Oxidation
- Furnaces
  - MRL Industries Model 718 System
  - (7 atmospheric tubes, 1 LPCVD tube)
- Wet Chemical Process Station
  - Semifab Inc. Model WPS-400
- Rapid Thermal Annealer
  - AG Associates Heatpulse 210T-02

Chemical Vapor Deposition/Etching
- PECVD/RIE (dual chamber)
  - Plasma Technology Plasmalab mP
- PECVD/RIE (single chamber)
  - PlasmaQuest

Etching
- ICP Deep Trench Etching System
  - STS - 6″
- ICP Deep Trench Etching System
  - STS - 4″
- Wet Chemical Process Station
  - Laminaire Corp.
- Wet Chemical Process Station
- Toxic Gas Monitor
  - MDA Scientific, Inc., PSM-8e
  - Multipoint Monitoring System
- Gas Cabinets
  - Scientific Gas Products

Metal Deposition
- Electron-Beam Evaporator
  - Temescal Semiconductor Products
- Sputtering System
  - Perkin Elmer Model 4450

Metrology
- Non-contact profiler WYKO Corp., RST
- Wafer curvature measurement system
  - KLA-Tencor FLX 2320
- Film thickness Measurement System
  - Nanometrics, Inc. Nanospec, AFT
  - Model L116BLC-26A
- Surface Profiler
  - Sloan Technology Corp. Dektak IIA
- IV Characterization
  - 2-point probe station
  - Tektronix 486 curve tracer

Experimental Apparatus
- Reactor for Low Pressure Epitaxial Growth of Erbium Doped Silicon and Silicon Germanium Alloys (L. C. Kimerling)

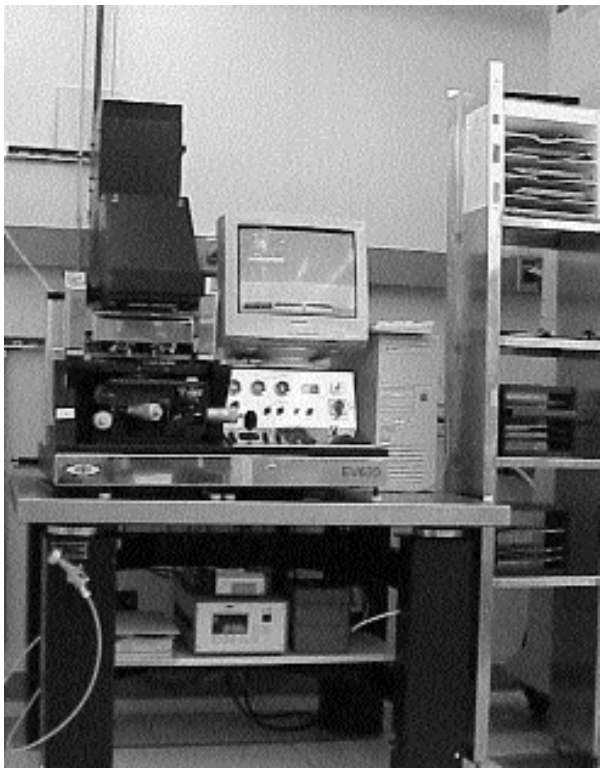
continued

continued

Equipment

Assembly

- Saw
  Disco Abrasive System Model DAD-2H/6T
- Die Bonder
  Kulicke and Soffa Industries Inc., Model 648
- Gold Ball Wire Bonder
  Kulicke and Soffa Industries Inc., Model 4124
- Wedge Bonder
  Kulicke and Soffa Industries Inc., Model 4123
- Junction Sectioner
  Philtec Instrument Co. Model 2015D



Electronic Vision (EV) Wafer Aligner-Bonder, TRL.

Computation and Communications

- Applications servers - Sun Ultra10 (2)
- Network mail server - Sun Ultra10
- CAD server - Sun Ultra2
- Simulation server - DEC Alpha
- Laboratory information servers - Sparc 20 (3)
- Laboratory information PCs - 23 Intel 400 MHz Pentium-III
- Research group workstations (60)
- Research group personal computers (40)
- X terminals (20)
- Network color laser, black and white printers
- Database servers(oracle) - Sun Ultra 10 (2)
- WWW Server - Sun Ultra 10
- Cad Server - Sun Ultra 2
- Application/backup Cad Server - Sun Ultra 2
- Application/Home Directory Server - Sun Ultra 2
- MTL Mail/NIS Server - Sparc 5
- Simulation Server - Dec Alpha 3000
- Laboratory Information Servers - Sparc 20 (2)
- Network Backup/Print Servers - Sparc 20 (3)
- Laboratory and Staff Desktop PCs - Intel 300MHz Pentium II (21)
- NT Network Servers - Intel/Dual Processor Pentium II (2)
- Network Switches - SuperStackII Switch 3300 (21)
- Cisco 2500 Router (ten dial-in lines)
- Peripheral Storage - total +207Gigabytes StorEdge Multipaks (6)
- Research Group Personal Computers (70)
- Research Group Workstations (Sun, HP, Alphas, IBM - 60)
- X-terminals NCD (20)
- Equipment Controller PCs (2)
- Laboratory Access PCs (2)
- Network Printers Apple Color, HP Laserwriters (9)

Related Research Facilities

NanoStructures Laboratory (NSL)

4500 sq-ft of laboratory space comprised of:
1,000 sq-ft class 10 clean space
1,000 sq-ft of class 10,000 space
2,500 sq-ft of ordinary lab space

The Nanostructures Laboratory (NSL) at MIT develops techniques for fabricating surface structures with feature sizes in the range from nanometers to micrometers, and uses these structures in a variety of research projects. The NSL is closely coupled to the Space Nanotechnology Laboratory (SNL) with which it shares facilities and a variety of joint programs. The NSL and SNL include facilities for lithography (photo, interferometric, electron-beam, and X-ray), etching (chemical, plasma and reactive-ion), liftoff, electroplating, sputter deposition, and e-beam evaporation. Much of the equipment, and nearly all of the methods, utilized in the NSL/SNL are developed in house. Generally, commercial processing equipment, designed for the semiconductor industry, cannot achieve the resolution needed for nanofabrication, is inordinately expensive, and lacks the required flexibility for our research. The research projects within the NSL/SNL fall into three major categories: (1) development of nanostructure fabrication technology; (2) short-channel semiconductor devices, nanomagnetics and microphotonics; (3) periodic structures for X-ray optics, spectroscopy, atomic interferometry and nanometer metrology.

NSL Research Staff and Personnel

H. I. Smith, Director
Keithley Professor of Electrical Engineering,
J. M. Carter, Research Specialist,
Research Lab of Electronics,
D. J. D. Carter, Research Engineer,
Research Lab of Electronics,
J. M. Daley, Project Technician,
Research Laboratory of Electronics,
J. G. Goodberlet, Research Engineer,
Research Laboratory of Electronics,
C. A. Lewis, Administrative Assistant,
Research Laboratory of Electronics,
M. K. Mondol, Research Specialist,
Research Laboratory of Electronics,
E. Murphy, Research Technician,
Center for Space Research
Dr. Mark L. Schattenburg, Principle Research Scientist,
Assoc. Director, NanoStructures Laboratory

continued

continued

Related Research Facilities

NanoStructure Laboratory (NSL) Equipment

- Electron-beam Lithography
  IBM Vector Scan VS-2A, 50 KV
- Electron-beam Lithography
  (Raith turnkey system)
- Achromatic Interferometric Lithography System
  (Custom System)
- Interference lithography system
  (Custom System)
- Holographic-phase-shifting interferometer
  (Custom System)
- X-ray Lithography Systems
  (4 Custom Systems)
- IBBI x-ray mask aligner
  (Custom System)
- UV Lithography
  Tamarack ELHG 200-350
- Deep UV Aligner
  OAI 400
- Zone-plate-array lithography
  (Custom System)
- Reactive Ion Etchers
  Perkin Elmer Model 3140
  Plasma Therm Model 790
- Plasma Etcher
  Technics Plasma Etch II
- Surface Profiler
  Tencor Alpha Step 200
- Optical Microscopes (3)
  Leitz, Orthoplan, Metalloplan
- Electron Microscope
  Zeiss (LEO) 982 Gemini
- Ellipsometer
  Gaertner L116B
- Substrate Cleaning Station
  Interlab
- Evaporators
  Ebeam: Airco Temescal BJD 1800
  Thermal: Cooke MV VII CFR
- Gold Electroplating Systems
  (2 Custom Systems)
- Ion Miller
  Ion Tech
- RF Sputter System
  MRC 8620
- Linnik Interferometer
  Leitz
- Imaging Interferometer
  Wyko Model 400
- Optical Spectrometer
  EG&G/PARC Model 1235
- Atomic Force - Scanning Tunneling Microscope
  Digital Instruments Nanoscope
- UV Ozone Cleaner
  Jelight Model 42
- Workstation Computers (14)
  various types

continued

Related Research Facilities

Space Nanotechnology Laboratory (SNL)

1930 sq-ft of laboratory space comprised of:
1430 sq-ft Class 100 space
500 sq-ft support space

The Space Nanotechnology Laboratory (SNL) is located in the Center for Space Research (CSR). The SNL's mission is twofold: (1) develop and apply advanced lithographic and nanofabrication technology to build high performance space instrumentation, including X-ray telescopes, magnetospheric imaging, and solar physics instrumentation; and (2) develop subnanometer-accuracy metrology and assembly technology of interest to government and industry. Applications of these technologies include nanometer-period transmission gratings for high-resolution X-ray spectroscopy and UV/atom beam filtering/diffraction, ultra-low distortion gratings for sub-nanometer metrology and integrated optoelectronics, lithographic fabrication of super-smooth foil-optic X-ray mirrors and reflection gratings for X-ray astronomy, and micromachining of micro-opto-mechanical structures for nano-accurate optics assembly.

The SNL has participated in many flight missions. The SNL fabricated a large quantity of 200-400 nm-period X-ray transmission gratings for high-resolution spectroscopy with the NASA Chandra X-ray telescope, which is now sending back spectacular high-resolution X-ray images and spectra. The SNL has also fabricated solar X-ray/EUV transmission gratings for the NASA Solar and Heliospheric Observatory (SOHO) and the NOAA Geostationary Operational Environmental Satellites (GOES). The SNL fabricated UV-filter transmission gratings for neutral atom telescopes on the NASA Imager for Magnetopause-to-Aurora Global Exploration (IMAGE) now sending back spectacular neutral atom images of Earth's magnetosphere, and the NASA follow-on mission Two Wide-Angle Imaging Neutral-Atom Spectrometers (TWINS). The SNL is also participating in several pre-mission technology development efforts, including Constellation X and the Micro Arcsecond X-ray Imaging Mission (MAXIM).

The SNL is tightly integrated with research in the NanoStructures Laboratory (NSL). With support from NASA, DARPA, NSF, and other sponsors, the SNL/NSL collaboration has sustained a leadership position in several areas of advanced lithography research over the last two decades, including optical, electron beam, and X-ray, and interference lithographies. In particular, the SNL houses the interference-lithography facility that was originally developed in the NSL. Nanometer-period gratings and grids patterned with this system support research at MIT in sub-nanometer metrology, integrated opto-electronics, field-emitter flat-panel displays, and high-density magnetic storage.

Additional SNL facilities include a full complement of advanced plasma and chemical-etch pattern-transfer equipment, metal plating, bonding, and thin-film metrology equipment. Cleanroom consumables, such as ultrapure nitrogen and deionized water, are provided through physical connections to the MTL via inter-building conduits. Access to a full complement of CMOS, compound semiconductor, and MEMS fabrication equipment such as thin-film deposition and etch tools, and advanced metrology tools such as SEM and AFM, many key pieces funded by the SNL, is provided through access to the NanoStructures Laboratory and other MTL-affiliated laboratories.

continued

continued

Related Research Facilities

Space Nanotechnology Laboratory (SNL)

Research Staff

Dr. M.L. Schattenburg, Principal Research Scientist, CSR (Lab Director)
Dr. C.R. Canizares, Professor of Physics and Associate Provost (Faculty Associate)
J.M. Carter, Research Specialist, RLE
R. C. Fleming, Semiconductor Process Engineer, CSR (Lab Manager)
Dr. R.K. Heilmann, Research Scientist, CSR (Lab Assistant Director)
Dr. M. McGuirk, Sponsored Research Technical Staff, CSR
E. Murphy, Project Technician, CSR
Dr. G.S. Pati, CSR (Postdoctoral Associate)
Dr. G.R. Ricker, Senior Research Scientist, CSR (Faculty Associate)
Dr. H.I. Smith, Professor, EECS (Lab Associate Director)

Equipment

- Interference Lithography System (IL)
  (MIT-built system)
- Interference Lithography System, Scanning Beam (SBIL)
  (MIT-built system)
- UV Lithography
  OAI Model 30
- Wafer Developer
  SVG Wafertrack Model 8132
- Spin Coater/Dryer
  Specialty Coating Systems Model P6204A
- Bake Oven
  VWR Model 1601
- UV Ozone Cleaner
  Jelight Model 42
- Reactive Ion Etcher
  Plasma Therm Model 770
- Full Wafer Imaging Interferometer (RIE Endpoint)
  LES Model 1000-IS
- Gold Fountain-Bath Pulse-Plating System
  Marks and Associates
- Gold/Nickel Fountain-Bath Pulse-Plating System
  (MIT-built system)
- Acid Spin-Etch System
  Materials and Technologies RotoEtch III
- Three-Axis Adhesive Dispensing System
  CAMELOT Model 1414
- Bonding Aligner
  (MIT-built system)
- Optical Emission Spectrometer
  EG&G Model 1420
- Optical Microscopes (2)
  Leitz Ergolux, Wild M3Z
- Surface Profilometer
  Dektak III
- Thin Film Analyzer, X-ray Fluorescence
  Fisons Instruments/ Kevex Omicron

continued

Related Research Facilities

Space Nanotechnology Laboratory (SNL) Equipment

- Thin Film Stress Monitor
  Ionic Systems Model 3000
- Analytical Microbalance
  Denver Instruments
Model A-200DS
- Workstation Computers
  (15 of various types)
- Leak Checker, Helium
  Balzers Model HLT 150
- Residual Gas Analyzer (3)
  Leybold Transpector C100F
- Furnace
  NEY Vulcan 3-550
- Signal Analyzer
  HP 35670A
- Optical Surface Analyzer,
  Hartmann Test
  (MIT-built system)
- Optic Foil Assembly Truss
  (MIT-built system)

Lab of Organic Optoelectronics Professor Vladimir Bulovic

Our research is focused on deciphering the physical properties that govern behavior of nanostructured organic materials and applying the findings to development of practical, active organic technologies. With focus on electronic and optoelectronic structures, to date we demonstrated efficient LEDs, lasers, solar cells, photodetectors, transistors, memory cells, and chemical sensors. In addition to working on small-molecular-weight van-der-Waals-bonded organic thin films, we also examine hybrid organic/inorganic structures, polymer solids, and self-assembled materials. Our work tends towards the nano-scale where through development of new patterning and materials growth techniques we aim to reduce the size of active device layers from the present nano-scale thickness of organic thin films to that of single molecules or atomic clusters. Our ultimate goal is to utilize the nano-scale functionality of molecules, polymers, and inorganic/organic hybrid assemblies in practical nano-scale devices and both small- and large-area integrated systems.

continued

Related Research Facilities

Facility for High-Frequency Characterization of Devices and Structures
Professor Clifton G. Fonstad

In this facility, members of the MIT community can characterize the response of devices, circuits, and structures to sinusoidal signals at frequencies up to 40 GHz. The centerpiece of this facility is a Hewlett-Packard 8510 Vector Network Analyzer System with a 40 GHz s-parameter test set. Complementing this system is a Cascade Microwave Probe Station for direct, on-wafer measurements; packaged devices can also be measured in this facility. Other equipment which is available includes a Hewlett-Packard 4145 Semiconductor Parameter Analyzer and a Tektronix 370 Digital Curve Tracer, either of which can be used to select and maintain bias points for the active devices under test.

This facility was established in part through gifts made by Hewlett-Packard and Tektronix, and in part through contributions from MTL faculty members and researchers. The facility is available to members of the MIT community. At the present time no charge are made for the use of the facility, but users are required to supply their own probe tips for the Cascade prober.

Millimeter-Wave, THz, and Subpicosecond Facilities
Professor Qing Hu

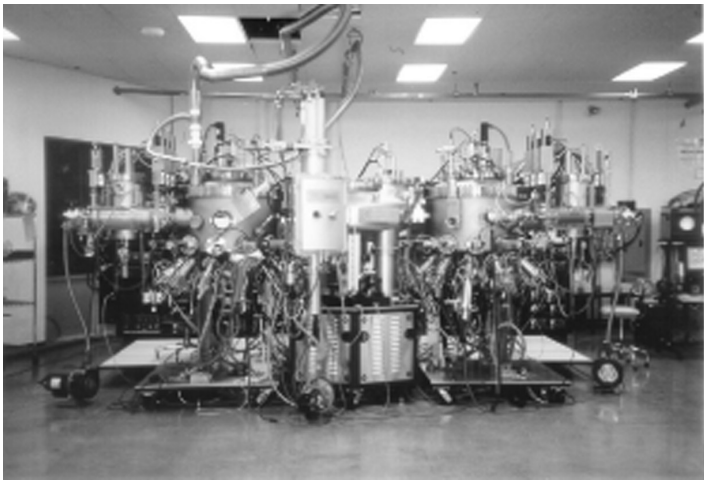
Professor Hu's laboratory is equipped with various millimeter-wave and infrared sources which can generate coherent and incoherent radiation from 75 GHz up to 30 THz. These include: Gunn oscillators at W-band frequencies (75 - 110 GHz); a frequency doubler, tripler, and quadrupler using Schottky diodes at 200, 300, and 400 GHz; an optically pumped far-infrared laser which generates coherent radiation from 245 GHz to 8 THz; and a far-infrared and an infrared Fourier transform spectrometer which are capable of performing linear spectroscopy from 45 GHz to 300 THz and beyond. This laboratory is also equipped with various cryogenic millimeter-wave and infrared detectors. These include: a Ge:Ga photoconductive detector, Si composite bolometers, InSb hot-electron bolometers, SIS (Superconductor-Insulator-Superconductor) receivers, and high Tc Josephson detectors. The laboratory also has a mode-locked Ti:sapphire laser that can generate optical pulses as short as 80 femtoseconds.

continued

Related Research Facilities

Facility for Growth and Processing of Compound Semiconductors
Professor Leslie A. Kolodziejski

In the compound semiconductor epitaxy facility, the growth of III-V materials is currently accomplished using gas source molecular beam epitaxy techniques. The modular epitaxy system consists of two gaseous source epitaxy reactors interconnected to several smaller chambers, which are used for sample introduction and in-situ surface analysis. The III-V Gas Source Molecular Beam Epitaxy (GSMBE) reactor is equipped with (1) solid elemental sources of Ga, In, Al, Si and Be, (2) gaseous hydride sources of arsenic and phosphorus, (3) an atomic hydrogen source and (4) an *in-situ* spectroscopic ellipsometer. The second gas source molecular beam epitaxy reactor was used for the growth of II-VI compound semiconductors using metalorganic, hydride, and solid sources.



The photograph shows the system during system acceptance at the factory.

The laboratory has recently purchased and taken the title of a new Veeco GEN 200 solid source, dual-reactor molecular beam epitaxy system (figure at right). The new system will allow for the epitaxial growth of dilute nitrides and antimony-based films in addition to arsenide- and phosphide-based films. The system platens can hold multiple 3″ or 4″ wafers, or a single 6″ or 8″ wafer. The system incorporates a low wobble manipulator that will allow *in-situ* feedback control of the epitaxial processes using optical sensors such as band edge absorption and spectroscopic ellipsometry. The system is currently awaiting the completion of the new laboratory at MIT.

MTL Memo Series

The MIT Microsystems Technology Laboratories (MTL) maintains a comprehensive pre-publication Memo Series covering the activities of MTL and related microsystems research at MIT. A chronological list of the memos issued in 2002 appears below. Copies of MTL Memos are available online exclusively to individuals whose companies are members of the Microsystems Industrial Group (MIG) at MTL. MIG members are invited to sign up for an account that will grant them access to these materials in a password-protected directory.

To sign up for a MTL Web Member account, use MTL's sign-up form online at *www-mtl.mit.edu/memberservices/* Materials can be accessed online at *www-mtl.mit.edu/mtlhome/members_only/:SSL*

02-1046 "Enhanced Performance of Optical Sources in III-V Materials Using Photonic Crystals," Alexei Andrew Erchak (216 pgs).

02-1047 "CMOS Passive Pixel Imager Design Techniques," Iliana Fujimori (122 pgs).

02-1048 "A Microbubble-Powered Bioparticle Actuator, Rebecca A. Braff, Antimony L. Gerhardt, Martin A. Schmidt, Martha L. Gray, and Mehmet Toner (4 pgs).

02-1049 "An Open-Source Export Package for the MIT Microelectronics WebLab, " James L. Hardison (43 pgs).

02-1050 "Integrated Optical Filters using Bragg Gratings and Resonators," Mohammad Jalal Khan (213 pgs).

02-1051 "Development of X-Ray Lithography and Nanofabrication Techniques for III-V Optical Devices," Michael Lim (122 pgs).

02-1052 "Hydraulic Amplification for Actuation in MicroElectroMechanical Systems, " J. Lodewyk Steyn (218 pgs).

02-1053 "Active Optical Clock Distribution ," Travis L. Simpkins (10 pgs).

02-1054 "Oversampled Pipeline A/D Converter with Mismatch Shaping," Ayman U. Shabra (141 pgs).

02-1055 "Efficient Light Emitting Devices Utilizing CdSe (ZnS) Quantum Dotsin Organic Host Matrices," Seth A. Coe (32 pgs).

02-1056 "BiCMOS RF Mixer for 5-Ghz Receivers," Michael W. Baker (119 pgs).

02-1057 "Variation Aware Design of Data Receiver Circuits for On-Chip Optical Interconnect," Michael J. Mills (126 pgs).

02-1058 "Circuit Techniques for Subthreshold Leakage Reduction in a Deep Sub-Micron Process," Benton Highsmith Calhoun (118 pgs).

02-1059 "Energy Efficient Operating Systems and Software," Amit Sinha (177 pgs).

02-1060 "Achieving Large Stable Vertical Displacement in Surface-Micromachined Microelectromechanical Systems (MEMS)," Erik R. Deutsch (80 pgs).

continued

continued

MTL Memo Series

02-1061 "Microfabricated Cross-Flow Chemical Reactor for Catalyst Testing," Sameer K. Ajmera, Cyril Delattre, Martin A. Schmidt, and Klavs F. Jensen (10 pgs).

02-1062 "Interconnect Modeling and Optimization in Deep Sub-Micron Technologies," Paul Peter P. Sotiriadis (233 pgs).

02-1063 "Feedback Circuit for Organic LED Active-Matrix Display Drivers," Eko T. Lisuwandi (61 pgs).

02-1064 "Chip-Scale Modeling of Pattern Dependencies in Copper Chemical Mechanical Polishing Processes," Tamba E. Gbondo-Tugbawa (232 pgs).

02-1065 "Investigation of Noise Sources in Scaled CMOS Field-Effect Transitors," Todd C. Sepke (111 pgs).

02-1066 "Modeling of Chemical Mechanical Polishing for Shallow Trench Isolation," Brian Lee (201 pgs).

02-1067 "Characterization and Modeling of Pattern Dependencies in Copper Interconnects for Integrated Circuits," Tae Hong Park (204 pgs).

02-1068 "Multivariate Endpoint Detection of Plasma Etching Processes," Brian E. Goodlin (226 pgs).

02-1069 "A Ring Oscillator Based Variation Test Chip," Joseph Panganiban (174 pgs).

02-1070 "Extraction of Variation Sources Due to Layout Practices," Karen Gonzalez-Valentin (107 pgs).

02-1071 "Maskless Parallel Patterning With Zone Plate Array Lithography (ZPAL)," Dario Gil (170 pgs).

02-1072 "Fabrication of a Planar Optical Add/Drop Channel Filter in Silicon Oxynitride," Joseph C. Huang (73 pgs).

02-1073 "Zone Plate Array Lithography (ZPAL): Simulations and System Design," Rajesh Menon (109 pgs).

02-1074 "Circuit Design and Technological Limitations of Silicon RFICs for Wireless Applications," Donald A. Hitko (206 pgs).

MTL VLSI Seminar Series

The Microsystems Technology Laboratories (MTL) hosts a series of talks each semester known as the MTL VLSI Seminar Series. Speakers for the Series are selected on the basis of their knowledge and competence in the areas of microelectronics research, manufacturing, or policy. The MTL VLSI Seminar Series is held on the MIT Campus on Tuesdays at 4:00 pm, and is open to the public.

A listing of recent seminars is also provided at *www-mtl.mit.edu/mtlhome/9Semi/Previous.html*. For information regarding the MTL VLSI Seminar Series, please write to the Microsystems Technology Laboratories; Room 39-321; MIT; 77 Massachusetts Avenue; Cambridge, MA 02139. Our fax number is (617) 253-9622, or you may send e-mail to debb@mtl.mit.edu.

Streaming videos of the VLSI Seminar Series are available online exclusively to individuals whose companies are members of the Microsystems Industrial Group (MIG) at MTL. MIG members are invited to sign up for an account that will grant them access to these materials in a password-protected directory (See instruction at "MTL Memo Series," p. 406).

Fall 2002

September 10	Krishnamurthy Soumyanath, Intel Corporation Challenges and Opportunities for Mixed Signal Systems in Sub 100nm CMOS Technologies
September 24	Pushkar Apte, McKinsey New Business Models in the "Atomizing" Semiconductor Industry
October 1	Mark Rodwell Submicron Scaling of InP Bipolar Transistors: Device Design, Scaling Laws, Technology Roadmaps, and Advanced Fabrication Processes.
October 8	Jeff Welser, IBM High Performance CMOS Design at IBM
October 29	Cherie Kagan, IBM Materials for Molecular Devices
November 5	Wanda Gass, Texas Instruments Digital Signal Processors: Past, Present, and Future
November 12	Joachim Burghartz, Delft University Add-on Process Modules for RF Silicon Technology
November 19	Hans Stork, Texas Instruments Sub 100 nm Process Development for System-on-Chip Devices

continued

continued

MTL VLSI Seminar Series

Spring 2003

March 4	Kerry Bernstein, IBM Microelectronics Process, Environmental, and Design Contributions to CMOS Delay Variation
March 18	Bob Rao, Intel Corporation MEMS Research at Intel
April 1	David Su, Atheros Communications Inc. Design Challenges in CMOS Transceiver for WLAN
April 8	John Paul Mattia, Big Bear Network Intelligent Optoelectronics for 10 and 40 Gb/s Transmission
April 15	P. K. Roy, Tokyo Electron Ltd (TEL) Extending Moore's Law: A Material Scientist's Point of View
April 29	Brian Halla, National Semiconductor Corporation A Technology Boom's in "Sight"? You Ain't Seen Nothin' Yet!
May 6	Kelin Kuhn, Intel Corporation RF/Analog Integration with 90nm digiDal CMOS

Abbreviations

Massachusetts Institute of Technology

ACC	Advanced Concepts Committee (MIT LL)
CAES	Center for Advanced Engineering Study
ChE	Chemical Engineering
CICS	Center for Integrated Circuits and Systems
CMSE	Center for Materials Science and Engineering
CSR	Center for Space Research
EECS	Department of Electrical Engineering and Computer Science
HST	Health Sciences and Technology, Harvard-MIT
ICL	Integrated Circuits Laboratory
ITRC	Intelligent Transportation Research Center
LFM	Leaders for Manufacturing
MIG	Microsystems Industrial Group
MIT	Massachusetts Institute of Technology
MPC	Materials Processing Center
MSE	Department of Materials Science and Engineering
MTL	Microsystems Technology Laboratories
NSL	NanoStructures Laboratory
RLE	Research Laboratory of Electronics
SML	Space Microstructures Laboratory
TRL	Technology Research Laboratory
UROP	Undergraduate Research Opportunities Program

Sponsors

Private

AMD	Advanced Micro Devices
AT&T	American Telephone and Telegraph
GE	General Electric Company
IBM	International Business Machines Corporation
MARCO	Microelectronics Advanced Research Corporation
NTT	Nippon Telephone and Telegraph
OIDA	Optoelectronics Industry Development Association
JOP	Joint Optoelectronics Program
SAO	Harvard-Smithsonian Astrophysical Observatory
SIA	Semiconductor Industry Association
SRC	Semiconductor Research Corporation
SwRI	Southwest Research Institute
TI	Texas Instruments
TMA	Technology Modeling Associates, Inc.
TSMC	Taiwan Semiconductor Manufacturing Corporation

continued

continued

Abbreviations

Sponsors

Government

AFOSR	U. S. Air Force Office of Scientific Research
ARPA	Advanced Research Projects Agency
ARO	U. S. Army Research Office
AXAF	Advanced X-ray Astrophysics Facility - (NASA)
CSE	Consortium on Superconducting Electronic
DOD	Department of Defense
JPL	Jet Propulsion Laboratories
JSEP	Joint Services Electronics Program
LANL	Los Alamos National Laboratory
MRSEC	Materials Research Science and Engineering Center
NASA	National Aeronautics and Space Administration
NCIPT	National Center for Integrated Photonics Technology
NIH	National Institute of Health
NIST	National Institute of Standards and Technology
NOAA	National Atmospheric and Oceanographic Administration
NREL	National Renewable Energy Laboratory
NRL	Naval Research Laboratory
NSA	National Security Administration
NSF	National Science Foundation
ONR	Office of Naval Research

Other

CFI	CAD Framework Initiative
CIM	Computer Integrated Manufacturing
IEEE	Institute of Electrical and Electronics Engineers
IEDM	International Electronic Devices Meeting
HARC	Houston Advanced Research Center
MCNC	Microelectronics Center of North Carolina
MRS	Materials Research Society
NATO	North Atlantic Treaty Organization
NTCIP	National Transportation Communications for Intelligent Transportation Systems Protocol
STW	Dutch Technology Foundation
UCLA	University of California at Los Angeles
ULSI	Ultra Large Scale Integration
VLSI	Very Large Scale Integration

Faculty and Senior Research Scientist Reference Index

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Faculty and Senior Research Scientist Reference Index

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Faculty and Senior Research Scientist Reference Index

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Faculty and Senior Research Scientist Reference Index

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Faculty and Senior Research Scientist Reference Index

continued

Faculty and Senior Research Scientist Reference Index

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