Improved Critical-Current-Density Uniformity of Nb Superconducting Fabrication Process Using Anodization

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Sponsorship

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We studied an anodization technique for a Nb/Al/AlO_x/Nb trilayer process which provides a significant improvement in critical-current-density J_c uniformity across a 150-mm-diameter wafer. Anodization is an electrolytic process in which the surface of a metal is converted to its oxide form, this metal oxide layer serves as a protective barrier to further ionic or electron flow. The superconducting Josephson junctions were fabricated in a class-10 cleanroom facility at MIT Lincoln Laboratory. The Nb superconducting process uses optical projection lithography, chemical mechanical planarization of two oxide layers, a self-aligned via process and dry Reactive Ion Etching (RIE) of the Nb and oxide layers. The most critical step in the fabrication process however is the definition of the tunnel junction. The junction consists of two Nb layers, the Base Electrode (B.E.) and Counter-Electrode (C.E.) separated by a thin AlO_x barrier. Figure 5a shows a cross-section of the Josephson junction region after RIE is performed on the counter-electrode. After RIE, the junction perimeter is exposed to the atmosphere and is therefore vulnerable to chemical and/or plasma damage. Anodization is useful in minimizing damage to the junction region (Figure 5b).

Critical current I_c measurements of Josephson junctions were performed at room temperature using specially designed test structures. We used an automatic probing station to determine the I_c values of junctions across the entire wafer. The J_c uniformity of anodized/unanodized wafer pairs, fabricated together, were compared. The cross-wafer standard deviation of J_c was typically ~ 5% for anodized wafers but was ≥15% for unanodized wafers (Figure 6). A low variation in J_c results in a higher yield of device chips per wafer with the desired current density. As a result of the improved cross-wafer distribution, the cross-chip uniformity is greatly improved as well; typically < 1% for anodized chips. Low cross-chip J_c variation is for fast digital superconducting electronics.

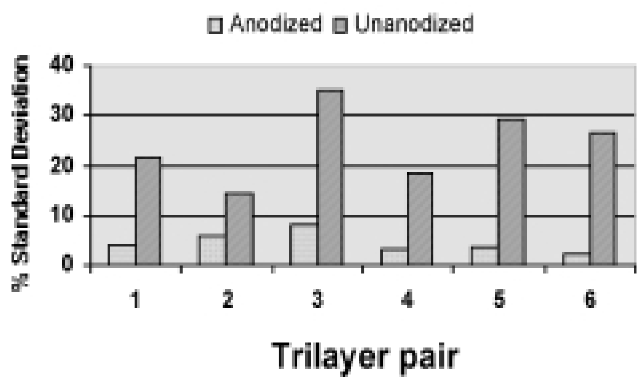

Fig. 6: Comparison of cross wafer critical current density standard deviation of anodized/unanodized wafer pairs.

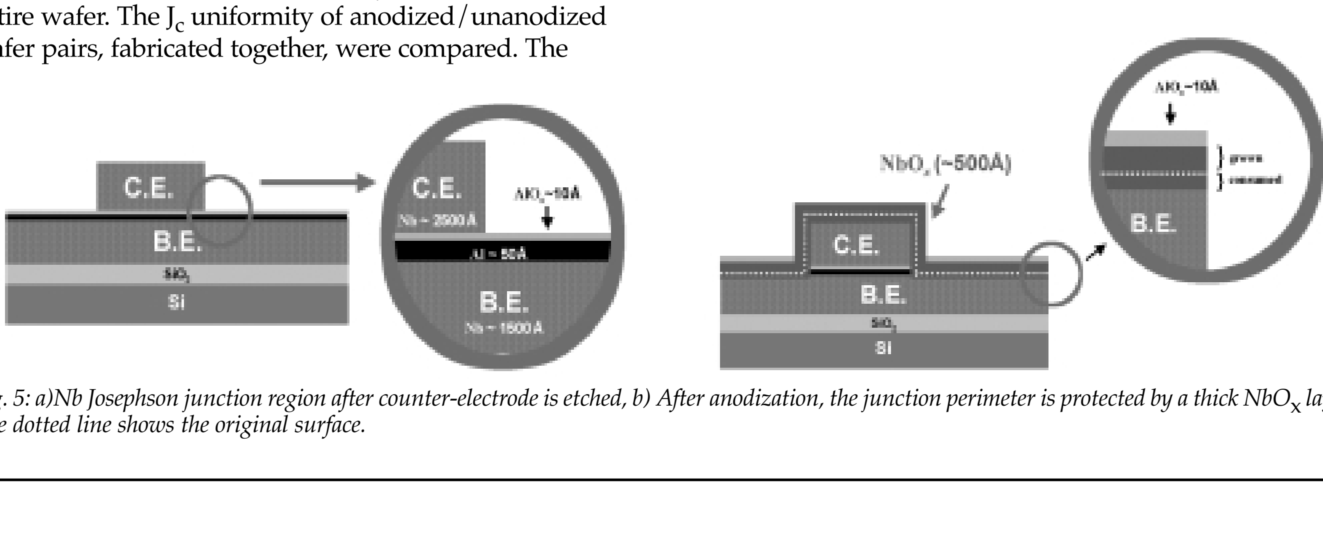

Fig. 5: a)Nb Josephson junction region after counter-electrode is etched, b) After anodization, the junction perimeter is protected by a thick NbO_x layer. The dotted line shows the original surface.