Data Receiver Circuits for On-Chip Optical Interconnect

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Sponsorship
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Alternative interconnect architectures for on-chip data communication are of substantial interest to overcome speed and signal integrity concerns in future electrical interconnect. In this work, we have developed and analyzed an on-chip optical data receiver circuit, with potential application to future on-chip guided wave distribution networks (as shown in Figure 37).

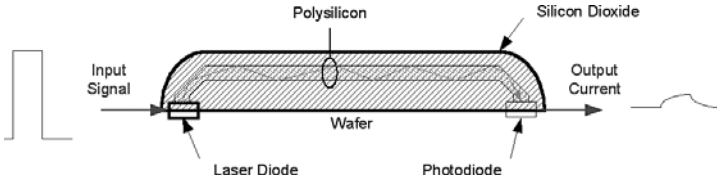

Fig. 37: Summary of Guided-Wave Approach

The optical data receiver circuit amplifies small currents from a photodiode into full range digital signals. The design uses a two-phase sense amplifier, as illustrated in Figure 38. Small input signals build up a differential across the input, which is transformed into a rail-to-rail signal during the second phase using positive feedback. Each group of data bits is accompanied by an additional "1" bit to establish a reference switching threshold. Variation between the input and reference side increase the total time needed to evaluate an input signal. The circuits were fabricated in December 2001, using 0.18 mm CMOS technology.

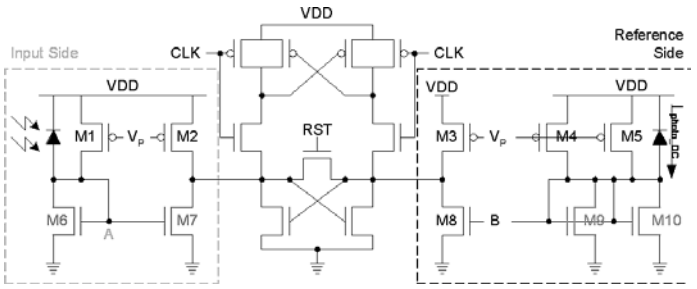

Fig. 38: Receiver Circuit, Consisting of Input Stage, Sense Amplifier, and Reference Circuit

The large photodiode capacitance is isolated using a current mirror. Additional transistors maintain a DC level of bias current through the mirrors, thereby setting the transimpedance gain. Combining two sets of bias current with the on current of a photodiode and dividing by two creates a reference voltage. This is equivalent to an input with exactly half of the steady state optical power for a "one" bit.

Uniform variation across the circuit has only a minimal impact on performance, but asymmetrical variation significantly decreases evaluation speed as shown in Figure 39. Therefore, as with all sense amplifier topologies, matching between sides is of the utmost concern.

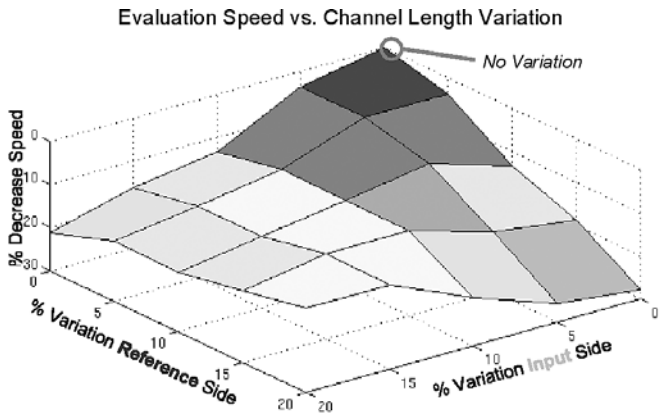

Fig. 39: Changes in Evaluation Speed Caused by Channel Length Variation