

# Design and Variation Analysis of an On-Chip Optical Clock Receiver Circuit

## Personnel

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## Sponsorship

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As deep sub-micron CMOS technology continues to scale, decreasing gate lengths and line widths introduce greater variation, propagation delay, crosstalk and other parasitics into clock distribution networks. Typical H-Tree and other balanced clock distribution schemes are becoming increasingly vulnerable to these effects, particularly to line-width variation and increased propagation delay. Often, buffers are inserted into the network so the total load seen at any segment of the network is decreased. However, buffers cannot compensate for line-width variation and crosstalk. Furthermore, power dissipation in the clock distribution network is becoming a significant fraction of the overall power budget.

An alternative to balanced electrical clock distribution networks is the use of an optical distribution network at the global level (Figure 35). Light can be distributed to multiple receivers across the chip with low skew. If this light can be efficiently converted to an electrical signal, this idea becomes a viable alternative. Thus optical receiver circuit design and analysis is a critical step toward implementation of on-chip optical clocks.

A first-generation receiver circuit was designed using a transimpedance amplifier as a preamplifier followed by a string of inverters biased using a replica biasing network (S. Sam). This circuit showed that power supply noise and gate length variation introduce considerable skew (100 ps and 80 ps respectively) into the recovered electrical signal and effectively limited the optical clock speed. A second-generation receiver circuit employing cascode gain stages, feedback biasing, a bandgap voltage reference and a linear voltage regulator (Figure 36) has been designed and fabricated (TSMC 0.18  $\mu\text{m}$ ) with robustness to power supply and biasing variation in mind. Testing of the fabricated circuit is ongoing. Simulations show that while skew due to power supply noise decreases dramatically (24 ps compared to 100 ps in the first-generation), threshold voltage ( $V_t$ ) variation introduces an increased amount of skew (70ps) into the electric signal. Furthermore, the size and power con-

sumption of the circuit may make it infeasible for practical application.

The second generation circuit design indicates that further improvements are needed to achieve practical, variation-robust on-chip optical receiver circuits. Differential signaling, additional feedback biasing, and adaptive biasing are being explored to overcome photodiode current variation, duty-cycle variation and threshold voltage variation while reducing area and power dissipation.

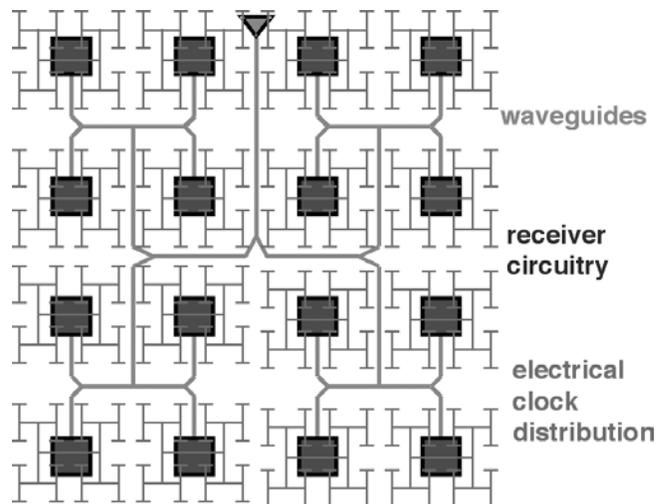


Fig. 35: Global optical clock with local electrical clock distribution.

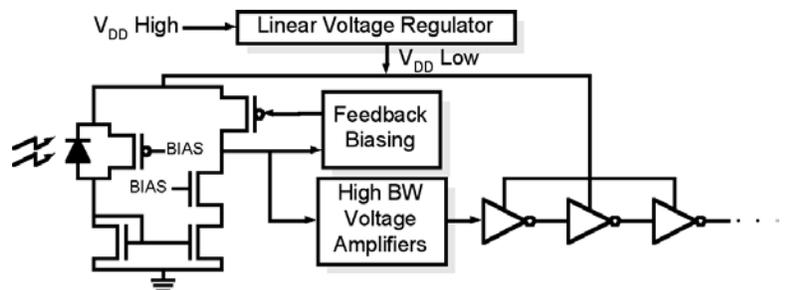


Fig. 36: Second generation clock receiver circuit.