Application of Aligned Pillar Bonding to Optical Clock Distribution on Si-CMOS

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One of the most significant factors limiting future microprocessor performance and one of the great consumers of microprocessor power is the clock distribution network. As clock rates continue to rise, the design of the clock distribution network will assume an increased importance. From the power point of view, the H-tree or other networks that distribute the global clock to functional sub-units are continually growing and must be charged and discharged during each cycle. From the performance point of view, as die sizes and clock rates increase, clock skew becomes very significant.

Clock skew may be divided into two classes. The first may be called deterministic clock skew and refers to the difference in time required for the global clock to reach different units of the chip. H-tree networks attempt to compensate for this skew by forcing an approximately equal path length from the global clock generator to all respective areas of the chip. The penalty in this case is increased capacitance, and therefore power consumption, as "filler" line is inserted in the network. Deterministic skew is relatively benign since it may be extracted from a chip layout and compensated for in the integrated circuit. The other form of clock skew may be called random and refers to the difference in arrival time of a clock edge due to process variation (e.g. thickness of intermetal dielectric or width of metal line). Since this skew is process-dependent (and therefore also time- and location-dependent assuming an unchanging process), it is not possible to compensate for it at the design stage. Circuits must instead be designed conservatively to tolerate a certain degree of random skew, and this sort of design limits performance.

Optical clock distribution could address all of the above problems. Depending on the scheme in use, deterministic skew may be significantly reduced. A global optical clock would also decrease power consumption as large metal lines (designed for high current-carrying capacity) would no longer require charging at each clock cycle. Optical distribution would also avoid a good deal of random skew for the same reason. Random skew in this design would be contributed my process variations affecting the performance of the optical receivers of the global clock. Circuit techniques to perform compensation of this sort of variation are being investigated and developed by Prof. Boning and his group.

In this work, InP-InGaAs PiN diodes are used to provide a photocurrent. The performance of these diodes depends strongly on the thickness of the i-layer and the area of the devices. The former factor is very strictly controlled as the devices are grown by MBE. The latter factor is not a significant issue since device dimensions are significantly larger than the expected variation of the photolithography and etching processes. As shown in Figure 34, the diodes will be bonded to 0.18u Si-

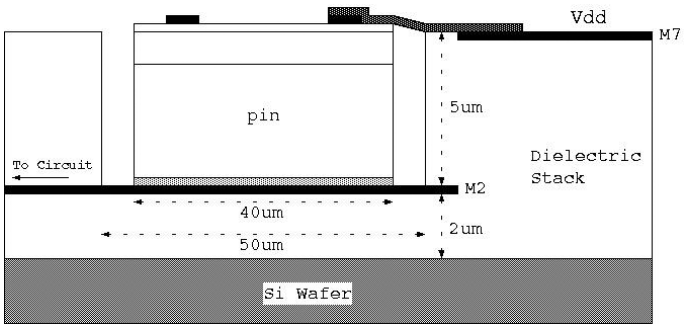

Fig. 34: Cross-sectional drawing illustrating a InP-InGaAs PiN photodiode ABP integrated on a CMOS integrated circuit chip for use in optical clock distribution studies.

CMOS test chips manufactured at Taiwan Semiconductor Manufacturing Company (designed by Prof. Boning and his group). Bonding will be done using the APB process onto the chip's Metal-2 layer.The bonding metallization is CMOS-compatible and will

absorb the plastic stress of the thermal mismatch between the silicon target wafer and the III-V diodes. Following bonding, the diodes will be processed in place on the chip by the deposition of ohmic contacts, a mesa etch to control dark current, passivation dielectric material, and a metal line to join the diode ohmic contacts with Metal-7 Vdd lines.