Aligned Pillar Bonding Technology for Heterogeneous Integration

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A new heterogeneous integration technique is under development which uses aligned, selective-area bonding to integrate III-V heterostructure devices, such as laser diodes and p-i-n detectors, with commercially-processed electronic integrated circuits to create optoelectronic integrated circuits (OEICs) with VLSI levels of density and complexity. This technique has been named Aligned Pillar Bonding (APB); it is illustrated in Figure 33. The APB technique is similar in function to the Epitaxy-on-Electronics (EoE) technique in which III-V device heterostructures are first grown epitaxially in dielectric growth windows exposing the substrate surface in selected areas on fully-processed GaAs integrated circuit wafers. The APB process used bonding rather than direct selective area epitaxy to add heterostructures to processed IC wafers. It is compatible with any VLSI process on wafers that match the thermal expansion coefficient of the heterostructure wafer, meaning that GaAs-based heterostructures can be APB-integrated on both GaAs IC wafers and on silicon-on-sapphire IC wafers.

In the APB technique, the heterostructure for an optoelectronic device, such as a laser diode, is first grown under optimal conditions on the optimal substrate. The heterostructure is then patterned into pillars, which are in turn wafer fusion bonded into dielectric windows on a suitably prepared integrated circuit wafer (i.e., into the same windows that would be used for epitaxy in the Epitaxy-on-Electronics process). Doing this requires something more complex than encountered in previous III-V bonding experiments, namely alignment. The wafer on which the device heterostructure is grown and the pillars are formed, called the "source" wafer, must be aligned with the dielectric windows on the integrated circuit wafer onto which the devices are to be bonded. This wafer is called the "target wafer.

We have developed techniques using equipment developed originally for MEMS processing for achieving this alignment, and have demonstrated for the first time the successful aligned fusion of III-V pillars in dielectric windows on a GaAs IC chip. We have also demonstrated the subsequent removal of the substrate of the source wafer to complete the transfer of the pillars to the target wafer. Our initial work involved direct semiconductor-to-semiconductor bonding and required sub-

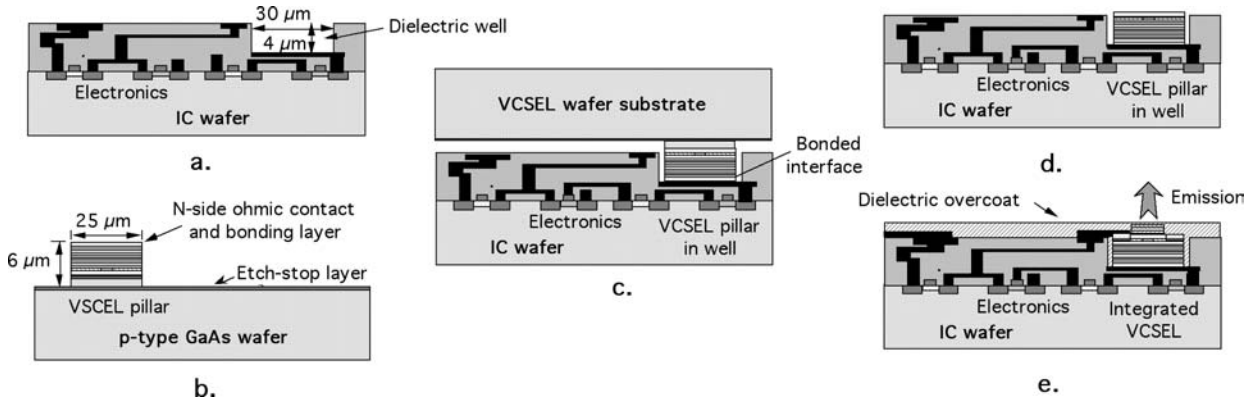

Fig. 33: The APB process: (a) the processed IC wafer as received from the manufacturer, and (b) the p-side down VCSEL wafer with pillars etched to match the windows on the IC wafer; (c) after bonding of the VCSEL and IC wafer; (d) after removal of the substrate of the VCSEL wafer leaving VCSEL heterostructures bonded in the windows; and (e) after completing device processing and integration.

stantial pressure to achieve contact and bonding. Subsequent work has investigated layered gold alloy-to-GaAs, palladium-to-GaAs and layered tin and palladium-to-GaAs bonding. All three have been successfully demonstrated, and work is continuing, with emphasis on the last system because the tin is expected to compensate for non-uniformities and slight misalignments during bonding, while also providing a superior electrical contact to palladium alone. We have established a collaboration with a group in Germany growing vertical-cavity surface-emitting laser (VCSEL) layers with the goal of using the APB technique to integrate VCSELs on, for example, OPTOCHIP die, and we have begun a new collaborative effort with Professor Dana Brooks at Northeastern University to develop biomedical sensors arrays (see the appropriate section below). We have also established a collaboration with Professor Yoon Fait Soon in Singapore to grow InP-based PiN detector epilayers to integrate detectors on OEIC-6 die and on CMOS die designed by Professor Duane Boning and his students at MIT (see the appropriate section below).