

Modeling of Advanced Devices

Personnel

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Sponsorship

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Direct quantitative 2-D characterization of sub-50 nm MOSFETs continues to be elusive. This research develops a comprehensive indirect inverse modeling technique for extracting the 2-D device topology using combined $\log(I)$ -V and C-V data. An optimization loop minimizes the error between a broad range of simulated and measured electrical characteristics by adjusting parameterized doping profiles. The extracted profiles are reliable in that they exhibit decreased RMS error as the doping parameterization becomes increasingly comprehensive of doping features.

The inverse modeling methodology pieces together complementary MOSFET data sets such as Cgg of the gate stack, process simulation for initial guess, 1-D doping analysis, subthreshold I-V which is a strong function of 2-D doping, and Cgsd-V data which is especially sensitive to the source/drain. Figure 9 shows how combining the data sets enhances the extracted profiles of a $T_{ox} = 3.3$ nm NMOS device family. Such profiles serve as a basis for tuning diffusion coefficients in order to realistically calibrate modern process simulators.

An important use of this technique is in the calibration of carrier transport models. With an accurate device topology, the transport model parameters can be adjusted to predict the on-state behavior. Utilizing a mobility model that conforms to the experimental effective field dependence and including a correction for parasitic resistance, the engineer calibrates the transport model for an advanced NMOS generation at various gate lengths and voltages as in Figure 10. Employing the Energy Balance model yields an energy relaxation value valid over all device nodes.

Furthermore, what has been learned from profile and transport calibration is applicable to investigating optimal paths for sub-20 nm MOSFET scaling. In a study of candidate architectures such as double-gate, single-gate, and bulk-Si, the power versus performance trade-off

was analyzed as a function of gate length and work-function.

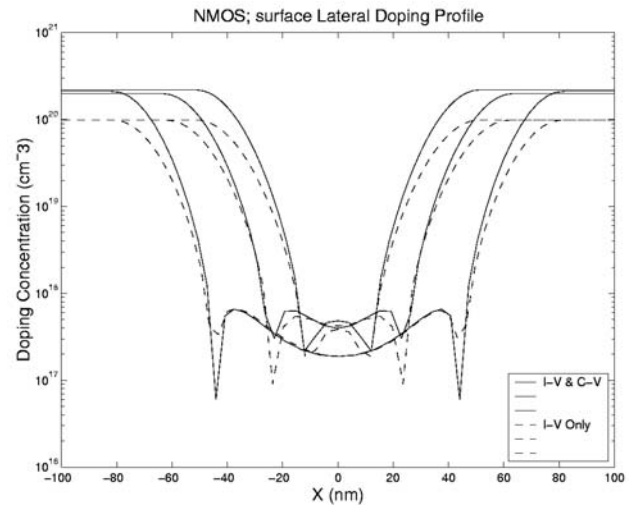


Fig. 9: Comparison between the extracted lateral doping profiles at the surface using combined "I-V & C-V" data versus "I-V Only" data on a $T_{ox} = 3.3$ nm NMOS family with various gate lengths.

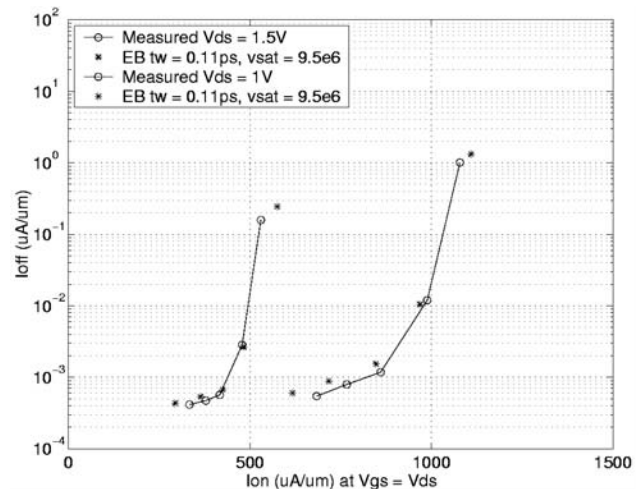


Fig. 10: The leakage current I_{off} versus drive current I_{on} curve of a state-of-the-art NMOS family with $T_{ox} = 17\text{\AA}$. The Energy Balance transport model has been adjusted using the inverse modeled profiles to match the experimental results for various I_{eff} nodes.