Integrated Chip-Scale Simulation of Pattern Dependencies in Copper Electroplating and Chemical Mechanical Polishing Processes

Personnel

T. Tugbawa and T. Park (D. Boning)

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Copper CMP is recognized to suffer from pattern dependent problems such as dishing and erosion, which cause increased metal line resistance and surface non-uniformity. The amount of dishing and erosion across an entire chip depends on the electroplated topography, the CMP process parameters (down force, table speed, slurry flow rate, etc.) and consumables, and the layout patterns. The electroplated topography itself depends on the layout patterns, further complicating the prediction of dishing and erosion during CMP. Efficient chip-level simulation of final copper line and structure thicknesses therefore requires an integrated copper electroplating and copper CMP modeling methodology.

For chip-level modeling, a given chip is first discretized into 40 µm by 40 µm cells. A layout extractor is used to compute the average, minimum, and maximum line widths, line lengths, and line spaces respectively in each of the cells. In addition, the local layout densities and the line width distributions are also computed in each cell. The plating model uses this information to compute the step-heights, copper thicknesses (average, minimum, and maximum), and the electroplated local copper densities in each cell, for a given electroplating process as shown in Figure 1. The outputs of the plating model, the local layout densities, line widths and line spaces, the CMP polish time, and other details of the copper CMP process (which are contained in the extracted CMP modeling parameters) serve as the inputs for the copper CMP model. This model computes dishing and erosion in each of the 40 µm by 40 µm cells, and the simulated result for the entire chip is shown in Figure 2.



Step Height Envelope Fig. 1: *Electroplating topography simulation; RMS error is ~* 300 Å.



Fig. 2: CMP simulation for dishing and erosion. Dishing has RMS error of 175 Å; erosion has RMS error of 355 Å.