High Mobility Strained Si/SiGe Heterostructure MOSFETs

Personnel
C. W. Leitz (E. A. Fitzgerald and D. A. Antoniadis)

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Strained Si- and SiGe-based heterostructure MOSFETs grown on relaxed SiGe virtual substrates exhibit dramatic electron and hole mobility enhancements over bulk Si, making them promising candidates for next generation CMOS devices. The most heavily investigated heterostructures consist of a single strained Si layer grown upon a relaxed SiGe substrate. While this configuration offers significant performance gains for CMOS, hole mobility is still much lower than electron mobility. By contrast, the combination of buried compressively strained $Si_{1-y}Ge_y$ layers and tensile strained Si surface layers grown on relaxed Si1-xGex virtual substrates, hereafter referred to as dual channel heterostructures, offers nearly symmetric electron and hole mobilities without compromising n-MOSFET performance. To investigate these heterostructures, we have studied the impact of various channel engineering parameters on channel mobility in long channel MOSFETs. In these experiments, MOSFETs are fabricated by a novel short flow process utilizing a deposited gate dielectric and only one lithography step. This type of device allows us to measure effective mobility at vertical fields approaching 1 MV/cm, thereby enabling us to quickly explore the impact of materials parameters on channel mobility at fields approaching those of state-of-the-art MOSFETs. With this approach, we have achieved hole mobility enhancement factors over bulk Si of 5.15 for dual channel heterostructure devices. By employing different virtual substrate compositions, we have decoupled the effects of strain and alloy scattering in both tensile strained surface channels and compressively strained buried channels. In tensile strained surface channels, alloy scattering degrades electron mobility much more severely than hole mobility. In compressively strained buried channels, high hole mobility is attainable even for mid-Ge-contents where alloy scattering is expected to be most severe. Figure 17 (next column) details the effect of varying buried channel composition, under constant strain (y – x = 30% Ge), on hole mobility in dual channel heterostructure p-MOSFETs.

Note that hole mobility for all dual channel configurations exceeds hole mobility in bulk Si and strained Si heterostructures. By adopting the combination of a strained Si surface channel and buried Si0.2Ge0.8 buried channel, grown on a relaxed Si0.5Ge0.5 virtual substrate, we have obtained nearly symmetric electron and hole mobility in the same heterostructure (with both electron and hole mobility enhanced relative to bulk Si). Overall, we have demonstrated that dual channel heterostructures provide excellent performance gains for both n- and p-MOSFETs.

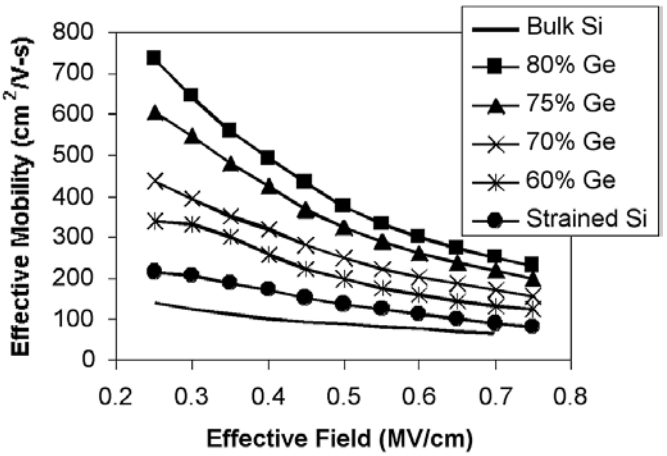

Fig. 17: Effective hole mobility versus effective vertical field for dual channel heterostructures under constant strain (y – x = 30% Ge) compared to a strained Si p-MOSFET. All channel thicknesses in dual channel heterostructures are 85 Å. Hole mobility in dual channel heterostructures increases with buried channel Ge composition.