Strained Ge *p*-type and *n*-type MOSFETs Fabricated on $Si_{1-x}Ge_x$ Virtual Substrates

Personnel

M. L. Lee, C.W. Leitz, A.J. Pitera, D.A. Antoniadis, and E.A. Fitzgerald

Sponsorship

Hanscom AirForce Base, Singapore-MIT Alliance Program, and NSF/MRSEC

We have fabricated strained Ge p-type and n-type Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) on relaxed $Si_{1-x}Ge_x$ graded buffers. Poor chemical and mechanical stability prohibits the use of germanium dioxide (GeO_2) as a gate dielectric for Ge devices, and bulk Ge wafers are not available in the sizes currently used in leading edge Si CMOS fabrication facilities. To accommodate the wafer incompatibility, Ge-based devices in this research are fabricated on relaxed SiGe grown on Si wafers, and to avoid the use of GeO_2, a thin epitaxial Si layer is grown on top of the strained Ge channel. The Si cap allows a high quality interface to be formed with a conventional SiO_2 gate and ensures basic compatibility with conventional Si CMOS processing. For strained Ge layers on relaxed SiGe, the valence band is offset from the relaxed virtual substrate below the channel and the Si above, resulting in a well for holes. Furthermore, compressive strain reduces the hole effective mass and lifts the valence band degeneracy in Ge. In our devices, Ge layers were grown on $Si_{1-x}Ge_x$ (x=0.7 to 1.0) and capped with Si in all cases. The high Ge content in the virtual substrate results in lattice mismatch of 2.8% to 4% for the Si layer, and considerable relaxation ensues as the cap is grown. Despite the defects in the Si layer, significant mobility enhancements for the p-MOSFETs were measured for all virtual substrate compositions, demonstrating the concept of Si as a universal cap material for a wide range of lattice constants. A sample with a 115 Å Ge channel grown on a $Si_{0.3}Ge_{0.7}$ virtual substrate exhibited hole mobility enhancements greater than 8 times over bulk Si. Further, by holding the Si cap thickness at 50Å or less, the hole mobility enhancement could be completely preserved at a wide range of vertical effective fields. The conduction band in the strained Ge MOSFET differs from the valence band, because the type-II band alignment of the strained Ge and Si cap forms a well at the surface for electrons. *n*-MOSFETs consisting of a 60Å strained Ge layer grown on a $Si_{0.3}Ge_{0.7}$ virtual substrate and capped with 45Å of Si exhibit electron mobility enhancements of 1.50 (±0.15) times over bulk Si. The observed mobility enhancement indicates that a high density of defects in the surface layer does not preclude high electron mobility.

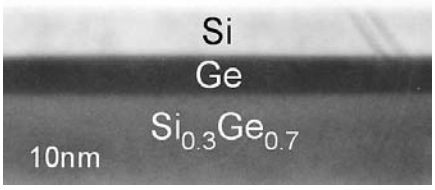

Fig. 15: TEM of Strained GE MOSFET structure

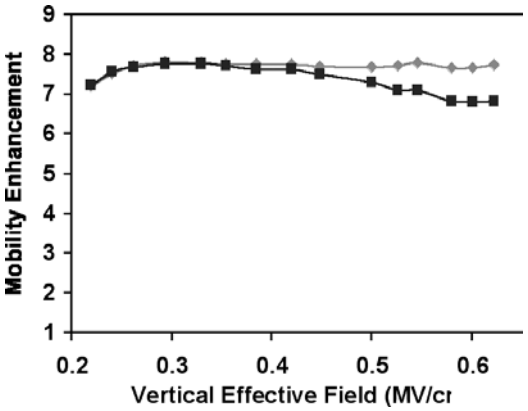

Fig. 16: Hole mobility enhancements in strained GE pMOS