Development of Processes and Technologies for Interconnects for 3D Integrated Circuits

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The exponentially increasing numbers of devices fabricated in a single silicon chip requires an even faster increase in the number of wires that interconnect theses devices. The total length of interconnecting wires (interconnects) in a single high-performance integrated circuit is already several kilometers. Latency associated with resistance-capacitance losses in interconnects now limits the speed of integrated circuits. One approach to limiting the effects of interconnects on circuit performance, is to stack device layers (or chips), so that many wires connect across the gap between the device layers. These 3D integrated circuits will have significantly reduced total interconnects lengths, and therefore significantly reduced signal delays, compared with 2D circuits with the same functionality.

One approach to the fabrication of 3D integrated circuits is to bond previously-processed device layers using metal-metal bonds that also serve as layer-to-layer interconnects. We are developing technologies for making and characterizing bonded interconnects for 3D IC's.

We have demonstrated the use of a 4-point bend test (Figure 4) to evaluate the strength of Cu-Cu bonds. We have investigated pressure bonds made by bonding wafers coated with Cu films or lines deposited on Ta layers on oxidized silicon wafers. From load-displacement measurements (Figure 5), the load for steady state crack propagation is determined. From this measurement, the critical strain energy release rate, which serves as a measure of the interface fracture toughness, can be obtained. We have found that bonds between 300nm-thick Cu films can have strengths of approximately 10 J/m^2, when created at 400C and at pressures of about 0.4MPa. We have also found that higher bond strengths with lower variabilities can be obtained when bonds are made in reducing gas (5%H_2 and 95%Ar) instead of pure N_2. The bond strength decreases with decreasing bonding temperature, but is still about 3 J/m^2 for bonds made at 300C. The bond strength is higher for thicker bonded films.

Having developed a quantitative technique for the evaluation of bond strengths, and having used this method to develop optimized bonding processes, we are now developing electrical/mechanical test structures and techniques that will allow investigation of bond strength variations over arrays of bonded interconnects, and will also allow bond reliability studies. These test structures will be made possible through the creation of metal-filled through-wafer vias. Through-wafer vias will be made using deep reactive etching, and they will be filled using electrodeposition.

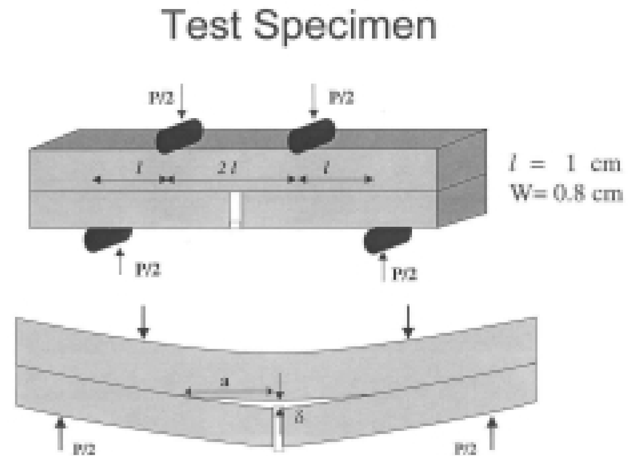

Fig. 4: Four-point bend test specimen.

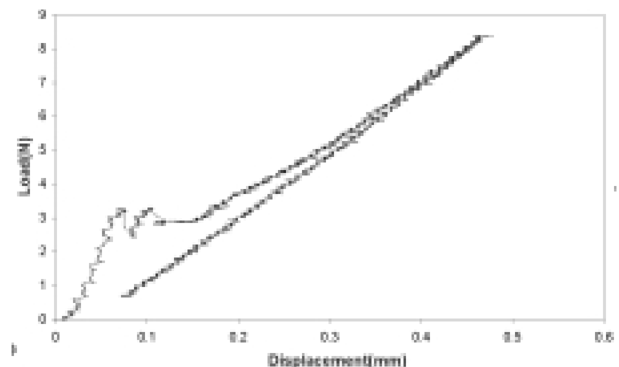

Fig. 5: Load-displacement behavior from a four-point test.