Experimental Characterization of Electromigration-Induced Failure of Cu-Based IC Interconnects

Personnel

F. Wei, C.L. Gan, Z. Choi, K.L. Pey, W.K. Choi, S.P. Hau-Riege, J.J. Clement, and C.V. Thompson

Sponsorship

SRC and SMA

Delay associated with over a kilometer of metallic interconnections in a single high-performance integrated circuit now limits the overall circuit speed. The delay associated with interconnects is due to parasitic capacitances that can be reduced by reducing the resistivity of the metal (until recently, Al) and by decreasing the dielectric constant of the material between interconnects (currently SiO_2). This has driven the development of new Cu-based IC interconnection technologies. The major limitation on the reliability of interconnects is associated with electromigration-induced failure. Electromigration is current-induced diffusion, and it results in interconnect failure when it causes the formation of voids or extrusions. Cu is expected to have intrinsically lower rates of electromigration. However, aspects of the technology changes associated with the introduction of Cu lead to new reliability issues.

In the last year, electromigration tests were performed on dual-damascene Cu interconnect structures that were fabricated at International Sematech Inc. in the U.S., and at the Institute of Microelectronics in Singapore. The dual-damascene Cu test structures include both via-to-via (straight-line) structures as well as multi-segmented tree structures with more than two vias.

Two types of via-to-via test structures were tested; structures in which the test segment was in the second layer of metallization (M2), and structures in which the test segment was in the first layer of metallization (M1). In each case, the connecting lines were in the other metallization layer and were at least 5 times wider than the test lines, so that current densities (and therefore failure rates) were higher in the test segments than in the connecting lines. We found that the lifetimes of otherwise identical M1 and M2 test structures, tested under identical conditions, were very different. Failure analyses suggest that this asymmetry occurs because of preferential formation and growth of voids at the Cu/Si_3N_4 interface at the top of the Cu lines. Larger voids are required for failure of M2 structures (Figure 2b) than for failure of M1 structures (Figure 2a). We have also found that the line-length dependence of the reliability of Cu interconnects is more complex than that of Al interconnects. Short Al interconnects tested at low current densities do not fail because current can shunt around voids through conducting over- and under-layers. However, because Cu has a non-conducting overlayer, even small voids can lead to failure (Figure 2a). This means that short Cu lines can be less reliable than equivalent Al lines. On the other hand, we also find that some long Cu lines have very long lifetimes when they are connected to sources and sinks for Cu. This is thought to be due to rupture of the thin refractory-metal liner at the base of the Cu vias (Figure 2c). Liner rupture allows free flow of Cu though the test structure. Whether this would lead to improved *circuit-level* reliability is not clear. In any event, for Cu, unlike Al, long test structures can have increased apparent reliabilities compared to shorter structures.

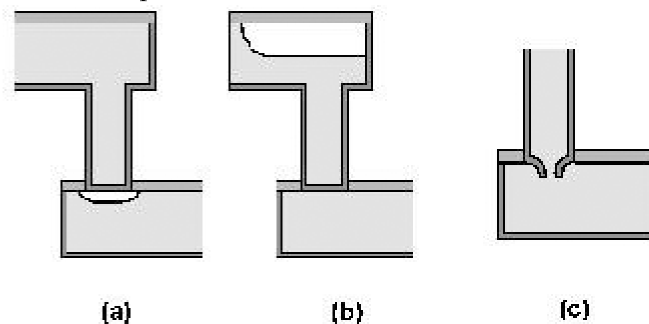

Fig. 2: Different response to tensile stresses at metal-to-metal vias in dual-damascene Cu technology.

We have also begun to test multi-terminal test structures. The simplest of these is a line with vias at both ends and in the middle (we have nicknamed these structures "dotted-i"s, Figure 3). The middle via divides the test line into two segments that can be subjected to different currents. Figure 3 shows some of the results obtained from these experiments. These results

segment cannot be assessed without knowledge or assumptions about the stress conditions of neighboring segments (though this is often what is done in circuit-level reliability assessments). These results therefore demonstrate that for Cu, as for Al, segments are not the appropriate fundamental reliability unit on which to base circuit-level reliability assessments. However, because vias in current Cu technology are not fully blocking, interconnect trees are also not appropriate fundamental reliability units (though they are for Al). These results therefore show that new methods are required for circuit-level reliability assessments for Cu interconnects.

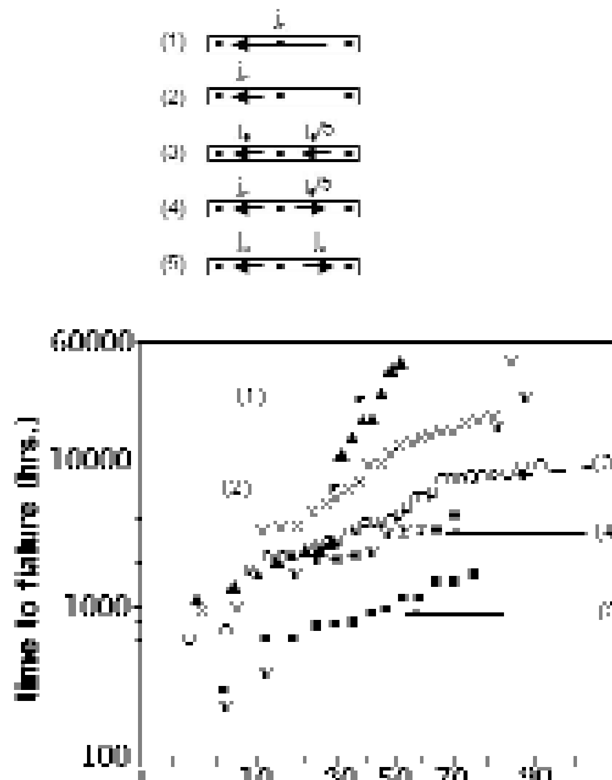

Fig. 3: Failure times (bottom) for 3-terminal Cu interconnects tested under different current configurations (top).