Characterizing Process Variation Using A Ring Oscillator Based Test Chip

Personnel
K. Gonzalez-Valentin and J. Panganiban (D. Boning)

Sponsorship
SEMATECH and IBM

Process variation is an increasingly difficult challenge in the design of high-yielding integrated circuits, and techniques are needed to measure and extract variation in a given process and link it to circuit performance. A test chip implemented in the MOSIS 0.25 µm TSMC process has been designed and fabricated, containing test structures aimed at extracting gate-length, interconnect geometry, threshold voltage, and other process variations. The core test structure is a Ring Oscillator (RO) composed of an odd number of cascaded inverters; since the RO frequency is dependent on device parameters and the load between stages, distributions of measured RO frequencies can be used to characterize variation in the devices and interconnect loads.

The 2.5 mm by 4.0 mm test chip is composed of forty-five unique ring oscillator types, which are replicated throughout the chip to incorporate over two-thousand RO test structures. Approximately half of the test structures are used to extract Front-End-Of-Line (FEOL) variation, such as gate-length and threshold voltage, while the other half concentrates on interconnect and Back-End-Of-Line (BEOL) process variation. A scan chain architecture, as shown in Figure 3, is used to enable frequency measurement of each structure. The basic building block is a "tile" which includes a single ring oscillator test structure as well as control circuitry responsible for enabling the RO and outputting the RO signal onto a horizontal bus which feeds into frequency division circuitry. These tiles are cascaded side by side to compose a row, and these rows can then be replicated vertically to make up the entire chip. In addition to increased RO density, this architecture allows for relatively efficient data collection on the board level without the need to probe the die for individual RO measurements; instead, frequency measurements of all two-thousand ROs can be accomplished with simple digital control (e.g. using LABVIEW).

Preliminary testing of recently fabricated chips confirms the functionality of the control architecture. Frequency measurements are made on all chips, and variation analysis on the data is currently being conducted. Table 1 summarizes a subset of ring oscillator designs for study of layout impact on FEOL variation. The table shows the oscillating frequency and standard deviation of different ROs with the same total gate length. The first three structures indicate that the standard deviation increases with the number of fingers in the RO, demonstrating a channel length variation increase with the number of fingers. Other layout effects on variation are also seen, such as the impact of vertical vs. horizontal transistor layout. Future work includes the extraction of both device and interconnect variation sources, and relating these to circuit impact such as timing sensitivities.

Description	Frequency [MHz]	σ [KHz]	σ% [%]	Variation
Single Finger RO	4.25	52.34	1.23	*Minimized ΔL Variation*
Three Finger RO (Canonical)	4.42	130.47	2.95	*Accentuated ΔL Variation*
Two Finger RO	4.21	75.98	1.8	*Studies Density vs. Isolated effect*
Three Finger RO with 1.2x Spacing Between Polysilicon Fingers	4.3	132.18	3.07	*Studies proximity effect*
Three Finger RO with 1.5x Spacing Between Polysilicon Fingers	4.2	126.87	3.02	
Three Finger RO with 2x Spacing Between Polysilicon Fingers	4.13	128.57	3.11	
Three Finger RO with 3x Spacing Between Polysilicon Fingers	4.12	134.98	3.28	
Three Finger RO Vertically Laid Out	4.36	144.33	3.31	*Studies Orientation Effect*

Table 1: Comparison of differently laid out ring oscillators with the same gate length

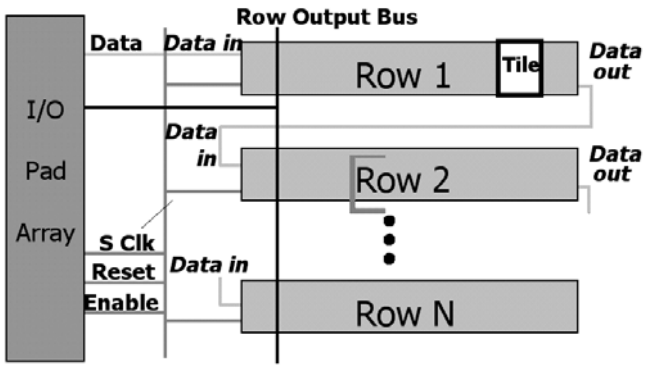

Fig. 3: Variation test chip architecture.