A Programmable, Wide Dynamic Range CMOS Imager with On-Chip Automatic Exposure Control

Personnel

P. M. Acosta Serafini (C. G. Sodini)

Sponsorship

Intelligent Transportation System Center and
National Semiconductor Fellowship

Machine vision applications that use visual information typically need an image sensor able to capture natural scenes that may have a dynamic range as high as four orders of magnitude. Reported wide dynamic range imagers may suffer from some or all of these problems: large silicon area, high cost, low spatial resolution, small intensity dynamic range, poor pixel sensitivity, small intensity resolution, etc. The primary focus of the proposed research is to develop a single-chip imager for machine vision applications which addresses these problems, but is still able to provide an ultra wide intensity dynamic range by implementing a novel pixel-by-pixel automatic exposure control. The secondary focus of the research is to make the imager programmable, so that its performance (light intensity dynamic range, spatial resolution, light intensity resolution, frame rate, etc.) can be tailored to suit a particular machine vision application.

The image sensing array has pixels which can be independently read and reset. The proposed brightness adaptive algorithm then predictively scales the voltage in photodiodes that would saturate under normal circumstances based on information gathered in several readout checks. The total integration time is subdivided into several integration times (called integration slots), which are progressively shorter. During any of the checks if it is determined that the pixel will saturate at the end of the integration slot, then the pixel is reset and it is allowed to once more integrate light, but for a shorter period of time. Each pixel has a small associated memory location to store an exponent that identifies the actual integration slot used. This information is used to appropriately scale the digitized pixel output.

The prototype ASIC includes a 1/3" VGA (640x480) array (7.5mm square pixels), 64 cyclic analog-to-digital converters for digital pixel output, an integration controller which implements the described algorithm, 4-bit per pixel SRAM memory for exponent storage, and supporting digital logic.