Low Power Reconfigurable Analog-to-Digital Converter

Personnel
K. Gulati (H.-S. Lee)

Sponsorship
Center for Integrated Circuits & Systems(CICS)

There are applications which require Analog to Digital Converters (ADC) that can digitize signals at a wide range of bandwidth at varying resolution with adaptive power consumption. Clearly, a conventional ADC with fixed topology and parameters cannot accomplish this task efficiently. An alternate approach is to employ an array of ADCs, each customized to work at narrow ranges of resolution and input bandwidth – such a system would occupy a prohibitively large area to achieve optimal power consumption at fine granularity over bandwidth and resolution. A single ADC with reconfigurable parameters and reconfigurable topology would be able to achieve the above goal. Prior reconfigurable ADCs, however, achieve very limited reconfigurability. The proposed ADC is designed to provide a significantly larger reconfigurability space. Its target resolution ranges from 6 to 16 bits and signal bandwidth from 0 to10MHz.

The concept of this ADC stems from the observation that certain ADC architectures such as the pipeline, cyclic and sigma-delta ADC topologies are composed of the same basic components such as opamps, comparators, switches and capacitors. The sole difference between them, from a network perspective, is the interconnection between these devices. Thus, a converter composed of these basic building blocks in conjunction with a configurable switch matrix, can be made to construct these different topologies and work at different resolutions and bandwidths.

The reconfigurable ADC consists of several basic building blocks as shown in Figure 35. A user defined 'resolution word' that determines the resolution of the ADC is supplied to the main reconfiguration logic that then determines the global structure of the ADC and the state of each block. The PLL shown in the figure uses the frequency information in the clock and the resolution information from the main reconfiguration logic to determine the appropriate bias current of the opamps.

The ADC was fabricated in a TSMC 0.6µm DPTM CMOS process and occupies a total die area of 10.5x7.6mm^2 (Figure 36). The reconfigurable ADC intrinsically requires an area only slightly larger than a 12-bit ADC, however, the prototype layout is optimized not for area but for testability. The resolution of the ADC can be varied from 6 - 15 bits while bias current can be varied over a range of about 3 orders of magnitude corresponding to a sampling rate range of 20KHz-20MHz. Table 2 provides a summary of representative measured results.

Process	0.6µm CMOS, DPTM
Die Area	10.5mm x 7.6mm
Power Supply	2.7V-4.6V
Parameter Reconfiguring Time	12 clock cycles
Sigma-Delta 15 bit Mode (3.3V)	
Resolution	15 bits
Fclock	10MHz
Fin	3.13KHz (1.5V p-p differential)
OSR	1024
Power	8.8mW
HD2	111.8dB
HD3	96.21dB
Pipeline 12 bit Mode (3.3V)	
Resolution	11 bits
Fclock	2.62MHz
Fin	1MHz (1V p-p differential)
Power	24.6mW
DNL	< +/- 0.55LSB
INL	< +/- 0.82LSB

Table 2: Measured results at two performance points.

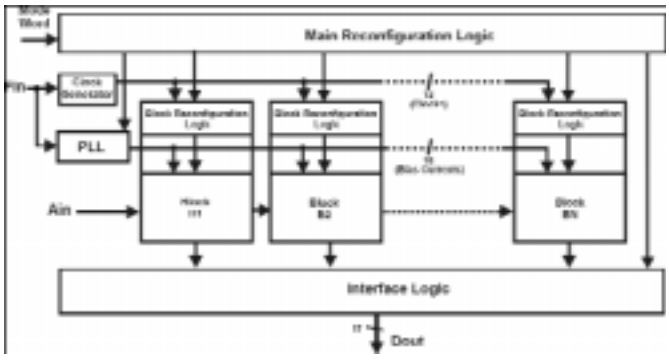

Fig. 35: ADC architectureFig.

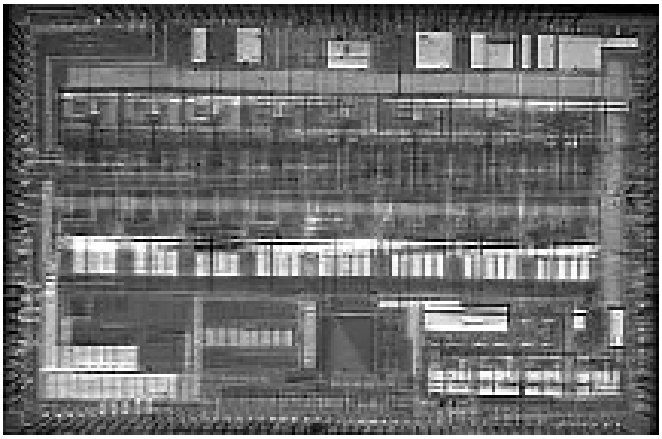

Fig. 36: ADC micro-photograph.