## **Radio Frequency Digital-to-Analog Converter**

**Personnel** S. Dacy (H.-S. Lee)

## Sponsorship

Lucent Fellowship, ABB, and Center for Integrated Circuits & Systems

Dynamic performance of high speed, high resolution, DACs is limited by distortion at the data switching instants. Inter-Symbol Interference (ISI), imperfect timing synchronization and clock jitter are all culprits. A DAC output current controlled by an oscillating waveform is proposed to mitigate the effects of the switching distortion. The oscillating waveform should be a multiple ( $k^*fs$ ) of the sampling frequency (fs), where k>1. The waveforms can be aligned so that the data switching occurs at the zero crossings of the oscillating current output. This makes the DAC insensitive to switch dynamics and jitter. The architecture has the additional benefit of mixing the DAC impulse response energy to a higher frequency. Instead of the conventional sinx/xDAC impulse response roll-off, there is a large high frequency lobe near the control oscillating waveform frequency (k\*fs). An image of a low Intermediate Frequency (IF) input signal can therefore be output directly at a high IF or Radio Frequency (RF) for transmit communications applications.

A narrowband sigma-delta DAC with eight unit elements was chosen to implement the RF DAC. A sigmadelta architecture allows the current source transistors to be smaller since mismatch shaping is employed. Smaller current source transistors have a lower drain capacitance, allowing large high frequency output impedance to be achieved without an extra cascode transistor. Elimination of the cascode reduces transistor headroom requirements and allows the DAC to be built with a 1.8V supply.

The RF DAC is currently being designed in 0.18µm, 1.8V CMOS technology. Target specifications are a 17.5MHz conversion bandwidth centered around 942.5MHz with 60dB SNR and 80dB SFDR.