Superconducting Bandpass Delta-Sigma A/D Converter

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The direct digitization of RF signals in the GHz range is a challenging application for any circuit technology. Traditionally, flash A/D converters have been used to digitize signal frequencies above 1 GHz, but their resolution and linearity are inadequate for most radio systems, which must handle signals with a large dynamic range. Semiconductor bandpass delta-sigma modulators are used to digitize IF signals with high resolution, but their performance at microwave frequencies is limited by the speed of semiconductor comparators and the low Q of integrated inductors.

In this program, we present the design and testing of a superconducting bandpass delta-sigma modulator for direct A/D conversion of GHz RF signals. The schematic of the circuit is shown in Figure 32. The input signal is capacitively coupled to one end of a superconducting microstrip transmission line, which serves as a high quality resonator (loaded Q > 5000). The current flowing out of the other end of the microstrip line is quantized by a clocked comparator comprising two Josephson junctions. If the current is above threshold, the lower junction switches and produces a quantized voltage pulse known as a Single Flux Quantum (SFQ) pulse. If the current is below threshold, the upper junction switches instead. The pattern of voltage pulses generated across the lower Josephson junction represents the digital output code of the delta-sigma modulator. These voltage pulses also inject current back into the microstrip line, providing the necessary "feedback" signal to the resonator. At the quarter-wave resonance of the microstrip line (about 2 GHz in our design), the resonator shunts the lower junction with a very low impedance, the "feedback" current to the resonator is maximized, and the quantization noise is minimized. Because of the high speed of Josephson junctions and the simplicity of the modulator circuit, the maximum sampling rate exceeds 40 GHz.

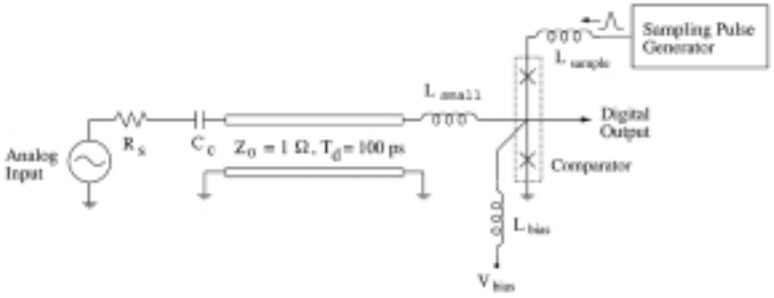

Fig. 32:

While such a high sampling rate improves the performance of the delta-sigma modulator, the challenges of high speed testing in a cryogenic environment are formidable. Even in the best cryogenic sample holders, the long cables used to connect the superconducting chip to room-temperature electronics have significant losses at frequencies above 10 GHz. Experimentally, we found two solutions for clocking the circuit at high frequencies. In the first approach (detailed in previous reports), we employ an optoelectronic clocking technique, in which picosecond optical pulses at a 20.6 GHz repetition rate are delivered (via optical fiber) to an on-chip photodetector, the current pulses from which drive a Josephson clock amplifier. In the second approach, the modulator is triggered by an on-chip clock source. An increase in bias current turns the Josephson clock amplifier into an oscillator tunable between 20 and 45 GHz. We found that surprisingly good frequency stability could be achieved with the on-chip clock source with careful adjustment of dc bias currents.

Since the modulator output data rate exceeds the capacity of the interface to room-temperature test equipment, on-chip processing of the data is used to reduce the bandwidth requirements for readout. As explained in the 1998 MTL report, two segments of the modulator's bit stream are captured with a pair of 128-bit shift registers. The number of clock cycles skipped between acquiring the two segments is set by an on-chip pro-

grammable counter (from 0 to over 8000). Cross-correlation of the two captured segments is used to provide estimates of the autocorrelation function R[n] of the modulator output, from n=0 up to a large value, such as n=8000. Fourier transformation of R[n] then yields a power spectrum with frequency resolution comparable to an 8K FFT of the original bit stream.

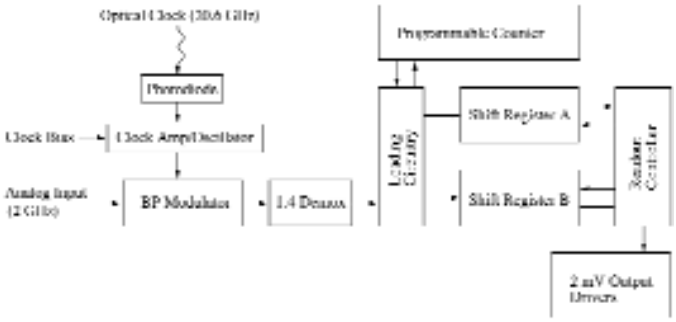

Fig. 33:

Figure 33 shows the block diagram of the modulator test chip. As mentioned above, the bandpass modulator can be clocked either externally by a 20.6 GHz optical source or internally by an on-chip Josephson oscillator. A 1:4 demultiplexer converts the single-bit output of the modulator to 4-bit words at one-fourth the sampling rate. This allows most of the test chip, including the programmable counter and the shift register memory banks, to operate at a reduced clock rate with larger timing margins. Because of the 1:4 demultiplexing, 128-bit memory banks A and B are organized as 4 parallel rows of 32-bit long shift registers. As just discussed, the number of clock cycles skipped between loading the A and B memory banks is set by a programmable counter, which is programmed by external control currents. Once the shift registers have been loaded, a readout controller unloads the stored bits and transfers them to "high-voltage" drivers, which amplify the output signals up to about 2 mV, which is large enough to be detected by room-temperature electronics. The test chip employs over 4000 Josephson junctions and represents one of the most complex circuits ever designed in this technology.

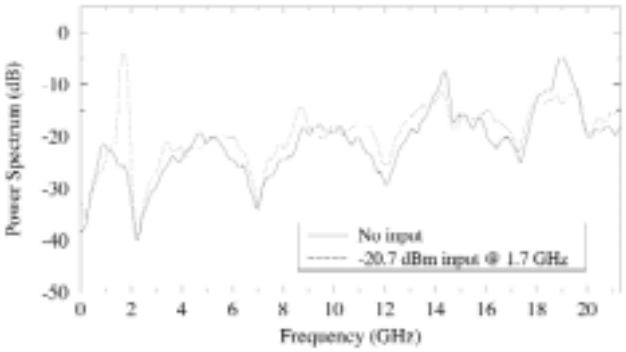

Fig. 34:

The test chip was fabricated at HYPRES, Inc. While the chip has been used with the 20.6 GHz optical clock, higher oversampling ratios and SNRs are attained with the on-chip clock source operating near 40 GHz. In the initial experiments, the programmable counter on the test chip was programmed so that the shift registers captured 256 consecutive bits from the modulator, so that 256-point FFTs could be calculated. The output spectra of the modulator at a sampling rate of 42.6 GHz are plotted in Figure 34. The width (about 500 MHz) of the input tone at 1.7 GHz reflects the low frequency resolution of the 256-point FFTs. The full-scale (FS) input sensitivity is -17.4 dBm (30 mV rms). Quantization noise is suppressed at 2.23 GHz and at higher frequencies corresponding to higher-order microstrip modes. The SNR (49 dB over a 20.8 MHz bandwidth) is limited by the frequency resolution of the measurements but still exceeds the SNRs of semiconductor modulators with comparable center frequencies. Other measurements, based on the correlation technique discussed above, show that the in-band noise over a 19.6 MHz bandwidth is -57 dBFS. The center frequency and sampling rate of the experimental modulator are the highest reported to date for a bandpass delta-sigma modulator in any technology.