Circuit Design and Technological Limitations of Silicon RFICs

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Wireless products and communications systems have thrived on the increased utility enabled by semiconductor technologies, the demand for which is necessitating ever higher communication channel frequencies to obtain wider bandwidth and to alleviate interference. This places still greater demands on the technologies used to implement the wireless systems; however, for a given application, the market determines the acceptable end product price based on convenience, functionality, and a comparison with substitutes, effectively setting a bound on the technologies that can be used. The limitations of these technologies in part determine the achievable performance, which then in turn may confine the very convenience and functionality being sought through the wireless system.

In this interplay of circuits and systems with technology where both price and performance are crucial, we are exploring two aspects that can yield significant improvements in the design of wireless systems. The first of these is the optimization of a broad range of RF circuits at the device level. By working through the exercise of designing the components needed to realize a 5.8GHz receiver, generalities are being sought which link technological parameters with system level performance. Using the receiver application to frame circuit constraints, device level issues are being studied to determine the physical origins of circuit limitations. Design techniques are then being investigated to mitigate these limitations to the extent possible, a procedure that aims to both optimize the circuits and underscore the degree to which the limitations are fundamental.

Next, the knowledge of those factors that are limiting circuit performance are then used to devise methods of implementing circuits in which the performance—measured in terms of system level parameters—can be dynamically tuned to match real-time conditions in a power efficient manner. This facility provides the mechanism by which energy can be conserved in RF circuits by sensing and using information about the environment, communications channel, and data to be transmitted. Incorporation of adaptability at the circuit and system levels is paramount in expanding capabilities and increasing utilization of wireless communication links, and yet remains a largely untapped resource in this field.

This project entails the application of these concepts to the development of the component-level circuits required in an integrated RF front end for a 1GBit/s wireless network operating at 5.8GHz. The typical components in a receiver—Low Noise Amplifiers (LNAs), Voltage-Controlled Oscillators (VCOs), and mixers—are considered in this work. A set of VCOs and LNAs have been designed into a 0.5μm SiGe BiCMOS technology as data points to illustrate device and circuit optimization trade-offs. Direct comparisons of CMOS versus bipolar, the impact of transistor f_T/f_{MAX}, and the implications of design methodologies based upon linear time variant models are some of the issues being explored. The approach that has been developed along with information gleaned from the experimental circuits can provide a basis for shaping future integrated circuits, technologies, and system designs for wireless applications.