RF Analog Circuit Design with Scaled CMOS Devices

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Because of the prospect of low cost and high integration of scaled CMOS, much effort is being focused on its use for Radio-Frequency (RF) communication circuits. Low Noise Amplifiers (LNA) are essential building blocks for the design of communication systems, and some applications would benefit from the use of low cost CMOS transistor technology to build the LNA. MOS transistors are typically considered to be the noisiest transistor technology, but with the scaling of channel length, MOS transistors have f_Ts in the tens of gigaHertz (where f_T is the transistor unity current gain frequency). High f_T results in gain out to higher frequencies, and a lower noise figure at those frequencies. While the noise theory of long channel devices is well understood, and a handful of theories exist for short channel devices, complete noise characterization of short channel devices is in short supply. Our approach is to thoroughly understand the long channel noise theory, examine possible short channel theories, gather measured data on a set of scaled CMOS transistors, and interpret the results. Equipped with this new information, existing LNA designs will be evaluated for use with scaled MOSFETs and design improvements examined.

The classic long channel noise theory for intrinsic FET transistors proposed by van der Ziel (Proc. of IRE, 1962) defines two noise sources that are present at the device terminals. The first is the drain current noise (i_d), which originates from the conductance of the channel, and the second is the induced gate current noise (i_g), which originates from the charge fluctuations in the channel when the drain current fluctuates. This description implies that the two would be completely correlated, but this is not the case. To be sure, they are dependent on each other, but due to the active nature of the channel, the two are only partially correlated ($|c| = 0.395$). Together, these sources give a complete description of the device noise suitable for a two-port Y-Parameter model.

In short channel transistors, the physics of the drain current is different from the long channel case, and the expressions for i_g, i_d and c are different from those van der Ziel derived. Based on the model from Pucel et. al. (Adv. in Electronics and Elec. Physics, 1975) for MESFETs, as the channel approaches complete velocity saturation, the correlation between the drain current noise and the gate current noise should approach unity. Pucel et. al. also considered the more general situation by dividing the channel into two regions, one where the gradual channel approximation holds and the other velocity saturated. Therefore, the results obtained under the assumption of complete velocity saturation represent a limiting case, and the actual performance should be between this solution and the long channel theory.

Device measurements are required to verify any changes in the amount of drain current noise, gate current noise, and their correlation. Fortunately, the procedure to setup a high frequency, noise figure based measurement system is fairly well documented in the literature (Pucel et. al, MTT 1992), and commercial systems are available. In order to measure the high frequency performance of the transistors on chip, special coplanar waveguide probes and probing structures must be used. Care must be taken to remove the effects of the measurement equipment and the on-wafer probing structures. The results of these efforts are a complete two-port noise description of the device. These results can then be fit to the i_g, i_d, and c model from above.

Applying the results obtained from the measured data to LNA design is the final objective of this work. Depending on the significance of the correlation between the induced gate current noise and the drain current noise, the magnitudes of gate and drain noise currents, and the small-signal performance, variations or changes in the approach of LNA design in scaled CMOS technology will be investigated.