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Substrate Noise Charaterization Shaping in Mixed-Signal Systems

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The basic demands of power, speed, and cost drive the ever tighter integration of all circuits in a system onto a single chip, or the so-called System on a Chip (SoC). This necessitates the integration of analog circuits with digital circuits. However, in this integration, the acute problem of substrate noise coupling arises. The noisy digital circuits inject noise into the common substrate, which can severely affect sensitive analog circuits. Improperly accounted for, this noise can degrade performance drastically, and in some cases destroy functionality.

Up to now, most efforts in addressing this problem have been to ensure that analog circuits are robust enough to withstand the digital noise. These techniques include physical separation, differential architectures, and simulation. Hardly any effort has been placed on reducing the substrate noise itself.

With this in mind, the focus of this research is to investigate the characteristics of the substrate noise as well as ways to cancel the injected substrate noise. We have implemented a test chip that includes a digital circuit as substrate noise generator and a delta-sigma A/D converter that samples the substrate noise. The digital circuit is operated in such way that it injects periodic noise waveform on the substrate. The delta-sigma converter is used as an accurate on-chip sampling scope to map the substrate noise as a function of time. The sampling edge of the delta-sigma A/D converter is moved relative to the digital clock edge. Figure 29 shows an example of measured substrate noise using this technique.

In order to reduce the effect of the substrate noise, we propose to cancel and shape the noise in bands of interest with a feedback loop. This type of noise shaping is well suited for oversampling and bandpass type applications.

The substrate noice shaping loop is based on a delta-sigma modulator loop with the substrate noise treated as quantization noise. The feedback D/A is replaced by an array of noise-injecting inverters. This has the advantage of simplicity and low power.

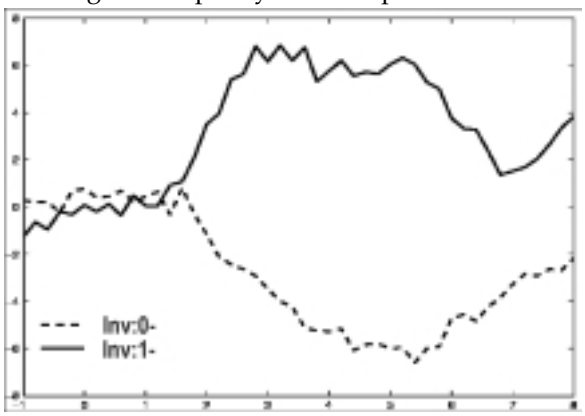

Fig. 29: Measured substrate noise with an on-chip sampling scope.

Furthermore, the addition of an independent substrate noise shaping loop to the system will require little effort and little loss of performance. The analog and digital circuits can be designed as if there was no substrate noise shaping loop.

As proof of concept, a prototype chip has been designed that integrates the substrate noise loop with a 16-bit delta-sigma A/D converter and a complex digital encryption engine onto the same substrate. The chip runs at 2.5V and has been fabricated in 0.25µm CMOS technology.

The chip is currently being tested and characterized. Preliminary measurements show noise cancellation in desired bands of interest. Figure 30 and 31 show the substrate noise spectra before and after noise shaping. The substrate noise shaping reduces the overall substrate noise by 15 dB in 0-45kHz frequency band.

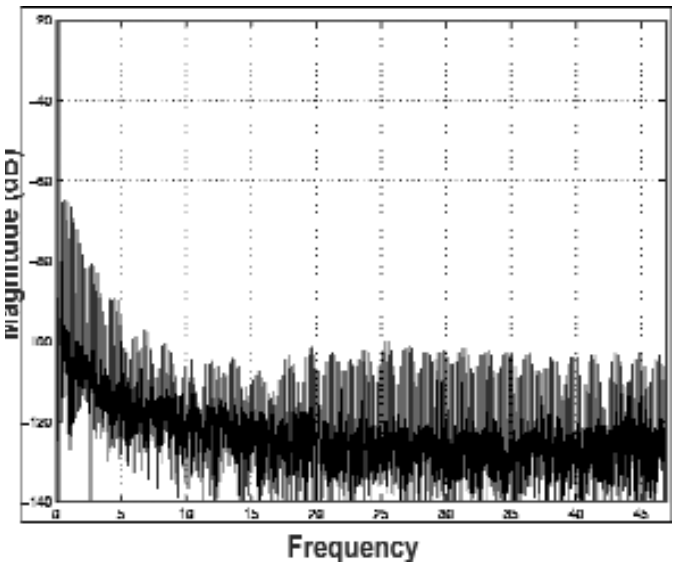

Fig. 30: Substrate Spec. w/out SN Shaping

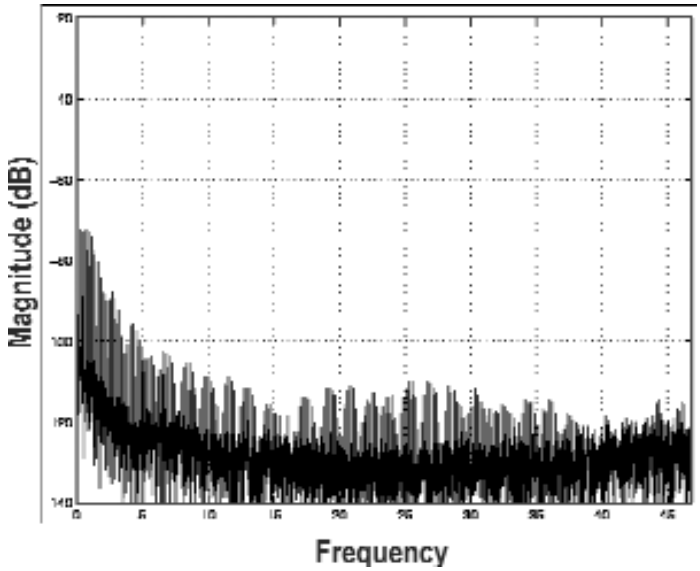

Fig. 31: Substrate Spec. w/ SN Shaping