Mixed-Signal Design in Deeply Scaled CMOS Technology

Personnel

J. Fiorenza (H.-S. Lee and C. G. Sodini)

Sponsorship

Center for Integrated Circuits & Systems and MARCO

There are tremendous challenges in implementing mixed-signal systems on a single substrate in deeply scaled CMOS technologies primarily due to the negative impact of the technology on analog circuits. Nearly every aspect of scaling except speed goes against analog circuits. Lower power supply voltage severely restricts the signal range, requiring substantially lower circuit noise in order to keep the signal-to-noise ratio. Small geometry transistors exhibit far less voltage gain and greater threshold voltage mismatches than their predecessors. Attempts to overcome device gain limitations with conventional techniques such as cascode and regulated cascode aggravates already slim signal swing. The use of long-channel devices for higher gain inevitably compromises the circuit speed.

In order to overcome the challenges, we are exploring innovative circuit techniques that avoid shortcomings of deeply scaled technologies, and actually exploit them in mixed signal systems. As the first step we have been investigating circuit techniques that overcome the device gain limitations without penalizing the signal swing or circuit speed. An innovative approach that we have developed employs two signal paths: the main path and the prediction path. The prediction path processes the signal ½ clock phase earlier than the main path at a reduced accuracy. The information obtained from the prediction phase is used to in the main path in order to compensate for the finite device gain, incomplete settling and other non-idealities. The two-path approach can be applied to many different classes of analog circuits including data converters, filters, instrumentation amplifiers, and many others. As the initial proof-of-concept, we designed a MOS sample-and-hold amplifier in a standard 0.18 μm digital CMOS process. The simulation predicts the accuracy corresponding to 100dB amplifier gain with no cascading. The chip design will be submitted for fabrication in April.