Characterization Methodology of CMOS Processes for Image Sensor Applications

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Sponsorship

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CMOS image sensors have lower power consumption and better circuit integration ability compared to CCD image sensors. However, standard CMOS processes are optimized for circuit applications rather than image sensing. Modifications from standard CMOS processes are often required for better image sensor performance. In order to select the most efficient photodiode structure and diagnose the effects of the modified process parameters, a two-stage characterization methodology is developed.

In the first stage, large photodiodes (~500 mm X 500 mm) with different junction structures, such as NW/Psub and N+/PW photodiodes, are implemented. This allows one to directly measure the fundamental junction properties of the diodes for image sensing. Two major parameters, quantum efficiency and leakage current are measured and compared. The large area of the diodes assures the measurement accuracy. Furthermore, the layouts of the diodes can be a bulk, strip or grid shape to study the area, edge, and corner components of the junction properties. In this first stage, the best junction type NW/Psub is identified for further investigation at the pixel level.

In the second stage, a small test pixel array (e.g. a 64 x 64 array) is implemented to study the pixel performance. Since this array is a miniature version of an imager, it contains all the characteristics of a large format imager. Its small size allows one to arrange several arrays with different designs on the same chip to remove wafer-to-wafer variation of the chips. Typical imager characteristics that can be measured with the test arrays include sensitivity, dark current, fixed pattern noise, random noise, and dynamic range. Process parameters, such as thermal treatment and sensor implant conditions, can also be fine-tuned with the test array.

This two-stage approach provides a methodology to select the best junction structure and process parameters for a CMOS image sensor process. This approach has been implemented in a 0.25μm CMOS process.