A Differential CMOS Passive Pixel Imager

Personnel
I. L. Fujimori (C. G. Sodini)

Sponsorship
Lucent GRPW Fellow and Intelligent Transportation Research Center

Passive pixel sensors provide an alternative to the conventional Active Pixel Sensor (APS) for high-density CMOS imaging arrays. Similar to the history of the single-transistor DRAM cell, this one-transistor pixel cell boasts one main advantage over the APS. It can achieve a high fill-factor in a smaller area, leading to a high-density array of pixels with high quantum efficiency. Experiments reveal a major weakness in passive pixels is a signal-dependent parasitic current that can contaminate charge signals in different parts of the array. In this project, we explain the origin of this parasitic current and demonstrate a Correlated Double Sampling (CDS) circuit in a differential architecture that removes its effects.

The passive pixel consists of a high-efficiency n-well photodiode and one transistor for reset and row select. The charge difference between the output of a sensing pixel and a dummy cell kept in the dark is converted to a voltage with a sense amplifier at the bottom of every column. The differential architecture is advantageous in rejecting any common-mode signals such as ground bounce.

Passive pixels are plagued with a signal-dependent parasitic current caused by photogenerated electrons collected by the reverse-biased junction of the column line at each pixel. The combined effect of the charge leakage from 256 cells on the column line can be significant and will appear as a parasitic current at each column line. This parasitic current, which is also present in active pixel arrays, is catastrophic in passive pixels because charge-to-voltage conversion does not occur within the pixel. The parasitic charge of a bright pixel can thus contaminate the output of a dark pixel in other rows in the column line and cause smear in the image.

Two strategies were used to remove the effects of the parasitic current. The first was at the architectural level where a differential readout between a sensing and a dummy column rejects the parasitic current that is common between the two columns. The second part consisted of removing the difference in parasitic currents between adjacent columns. The latter was achieved with a CDS circuit that senses the signal with the parasitic current during the first sample phase and then senses the parasitic current only during the second sample phase. The difference between the output of these two sample phases then purely corresponds to the pixel signal and is no longer dependent on the parasitic current.

The improvements achieved with the differential CDS circuit were quantified in terms of column-to-column Fixed-Pattern Noise (FPN). As expected, the dark FPN values are similar at 0.4% with and without CDS. The difference becomes more pronounced as the light intensity increases and the parasitic current mismatches result in a much higher FPN in the absence of the differential CDS circuit.

While this improved passive pixel imager addresses many of the problems that have plagued passive pixels in the past, it does not easily scale with increasing array sizes. The main limiting factor is the readout noise, which is proportional to the column line capacitance and inversely proportional to the pixel capacitance. The combined effect of these factors severely limits the intensity resolution that can be achieved for high-density arrays. The latest research efforts indicate that the noise may be suppressed by introducing a high load capacitance on the column amplifier. While requiring higher currents to achieve the original bandwidth, this method may allow passive pixels to remain in the imaging race for high-density arrays.