A CMOS-Compatible Compact Display

Personnel
A. Chen (A.I. Akinwande and H.S. Lee)

Sponsorship
3M and MARCO

The proliferation of portable electronic systems has created demand for high-resolution displays which are compact and highly energy-efficient. We have designed and built a proof-of-concept for a display that meets these design constraints. Our display uses a standard digital CMOS integrated circuit to produce a low-brightness image, and an image intensifier to increase brightness to a visible level. Since a only very low light level needs to be generated from the CMOS chip the power efficiency is primarily determined by the intensifier which typically exhibit high efficiency. Moreover, exploiting high level of integration achieved by the CMOS IC, low power techniques such as pixel memory and data compression can be implemented further lowring the system power consumption. A display using our design should produce a daylight-visible image using approximately half a watt of power.

Silicon devices can convert electrical energy into light, although their efficiency is very low. We use silicon light-emitting diodes to produce a very faint image which is optically coupled into an image intensifier. The image intensifier is a compact vacuum device that uses cathodoluminescence to increase the brightness of an image. It is comonly found in night vision scopes and scientific equipment. Cathodoluminescence, using a phosphor to convert electrons to photons, is an established technology used in cathode-ray tubes. Cathodoluminescent devices have high conversion efficiency (40 lumens/watt), high reliability, and can achieve very high output brightness (projection televisions).

Our first research objective was to produce a laboratory demonstration of the system, and to quantify its performance. An integrated circuit with light-emitting arrays was fabricated in a commercial 0.18µm CMOS logic process. Each array measured 16x32 pixels and included a wordline decoder. Each pixel contained a 1-bit digital memory along with light emitter and driver circuits. We used the p+/nwell junction as a light-emitting structure. Power conversion efficiency was approximately 10^{-6} (W/W), and we observed a broad emission spectrum peaking at 700nm. A test system consisting of the integrated circuit, microscope optics, and image intensifier has been constructed. Sample images were recorded, as shown below. Grayscaling was demonstrated at 32-levels, limited by the speed of the speed of the microcontroller.

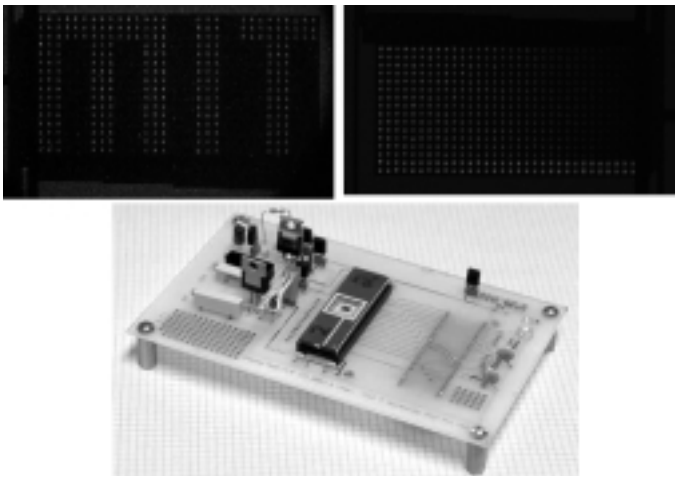

Fig. 26: Top left: image from test system captured with CCD camera, Top right: 32-level grayscale demonstration, bottom left: circuit board including IC in 0.18um CMOS process.

In the near future, we will investigate circuit designs to support the integration of light emitters onto CMOS integrated circuits. Memory can be added to the display to eliminate the need for refreshing, thus reducing switching power. Analog, or digital multiple bits-per-pixel memories are being investigated. In addition, row parallel current level addressing is being investigated. This addressing allows analog and digital calibration for precise brightness control of each pixel. High-level computation can be integrated on-chip to perform image processing, or data compression/decompression, or intelligent power management. High-resolution dis-

plays require large input data bandwidth, for example computer monitors typically require over 2GHz bandwidth and interface circuits dissipate high power. For example, The Silicon Image Sil 161B digital video interface receiver dissipates 800 mW. Interface circuits using compression and/or circuit techniques such as low-swing signaling can reduce the interface power dramatically, lowering the overall system power.

We will also be investigating a RF wireless link between the display and the host. For high resolution displays, even with on-chip data compression, the I/O data rate will still be very high. For this reason, the traditional narrow-band wireless link is not a suitable technology. We propose ultra-wideband data communication technology for host-to-display data communication. This technology can potentially be extended to chip-to-chip and back plane data communication as well. The ultra-wideband communication, which has been in limited use for medium-to-long range (~mile), low-data rate communication, employs a train of impulses rather than a single frequency RF carrier. The impulse train has a very wide frequency spectrum, typically DC- GHz range. Since the energy is spread in such a wide frequency range, there is negligible interference with traditional narrowband RF systems. Unlike narrowband transceivers, highly frequency selective circuits are unnecessary facilitating the integration of the entire transceiver. Also, the effect of the multipath can be mitigated, and even exploited by measuring the arrival time and the phase of the multipath signals. For this reason, the untra-wideband technology is more suitable for short-range, fixed environment communication than the application that has been in use. The host-to-display, chip-to-chip, and backplane communication can benefit from the ultra-wideband communication because they are typically short-range, fixed environment communication. The short-range nature of the host-to-display, chip-to-chip, and backplane communication could provide a reasonable signal-to-noise ratio, which, combined with ultra-wideband would provide potentially very high data rate required in such data communication. Also, the host-to-display wireless link has an added possibility of broadcasting to multiple displays.