5.8 GHz Wideband Receiver for Wireless Gigabit LAN

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To take advantage of space-time diversity algorithms, multiple receiver front ends are needed on a single chip. Direct conversion does not require an image reject filter and simplifies the Radio Frequency (RF) filtering requirements. The nature of multiple receivers on chip, however, implies that the homodyne's local oscillator radiation would significantly interfere with nearby receivers since its frequency is in-band to the desired RF signal. In addition, a direct conversion receiver performs in-phase and quadrature (I/Q) demodulation in the analog domain. An I/Q phase imbalance, directly impacts the bit-error-rate performance. With a heterodyne architecture, the received signal can be digitized at the IF and the functions of I/Q demodulation along with channel selection can be performed in the digital domain.

The receiver for the WiGLAN performs amplification, filtering and downconversion of the 150 MHz signal centered at 5.8 GHz. The receiver downconverts the Radio Frequency (RF) signal to an Intermediate Frequency (IF) that is fed to the analog baseband processor where it is equalized and digitized. The design approach for the receiver is based upon block level analyses that consider the gain, noise, and linearity tradeoffs necessary for the WiGLAN's adaptive modulation scheme.

The focus of this research is the design of on chip filters within the framework of the Wireless Gigabit LAN receiver design. To reduce the effect of image frequencies for the heterodyne receiver, a dual conversion architecture is selected to allow for optimized frequency planning. As such, filters are needed for the band selection and image rejection at the RF carrier frequency, band selection at the first IF, and anti-aliasing at the low IF. The primary challenges are to obtain the necessary band and image rejection filtering with an integrated approach without severely degrading the system's noise and linearity performance.

An initial integrated image reject filter was designed, simulated, and fabricated in IBM BiCMOS 6HP process technology (Figure 24). The filter incorporates an on chip inductor that has its quality factor enhanced through the use of a negative resistance circuit. The filter's center frequency is tunable externally with a DC voltage. In addition, by controlling the DC current of the negative resistance circuit, the rejection response is also adjustable (Figure 25). This simple notch filter circuit performs rejection at the image frequency. This initial circuit serves as the building block for more complex responses for both the image band rejection and the signal band selection at the RF and IF stages. Besides the impact on the receiver's noise and linearity performance, the design of integrated filters must also consider issues of stability and possible automatic frequency response adjustments to account for device tolerances.

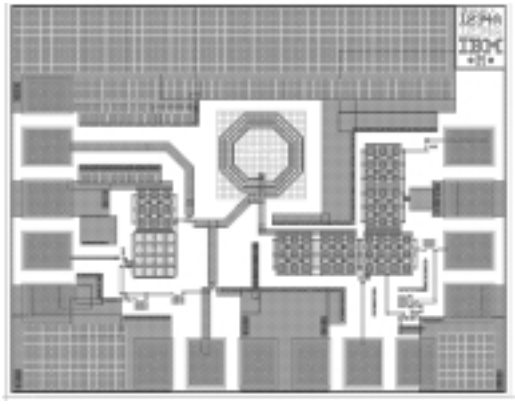

Fig. 24: Layout of notch filter for image rejection on IBM BiCMOS 6HP process.

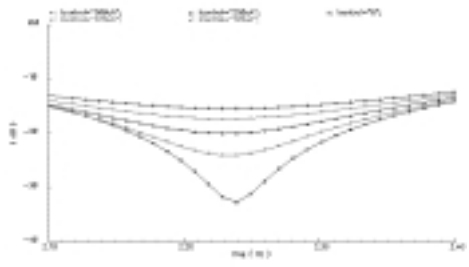

Fig. 25: Tunable notch for device tolerances.