Biasing and Power Combining Techniques for Power Amplifiers

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Power amplifiers with conventional fixed biasing attain their best efficiency when operated at the maximum output power. For lower output levels, these amplifiers are very inefficient. This is the major shortcoming for use in recent wireless applications with an adaptive power design; where the output power is a function of the bit-error rate, channel characteristics, modulation schemes, etc. Such applications require the power amplifier to have an optimum performance not only at the peak output level, but also across the power range.

One way to improve low-level efficiency is to use adaptive biasing, where the biasing circuitry senses the input signal, averages it, and adjusts the bias current based on the detected RF input level. The adaptive biasing technique is implemented using the IBM 6HP SiGe BiCMOS process for a class-A power amplifier. The simulated efficiency curve, and the test chip micrograph are shown in the following figures.

Another way to improve efficiency performance across the output range employs multiple power amplifiers with a power combiner. In this case, a number of smaller power amplifiers, each of which is optimized for a fraction of the maximum required output power, feed their outputs to a low-loss power combiner. Depending on the input level, the controlling circuits turn on an appropriate number of power amplifiers. Such a configuration ensures that each power amplifier operates at or near its highest output level and improves efficiency across the output power range.

The multiple power amplifiers combining technique also reduces constraints caused by low transistor breakdown voltages as technology scale. As a proof of concept, a four-port printed-circuit board micro-strip combiner has been fabricated for use with four identical power amplifiers. On chip combiners will be studied for the possibility of a fully integrated power amplifier using these power combining techniques.

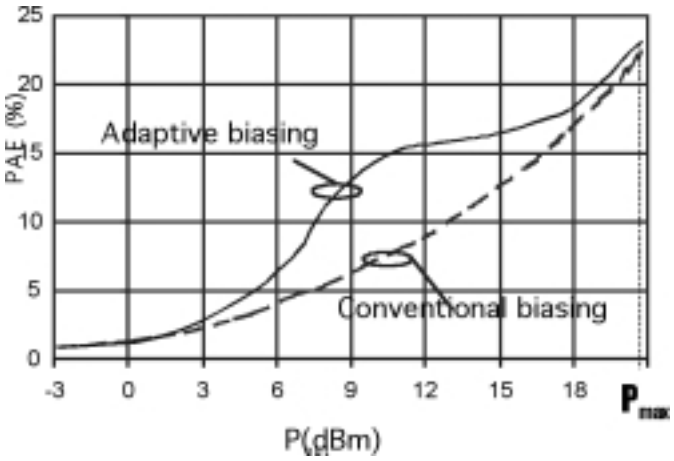

Fig. 22: Power added efficiency vs. input power with and with and without adaptive biasing.

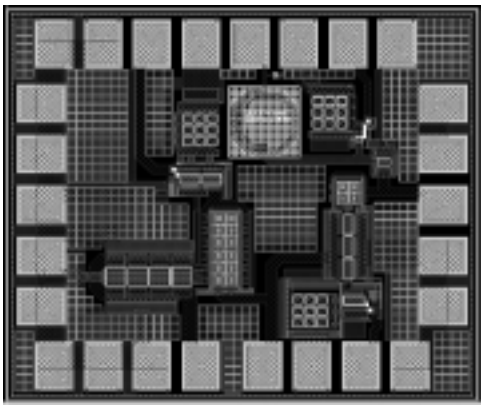

Fig. 23: Layout of power amplifier with adaptive biasing using IBM BiCMOS 6HP process.