Analog Base-band Processor for Wireless Gigabit LAN

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Sponsorship
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The base-band analog processor performs necessary signal processing on the 150 MHz base-band signal in the transmit and receive signal paths for a wide-band wireless local area network. The individual channel characteristics depend on the RF signal fade and interference. Broadcasting to multiple appliances requires channel equalization at the receiver. In the receive (Rx) section, the wide-band amplifier amplifies the received signal from the RF transceiver network and is followed by a equalization filter. The amplitude of the signal following the channel equalization filter can very greatly, depending on the channel conditions, so a programmable gain amplifier is needed to better match the signal amplitude to the dynamic range of the subsequent analog-to-digital converter. The demodulation of the carrier is then carried out in the digital domain by a DSP.

There are tremendous technical challenges in the development of the base-band analog processor. The analog circuits in both the transmit and receive sections of the processor must handle 150MHz of signal bandwidth with high signal-to-noise ratio. These analog circuits include the Wide-Band Amplifier (WBA), the Programmable Gain Amplifier (PGA), the anti-alias filter, the channel equalization filter, the D/A converter in the Tx section, and the A/D converter in the Rx section. In order to digitize the wide 150 MHz signal band, the A/D converter must have an effective sampling rate of at least 300 MHz, and preferably above 600 MHz to ease the anti-alias and digital filtering requirements. The preliminary estimate of the A/D converter resolution needed to handle the wide dynamic range of the received signal is 12 bits. At present, such high performance is beyond the capability of monolithic silicon integrated circuits. Additionally, any harmonic and intermodulation distortion in the signal path produces spurious signals in other sub-bands, so the WBA, the PGA, the anti-alias and channel equalization filters and the A/D converter must exhibit very high Spurious-Free Dynamic Range (SFDR) in addition to wide bandwidth. In the Tx section, the D/A converter and reconstruction filter must posses similar performance levels. In order to address these technical challenges, we propose to investigate innovative techniques for the base-band analog processor.

This work focuses on the implementation of the extremely high speed, high resolution, and wide-bandwidth A/D converter in the Rx section. To achieve high speed operation, some degree of parallelism is often employed. In a parallel time-interleaved converter, any mismatch in the gain, offset, or timing of the constituent channels results in undesirable harmonics in the output spectrum, related to the sampling rate of the individual channels. Therefore, the present time interleaving typically employs a small degree of parallelism, so that the harmonics either out of the signal band of interest, or below the quantization noise floor. Our approach is to use large-scale parallelism (64 or 128 channels) in a time-interleaved pipeline A/D converter. Back-end digital calibration is applied to account for static gain, offset, and timing mismatch errors between channels, so that the resulting calibrated output has sufficiently low spurious harmonics.

Measurement and calibration techniques for gain and offset errors are performed using standard calibration techniques. By digitizing a fast ramp using one converter as a fixed timing reference for the remaining converters, the relative timing skew between channels can be discerned. The calculated timing offsets are then used to re-time the output data stream using polynomial interpolation in the DSP in the back-end. Thus all of of the calibration is performed using simple algebraic operations with minimal latency. To allow all of the calibration operations to be performed in the background, a small fraction of the available channels are systematically pulled out for calibration, while a novel token-passing control scheme selects which of the 'active' converters will sample the incoming signal.

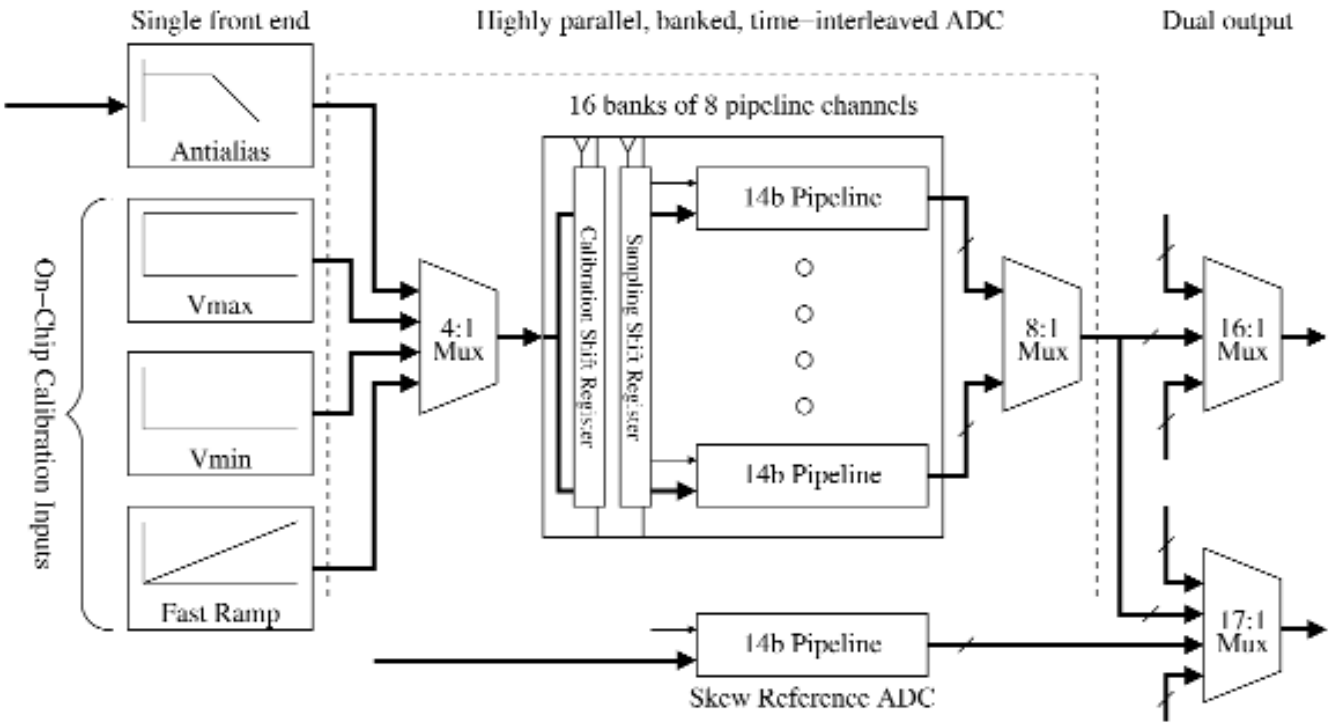

Fig. 21: A top-level block diagram of the proposed A/D converter. 129 identical pipeline A/D channels are organized into 16 banks of 8 converters, with one additional converter used only as a skew timing reference. In this scheme 2 banks are pulled out at a time for calibration, so the remaining 112 converters operate at about 5.5 MHz to achieve the desired 600MHz aggregate sampling rate. 14 bit pipelines are used to generate 12 bit digitally error-corrected outputs. The converter bank that is actively digitizing the input signal receive the output of the front-end anti-aliasing filter. The converter banks that are under calibration may digitize DC values for gain and offset measurements or the fast ramp for timing skew measurements. The converter has two sets out outputs so that digitized signal samples and calibration data may be output simultaneously. The back-end DSP averages the calibration data, and generates the algebraic coefficients needed to correct the gain, offset, and timing mismatch errors.