The Low-Power Bionic Ear Project

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The aim of the project is to construct a cochlear-implant processor for the deaf that has the potential to reduce the current power consumption of such processors by more than an order of magnitude via low power analog VLSI processing. In addition, a cochlear implant processor that is based on the architecture of a silicon cochlea, i.e., on an analog electronic model of the inner ear, is being explored for its potential to revolutionize patient's speech recognition in noise (Rahul Sarpeshkar, Lorenzo Turicchia, George Efthivoulidis, and Luc Van Immerseel, "The Silicon Cochlea: From Biology to Bionics", accepted paper, Proceedings of The Biophysics of the Cochlea: Molecules to Models Conference, Titisee, Black Forest, Germany, July 27-August 1, 2002.)

Several building block circuits for such a processor including a 100uW analog front end, a programmable bandpass filter, and a logarithmic map circuit were designed. Figure 14 shows a chip photograph of a DAC programmable fourth-order programmable bandpass filter that operates on 6uW of power consumption with over 60dB of dynamic range on a 2.8V supply (Christopher Salthouse and Rahul Sarpeshkar, "A Micropower Bandpass Filter for Use in Cochlear Implants", accepted paper, IEEE International Symposium on Circuits and Systems, Arizona, May 2002.)

Figure 13 shows the overall system architecture of a current bionic ear system (cochlear implant system). Sound that is transduced from a microphone is eventually converted into electrode stimulation in surgically implanted electrodes. The aim of this project is to reduce the power consumption to levels that will enable fully implanted systems to become a reality.

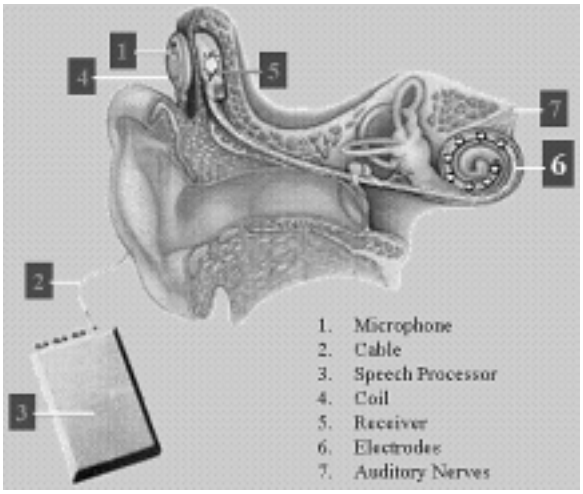

Fig. 13: Overview of a Bionic Ear System.

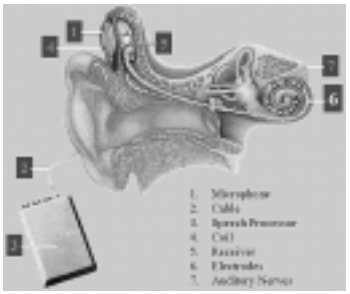

Fig. 14: Capacitive Attenuation Filters built on AMI's 1.5µm BiCMOS process.