Novel Techniques Addressing Delay and Power Issues in Deep Sub-Micron Buses

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Sponsorship

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In deep-submicron technologies the primary component of delay is shifting from logic gates to the interconnect network. Buses can no longer be considered as a set of independent lines that don't interact. A more appropriate model would treat the bus as a distributed system, where a transition on a line would affect adjacent lines as well. However, the transitions on the buses can be grouped into delay classes, depending on the effective capacitance that the driver circuit needs to charge.

A very effective way to reduce delay in buses is by eliminating the transitions that are relatively time consuming. We are using coding schemes to accomplish that, by increasing the number of lines in the bus, thus imposing some redundancy. In our implementation we are mapping a 4-line bus to a 6-line bus.

Another significant problem in modern VLSI is the way power is distributed to the various components of a chip. The portion of the power dissipated in the interconnect network is increasing rapidly with technology downscaling. Therefore, smart power aware techniques have to be introduced in order to minimize this portion. As a consequence, this would reduce the total power consumption of the whole circuit.

Our approach exploits charge recycling. The stored charge is redistributed and shared among the lines that make a transition. We are building smart and effective bus drivers that generate the control signals, implementing the charge recycling technique. The resulting partial charge conservation reduces power consumption.