Power Aware Hardware Reconfigurable Digital Signal Processing Architecture for Wireless Communications

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Energy dissipation is a critical design constraint for integrated wireless systems, particularly for mobile applications. For deep submicron designs, subthreshold leakage is becoming an increasing component of over all energy consumption. This research explores the use of architecture and circuit techniques to address energy consumption in both standby and active modes. The proposed system includes a novel architecture for an energy efficient FPGA core.

FPGA's have been shown to be computationally efficient for implementing signal processing functions based on Distributed Arithmetic (DA). Tuned for DA signal processing, the logic blocks in our design allow can significantly increase design density thereby relieving pressure on interconnect resources. The logic block architecture features the ability to automatically power down inactive elements to reduce current leakage. Interconnect elements, a dominant source of power consumption, are tuned to match this DA structure. The FPGA core is currently being targeted for a 1.0-volt, 0.13 micron, dual voltage threshold logic process with a full custom design flow.

The FPGA core when embedded with a microprocessor core and environment monitoring hardware (shown in the figure) can be dynamically reconfigured to allow for tradeoffs in energy usage versus algorithm complexity.

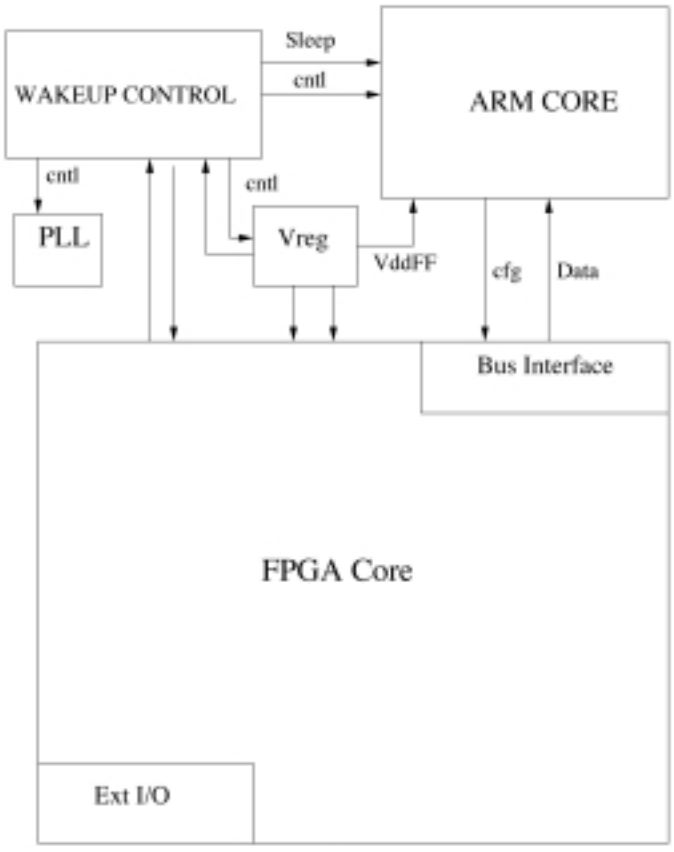

Fig. 8: