Circuit Techniques for Subthreshold Leakage Reduction in a Deep SubMicron Process

Personnel
B. Calhoun (A. P. Chandrakasan)

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Texas Instruments

The trend of process scaling for CMOS technology has made subthreshold leakage reduction a growing concern for submicron circuit designers. Power consumption has become a principle design consideration as device sizes decrease and many more devices fit on a single chip. Since switching power is proportional to V_{dd}^2, new processes are tailored for lower supply voltages. The decrease in V_{dd} slows down devices which requires that the threshold voltage, V_t, must be lowered to maintain performance. This reduction of V_t produces the exponential increase of subthreshold leakage currents that has become well known.

Field Programmable Gate Arrays (FPGAs) are one type of chip that could benefit from subthreshold leakage reduction techniques. The programmable nature of FPGA designs is amenable to standby mode leakage reduction since some of the logic blocks might be unused. Leakage reduction for programmed blocks would make FPGAs more attractive to the designers of battery-operated devices.

Our research demonstrates circuit techniques to reduce subthreshold leakage for the TSMC 0.13 μm process. Although applicable to generic CMOS circuits in this process, the techniques in this work are specifically intended for use in low power FPGA design.

A testchip uses Multi-Threshold CMOS (MTCMOS) style logic design to implement a new type of FPGA architecture for distributed arithmetic. The circuits are designed to provide maximum reduction in standby leakage current without degrading performance of the circuits by more that 10% relative to an all low-V_t design. Sections of the FPGA which are not used in a given configuration are automatically placed in a low leakage state. The design also uses flip-flops that retain state in standby mode.