
Subthreshold Circuit Design for Ultra Low Power Sensor Systems

Personnel

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Energy efficient Digital Signal Processors (DSPs) are becoming increasingly important with the growth of portable, wireless, battery-operated appliances such as cellular phones, Personal Digital Assistants (PDAs) and laptops. In the constantly changing environment of a portable device, an energy-aware DSP is required for long battery lifetimes and high system efficiency. An energy-aware DSP will be able to adapt energy consumption as energy resources of the system diminish or as performance requirements change. This is in contrast to low power design, which targets the worst case scenario and may not be globally optimal for systems with varying conditions.

My research into energy-aware DSPs focuses on several aspects of energy-aware design : algorithm, system, architecture and circuits. In particular, we have been exploring the use of subthreshold circuits for ultra low power computational engines. Subthreshold circuit design is the design of circuits whose voltage supply is scaled down below the threshold voltage. These circuits use the subthreshold leakage currents to switch load capacitances, currents which are orders of magnitude lower than in the strong inversion regime. We will explore different logic families and memory design for the subthreshold regime, and these techniques will be demonstrated through the design and implementation of a 1024 FFT processor operating at voltage supplies as low as 100 mV.
