# Hardware Architecture for a Power-Aware Microsensor Node

## Personnel

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The second prototype of a power-aware microsensor node has been developed for the MIT $\mu$AMPS project. The improvements from the previous generation include smaller footprint size of the node to facilitate unobtrusive sensing, baseband and slave snap-on modules, additional hardware controls at all levels for precise power manipulation, improvements in the radio performance that allow for transmission distances up to 100 meters, and improved circuits. Additionally, a link layer was fused with the radio board, and a MAC layer has been developed to demonstrate the innovative power aware features of the $\mu$AMPS system-driven design.

SENSORS: Microphone amplifier stages and an integrated 12-bit A/D are added to the processor board. The higher order filters of the mircrophone circuit and improved noise filtering allow for accurate data gathering. The first $\mu$AMPS application will be acoustic sensing.

PROCESSOR AND MEMORY: The $\mu$AMPS processor module is a 55mm square PCB with a StrongARM CPU, SRAM, and flash ROM. The module also includes high-efficiency dc/dc converters that provide regulated power for all of the digital electronics in the mAMPS node. The StrongARM core is powered by a special variable-voltage dc/dc converter that allows the core voltage to be adjusted, on the fly, to match the processor's clock speed (which also can be adjusted on the fly). This significantly reduces the leakage power dissipated in the processor. The operating system used on $\mu$AMPS node is RedHat eCos, This operating system was chosen because of its high degree of configurability, which allows the system's memory requirements to be minimized. Custom power management functionality has been developed and added to eCos, in order to exploit the power scaling capabilities of the $\mu$AMPS hardware.

RADIO: The second prototype of the $\mu$AMPS radio matches the 55mm square footprint for the node module stack. The radio module operates on the ISM 2.45GHz band, and is built from commercial parts. A 6-level, power aware power amplifier is used to allow the radio to react to environmental and system-driven requirements. A small feature size antenna is integrated onto the PCB, as well as circuitry to provide automatic tuning of the varactor in the discriminator circuit. The maximum bit-rate of a point-to-point wireless link is 1Mbps. The link layer is integrated onto the radio PCB and acts as a memory storage block as seen by the $\mu$AMPS processor board. Extensive power routing, microstrip layout, and noise isolation techniques are used in the layout of the $\mu$AMPS radio board.

The power aware features of the $\mu$AMPS board allow for thirteen relevant power consumption stages. Among those thirteen states are six states of different power amplifier gains to support transmission distances from 10 meters to 100 meters. In the off state, the radio consumes no power. In the idle state, the radio consumes 60mW, mostly due to the off-chip VCO and idle current of the commercial transceiver chip. In the receive state, the radio consumes 280mW. In the lowest transmit state, the radio consumes 330mW. In the highest transmit state, the radio consumes 1.1W. There are other minor intermediate stages that have not been described which can be intelligently used in local data management algorithms to improve power awareness. By system flexibility, low power circuit design and creative system-driven algorithms for the MAC layer, this versatile radio is able to help demonstrate some basic techniques that contribute to a power-aware wireless sensor network.

MAC LAYER: In a distributed wireless sensor network, hundreds of randomly scattered microsensor nodes are capable of ubiquitous sensing and data gathering. In such a system, a need to prolong the lifetime of the network is crucial and limited by the battery capacity. As communication traffics among sensor nodes are driven by sensing events, power-aware features can be integrated in each layer of protocol stacks design.

Specifically, embedding power-aware features in Media Access Control (MAC), and network layer, promises to extend the lifetime of the sensor network.

We have chosen TDMA as a MAC layer protocol for its inherited power-aware mechanism of radio shutdowns outside its TDMA slot and in absence of sensing events. Another level of power-aware features can be deployed in MAC ID and TDMA slot assignments. In a field of scattered sensor nodes, not all the nodes are in radio range of one another or of the base station. Hence, assigning N TDMA slots for the network of N sensor nodes that are not all in radio range of one another will waste the receiver energy and link bandwidth. To solve this problem, TDMA slot can be assigned efficiently by being mapped to each node's MAC ID, given that MAC IDs are reused in the network. As the number of different MAC IDs needed for node assignments varies with the number of nodes that are in 2-hop radio range of one another, varying the transmit power and the node density can optimize the system lifetime. Power scalability will be illustrated on $\mu$AMPS sensor node prototypes, with TDMA Media Access and vehicle tracking application.

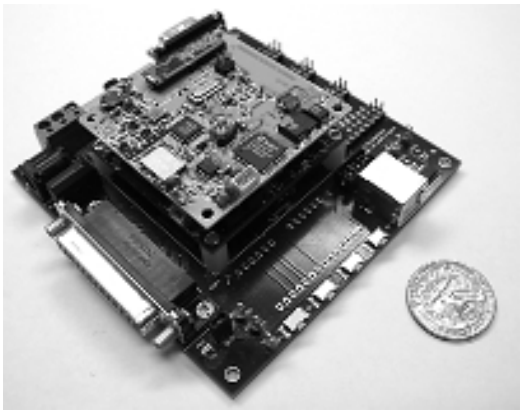

*Fig. 4: Radio Board*