Energy Efficient Transmitter for Wireless Microsensors

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The communication module of a wireless microsensor node must consume low energy in order to maximize the battery lifetime of a sensor network. In order to save power in the radio module, the electronics must be turned off during idle periods. Unfortunately, frequency synthesizers require a significant overhead in terms of time and energy dissipation to go from the sleep state to the active state. For short packet sizes, the transient energy during the start-up can be significantly higher than the energy required by the electronics during the actual transmission. Therefore reducing the start-up time is a key issue in designing an energy efficient radio for microsensors. In addition, power consumption of a transmitter in short range transmission at GHz frequencies is dominated by the radio electronics (frequency synthesizer, mixers, etc.) and not the output transmit power. Hence reducing the power consumption and the on-time of the transmitter is also important to achieve energy efficient transmitter.

These design goals were incorporated to a 6.5GHz BFSK modulator that is capable of achieving fast start-up time, high data rate and low power consumption. To reduce the start-up time, variable loop bandwidth technique was employed in a fractional-N synthesizer, which switches the loop bandwidth from a large to a small loop bandwidth. It achieves 20 μs start-up time, which is 4 times smaller than that of a fixed loop bandwidth.

In order to reduce the power consumption of the frequency synthesizer, trade-off between the analog and digital components were exploited. In detail, loop bandwidth of the sigma-delta synthesizer is optimized, exploiting noise and power properties of divider, VCO and sigma-delta complexity. For high data rate FSK modulation, a closed loop direct VCO modulation technique was employed. The chip uses 0.25 μm CMOS in a SiGe BiCMOS technology. The block diagram and the die photo of the chip are shown in Figure 2 and 3, respectively. The summary of chip test results are shown in Table 1.

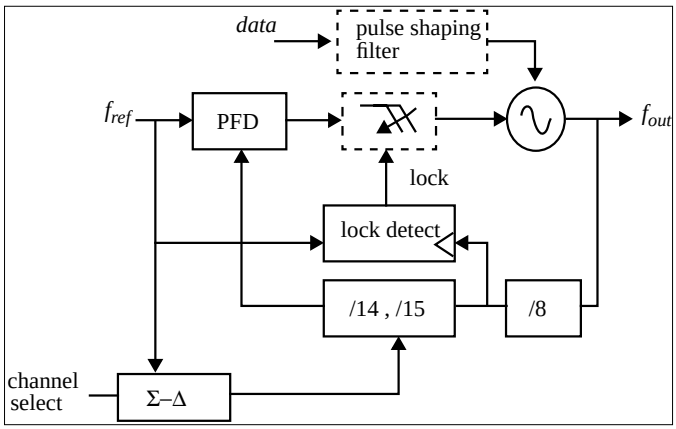

Fig. 2: Architecture of the energy efficient transmitter

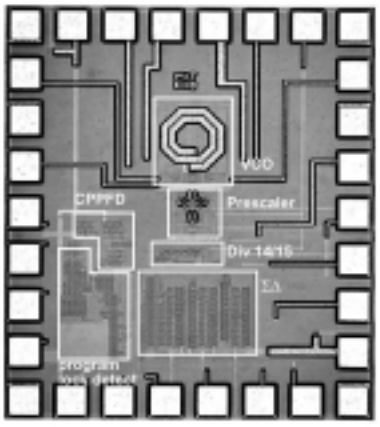

Fig. 3: Die photo of the chip

Frequency:	6.1 – 6.9GHz
VCO phase noise:	-112dBc/Hz @ 1MHz
Data rate:	5Mbps BFSK, (2.5Mbps effective)
Start-up time:	20ms
Power consumption:	22.2mW (VCO:17.7mW, Rest:4.5μW)
Size :	1.2mm x 1.3mm

Table 1: Summary of chip test results