Novel Techniques for Power Reduction, Speed Increase and Optical Clock Distribution in Deep-sup-micron Technologies

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A data-distribution and bus-structure aware methodology for designing coding schemes for low power has been developed. A general class of coding schemes for low power, termed Transition Pattern Coding schemes, has been introduced and its energy behavior has been mathematically analyzed in detail. Two algorithms have been proposed for deriving such efficient coding schemes that are optimized for the desired bus structure and data distribution. Bus partitioning has been mathematically analyzed as a way to reduce the complexity of the encoder/decoder.

In this work we asked: what is the maximum possible reduction in power consumption in deep-sub-micron buses using coding techniques? We answered the question in two steps. First we gave the minimum energy per information bit required for communicating through deep-sub-micron buses. Then, we showed that the minimum energy is asymptotically achievable using coding. In addition, a simple differential coding scheme was proposed that achieves most of the possible energy reduction. The methodology used here also applies to more general communication and computation models.

In this work I also introduced the idea of using coding to increase the throughput and communication speed in deep-sub-micron buses. I used a detailed transmission line model for the bus in order to estimate the time needed for the different transitions to get completed. After classifying the transitions according to their delays, I proposed a coding appropriate for constrained communication channels to increase the communication speed. The idea is to encode the data with the goal of eliminating certain types of transitions that require a lot of time to get completed. By using proper encoding techniques, the bus delay can be reduced by a factor of 2!

Finally, a class of circuits that accurately compare the phase difference between periodic optical and electrical signals of the same frequency has been developed. These novel topologies have allowed the development of a new optical on-chip clock distribution architecture that bypass the disadvantages of trans-conductance amplifiers.