Three-dimensional Integration of GaAs and Si Circuitry Using Low Temperature Oxide Bonding Techniques

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Recently we proposed the development of a technology for 3-dimensional heterogeneous integration of silicon CMOS VLSI (memory and signal processing electronics) with III-V HEMT and HBT MMICs using aligned low-temperature oxide wafer bonding, with the purpose of dramatically increasing the capabilities, complexity, and performance of microwave integrated circuits, and we are currently pursuing this goal in a one-student effort.

The aspects of modern electronic systems that are hardest to integrate on GaAs and InP are large amounts of memory and highly complex signal processing circuitry. By integrating silicon CMOS VLSI directly with III-V MMICs, we immediately add high density memory and complex signal processing circuitry to the MMIC toolbox, highly leveraging the billions of dollars spent on developing modern silicon technology, and leap-frogging completely the costly and formidable (perhaps impossible) problem of fabricating comparable circuitry in GaAs and InP. The proposed technology represents a paradigm-shifting enhancement in MMIC complexity and performance. The CMOS circuitry can be used, for example, to store coordinate data, adjust phase delays and steer beams, tune and/or change carrier frequencies, modify code patterns and keys, monitor signal quality and make critical adjustments to optimize performance, do complex signal conditioning, and much more, in the underlying MMIC. The only limitations to the potential of these Intelligent MMICs should be the imaginations of application engineers.

The present concept builds on the low temperature oxide Silicon-on-Gallium arsenide (SonG) bonding process we developed for optoelectronic integration. The proposal is to bond fully processed silicon and III-V wafers using low-temperature oxide bonding techniques, to remove the substrate of the silicon wafers, and to then interconnect the three-dimensionally stacked CMOS and microwave circuitry to complete the integration process. The silicon circuitry will be strained, but no more than in Silicon-On-Sapphire (SOS) integrated circuits.

Because of the thermal expansion coefficient mismatch between Si and GaAs and the presence of metalization on the processed IC wafers, the 3-D integration process must incorporate low temperature bonding techniques. Consequently, we have explored the use of Low Temperature Oxide (LTO) deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD). The LTO is deposited on the bonding surface of both the GaAs and Si wafers. In order to promote the desorption of various species from the LTO, the film is densified at 450˚C following deposition. The LTO is then Chemo-Mechanically Polished (CMP) to obtain a planar surface with a low microroughness. We have found from studies using Atomic Force Microscopy (AFM) that surfaces with a microroughness less than 5 Angstroms r.m.s. will bond quite readily. However, even when the surface meets this low microroughness criteria, the bond quality may be adversely affected by the presence of CMP slurry particles left on the surface as a result of the CMP step. We are currently exploring the effectiveness of using Poly-Vinyl Alcohol (PVA) post CMP cleaning pads to help remove such particles. After the post-CMP clean, the wafers are bonded at room temperature and annealed to temperatures approaching 200˚C. We have found that at temperatures above 200˚C, the wafers will break or separate due to the thermal expansion coefficient mismatch. It is only after the substrate removal of the SIMOX wafer that the wafer pair may be exposed to higher anneal temperatures, where the maximum temperature is then set by the presence of metal on the wafers.

We have successfully demonstrated the wafer bonding of Si to GaAs using the aforementioned process. In this case, the Si wafer contained a serpentine Al metal pattern consisting of 1000 Angstrom thick metal with 5μm wide lines set at a 5μm spacing. This successful bond is

an important step toward the goal of bonding fully processed SIMOX wafers to GaAs wafers. We are currently working on obtaining fully processed SIMOX wafers from IBM in order to test our process for a “real world” case. We hope to eventually demonstrate a fully integrated and interconnected system in which processed GaAs wafers are bonded to processed SIMOX wafers.