A Silicon Substrate-Via Technology with High Aspect Ratio

Personnel

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As silicon RF integrated circuits strive for high-performance operation at high frequencies, it becomes increasingly important to reduce all parasitics. Of particular concern are the source impedance of MOSFETs and the emitter impedance of BJTs, which greatly affect the gain and efficiency of RF amplifiers. To address this, we have developed a through-wafer via technology for silicon, which allows the implementation of high-aspect ratio, low-impedance ground connections. Because this via technology incorporates an insulator liner, it could also be used to distribute power, ground, and signals in logic circuits and MEMS. Furthermore, this technology has enabled a novel isolation scheme to reduce crosstalk in mixed-signal circuits for System-on-a-Chip (SOC) applications.

Via etching was performed by DRIE from the front of the wafer to produce nearly vertical sidewalls. Aspect ratios as high as 49 were achieved. The insulator liner was made of silicon nitride, which, in addition to electrically insulating the via from the substrate, prevents Cu diffusion into silicon. Si_3N_4 was deposited by PECVD. The conformality of the nitride is limited to an aspect ratio of approximately 15. Copper was electroplated starting from a Ta-Ti-Cu seed layer that was e-beam deposited on the backside of the wafer. We used CMP to remove excess Cu. We have succeeded in completely filling trenches with Cu with an aspect ratio of 49, and vias with an aspect ratio of 10.

A test structure for measuring the impedance of a single via in the microwave regime was designed and fabricated (see figure inset). The ground pads are shorted to the Cu ground plane through a large number of vias. We found that up to 50 GHz, the vias could be accurately modeled by a resistor-inductor series network. The figure shows the extracted inductance of several vias as a function of the nominal via aspect ratio. The figure also includes a theoretical calculation. The experimental data agree well with the model. This gives us confidence that the proposed technology can produce vias with theoretically minimum inductance.

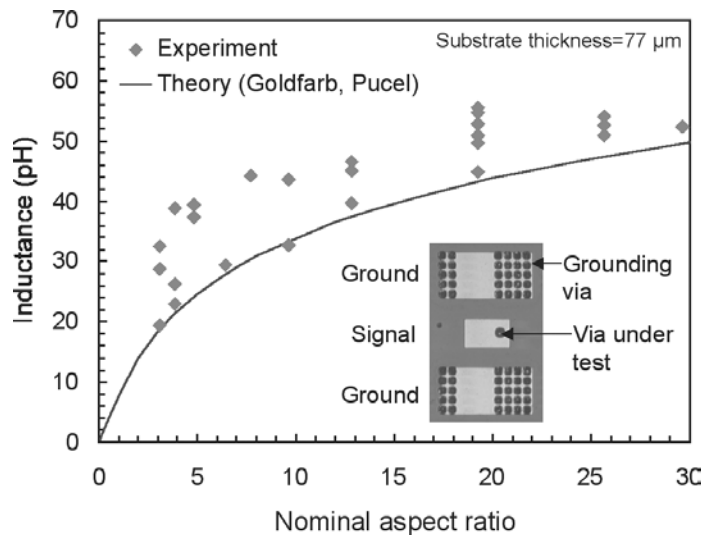

Fig. 36: Inductance vs. aspect ratio of vias on a substrate thickness of 77 µm. Each data point represents a different via. Plotted in a solid line is the theoretical inductance following the model of Goldfarb and Pucel. The inset is a picture of an actual test structure with a 12-µm wide via under test. The multiple grounding vias are introduced to reduce the impedance of the ground pads.