Field Emitter Arrays for Low Voltage Applications with Sub 100 nm Apertures and 200 nm Period

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Field emission devices operate on the basis of electron tunneling through a surface energy barrier when the barrier width is "reduced" through the application of a voltage to a controlling electrode (gate). The electrons tunnel from the emitter and are collected by the anode. The emission current is proportional to the electron supply and transmission through the barrier. Significant transmission occurs when the barrier width is about 2 nm corresponding to a surface field of 2×10^7 V/cm ($\chi Si \approx 4$ eV). Using a simple ball-in-sphere model to represent the tip and gate aperture, the electric field at the tip surface is given by $E_{tip} = V\left(\frac{1}{r} - \frac{1}{R}\right)$, where r is the tip radius and R is the gate aperture. From this simple model it is obvious that to obtain electron emission at a low gate voltage, both the aperture and the tip radius have to be scaled to smaller dimensions.

Our approach to reducing the gate aperture is to use tri-level resist and interferometric lithography to create tri-level resist posts that were used to pattern oxide disks which were in turn used to define silicon tips using an isotropic etch in SF_6. The resist posts have 100 nm diameter and 200 nm period resulting in tip density of 2.5×10^9 tips/cm^{-2}. The tips were then sharpened in dry oxidation at 950°C. After oxidation, the cap was removed and conformal layers of silicon dioxide and poly-silicon were deposited by Low-Pressure Chemical Vapor Deposition (LPCVD). The poly-silicon layer was doped by P ion-implantation followed by furnace annealing. The gate aperture was defined by Chemical-Mechanical Polishing (CMP). Figure 35 shows a silicon field emission array with 70 nm gate-aperture and 200 nm period while Figure 36 is a TEM of a tip from the array indicating a radius of about 1.6 nm comparable to radius of single walled carbon nanotubes (1.4nm). A large number of TEMs were taken and Figure 37 shows that the tip radius follows a log-normal distribution with a peak at 3.5 nm. The tip radius distribution could be traced to the initial resist post diameter distribution.

Using interferometric lithography, we demonstrated 70 nm gate aperture Silicon FEAs at a 200 nm period that turned on at gate voltages as low as 8.5 V and achieved emission currents of 1 μA at Vg of 13 V, which represents an array current density of approximately 10 μA/cm^2. Currents as high as 30 μA were measured at V_g of 21 V. A typical I-V transfer characteristics taken with an anode voltage of 600 V is shown in Figure 38b while the corresponding Fowler-Nordheim plot is also shown in Figure 38a. Using first order analysis based on calculating the tip surface field with the ball-in-sphere model, a tip radius of about 1.7 nm was extracted from the slope of the Fowler-Nordheim plot assuming the barrier height is the electron affinity of silicon. The use of numerical simulation to analyze experimental array performance indicated that the tested arrays exhibited characteristics of simulated devices with tip radius of 2 nm. An analysis using a TEM was done to determine a tip radius distribution (~100 tips were measured) and verified tips radii under 2 nm, which was in agreement with the electrical characterization and simulation. More detailed simulations using the calculated tip distribution confirmed the fact that only the sharpest tips, even if only a small percentage of the total, will dominate the array performance.

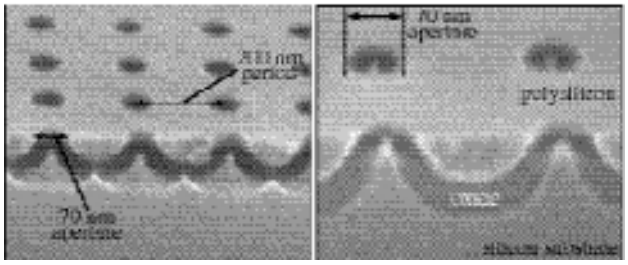

Fig. 35: 200 nm period silicon arrays. The gate apertures on these arrays ranged from 70 – 90 nm. The figures show varying amount of gate oxide being removed.

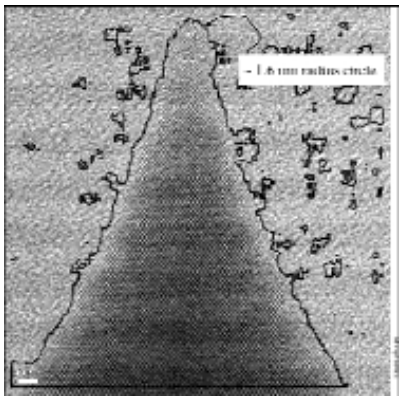

Fig. 36: TEM Micrograph processing using Fourier Analysis. The micrograph can be enhanced using a simple spatial frequency analysis of the electronic image.

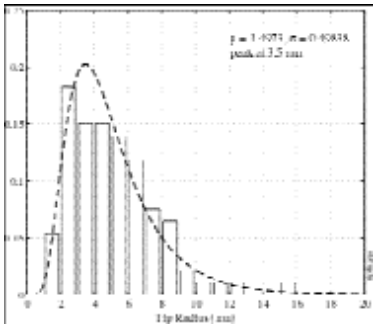

Fig. 37: Distribution of Silicon Tip radius. Tips from an oxidation sharpened Si array was measured in an SEM and a TEM. The data from over 90 tips is shown by the bars of the histogram and the dashed line is the fit to a log-normal PDF.

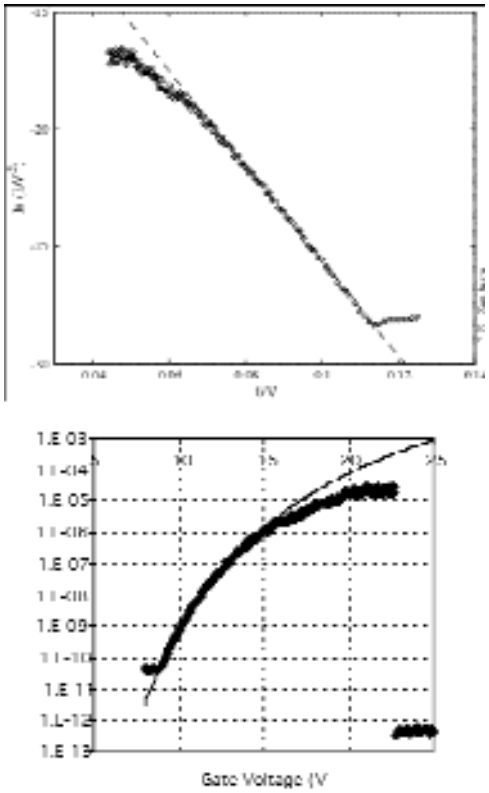

Fig. 38: IV and FN for 200 nm period silicon array (729200). Anode current vs. Gate voltage and FN plot for array 7_29_2_00, 100 × 100 mm, tested at 5×10^{-10} torr. Fowler Nordheim coefficients: aFN = 4.9×10^{-3}, $b_{FN} = 203$, $\alpha = 1.9 \times 10^{-11}$, $\beta = 2.6 \times 10^{6}$. The lines are the fit to the Fowler Nordheim equation, which is used to extract the coefficients.