Mobility in Ultra-Thin SOI MOSFETs

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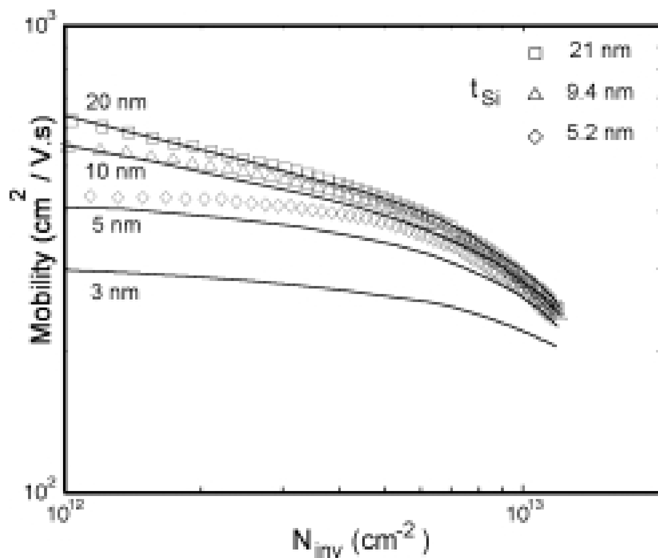
Double-gate devices with ultra-thin SOI thickness are considered as the most promising candidates for scaling down to 10 nm. In order to suppress short-channel effects, film thickness should be scaled down along with shrinking the gate length (e.g. 3 nm-thick for 10 nm gate length). It has been shown both theoretically and experimentally that the mobility is degraded for films thinner than 10 nm. To consider this degradation in device simulation and optimizations, we have developed a method to calculate the mobility in ultra-thin SOI films based on the spatial distribution of the carriers. Self-consistent Schrödinger-Poisson simulations are used to obtain carrier distribution in the film. Experimental universal mobility is then used to correlate this spatial distribution with the mobility. As shown in Figure 25, results of these calculations are in good agreement with recent experimental data for



ultra-thin SOI.

Fig.25 Comparison of the mobility calculated from spatial distribution of carriers with recent experimental results.