Electrical Reliability of GaAs PHEMTs

Personnel

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GaAs Pseudomorphic High-Electron Mobility Transistors (PHEMTs) have great potential for RF power applications. A major issue with these devices is the gradual degradation of certain device characteristics that occur as a result of biasing the device at high voltages for extended periods of time. Previous research in this area has identified the drain side of the device as the region that sustains most of the damage. Also, a close correlation between electrical degradation and impact ionization in the channel of the device has also been established. However, the details of the physics behind this problem are not known and solutions have not been identified.

The first goal of this research project is to provide a fundamental understanding of the physics of electrical degradation of experimental GaAs PHEMTs provided by our sponsor, Mitsubishi Electric (these devices are not under production at this time). Once this is achieved, the next goal is to identify and suggest device design strategies and fabrication process modifications that mitigate the electrical degradation in these devices.

To carry out this research, an automated test suite has been developed that fully characterizes the Device Under Test (DUT), without resulting in any device degradation. This test suite is then used to characterize the DUT before any electrical stressing, and also at frequent time intervals during the stressing experiments. In this way, the time evolution of various key device figures of merit may be closely monitored.

To actually produce electrical degradation in these devices, several different biasing conditions are possible. Since impact ionization has been linked to the electrical degradation in these devices, a stressing scheme that keeps the impact ionization rate constant is desired. Therefore, the type of stressing scheme used to degrade these devices was chosen to be one that keeps the drain current I_D constant and the intrinsic drain-to-gate voltage V_{DGo} constant (relative to the threshold voltage).

Early reliability measurements in these devices suggested that severe bias stressing conditions (high V_{DS}, applied for extended periods of time) were needed to observe any significant electrical degradation. Thus, in order to optimize the time needed for stressing experiments, $V_{DGo}+V_T$ was initially set at a high voltage and then stepped up at various time intervals. Data from the early stages of this type of step-stressing experiment is shown in Figure 24. As seen in the graph, in these experimental devices, the threshold voltage decreases by about 16% after being stressed at high voltage for 1300 minutes.
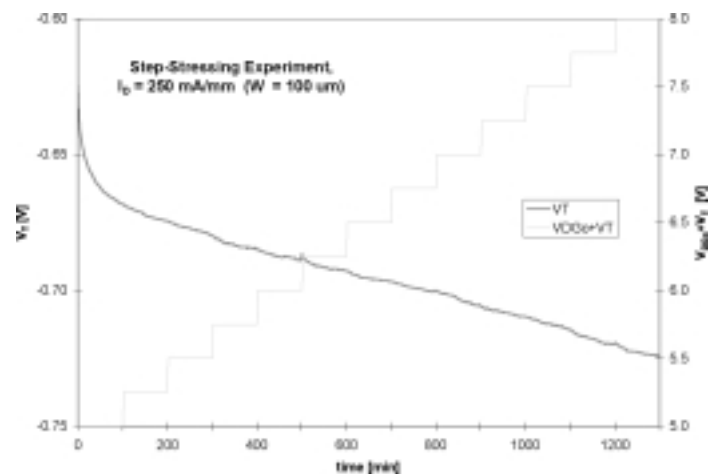

Fig. 24: Time evolution of the threshold voltage of experimental GaAs PHEMT stressed at I_D=250 mA/mm, and $V_{DGo}+V_T$ from 5.0 to 8.0 V.