CMOS-like Fabrication of InP-HEMTs for 100 Gbit/s Photonics Applications

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InP high-electron mobility transistors (HEMTs) have been shown to exhibit the fastest transistor operation of any microelectronics technology. It is believed that InP-HEMT-technology is the only one suitable for fiber optics communication systems at 100 Gbit/s operation and beyond. However, InP-HEMTs suffer from low reliability and manufacturability since the evolution of these devices has mostly been driven by millimeter-wave rather than photonics applications. This is reflected in the fact that only recently digital ICs for 40 Gbit/s optical fiber communications systems have been demonstrated with a complexity of ~10^2 gates. On the other hand CMOS-technology is the most advanced microelectronics technology having achieved integration levels of order ~10^7 gates recently. Hence, it is appealing to explore the possibility of using CMOS-like process techniques for the fabrication of InP-HEMTs.

This project deals with the development of a CMOS-like, fully self-aligned process technology for InP-HEMTs that aims to achieve improved device manufacturability and reliability. In particular, fabrication techniques such as a fully planar process by means of chemical-mechanical polishing, the use of spacers for self-alignment and electroplating play a key role in this project. Figure 23 shows a cross-section of a tentative device design. This particular design exhibits three main features: i) a shallow-trench-isolation (STI), ii) a self-aligned, high aspect ratio gate, and iii) non-alloyed ohmic contacts.

The benefits of this design are as follows: The shallow-trench isolation provides for device isolation while keeping the wafer surface flat and minimizing parasitic capacitances. The use of spacers allows the generation of a small gate footprint from a larger mask opening that is self-aligned to source and drain. Non-alloyed ohmic contacts have a smooth surface and allow well-defined contact geometries, mandatory for scaling-down the devices. As a further benefit of this device design, the gate recess region - known to cause reliability problems – is always covered.

The high manufacturability of InP-HEMTs achievable with the proposed CMOS-like device and process architecture will enable us to significantly improve the reliability as well as the uniformity of these devices needed in order to realize complex integrated circuits operating at 100 Gbit/s and beyond.

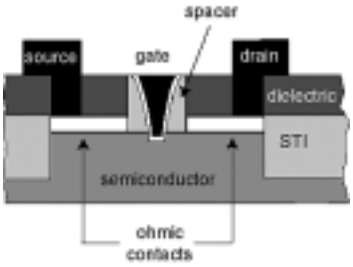

Fig.23. Cross-sectional view of a tentative device design for an InP-HEMT fabricated using a CMOS-like process.