Hydrogen Degradation of InP High Electron Mobility Transistors

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GaAs and InP High Electron Mobility Transistors (HEMT) hold promise for ultra-high-speed photonics and millimeter wave power-applications. A major reliability concern in some of these devices is the shift of the threshold voltage that is observed when the device is exposed to hydrogen. The goal of this project is to understand this reliability problem and find device level solutions to mitigate it.

Recent research at MIT has shown that H exposure results in the formation of TiH_x in Ti/Pt/Au gates. This produces compressive stress in the gate which generates a tensile stress in the heterostructure underneath. The resulting piezoelectric polarization charge in the semiconductor causes a threshold voltage shift. For InP HEMTs with Ti/Pt/Au gates of short gate lengths (around 0.1 μm) shifts of several hundred mV have been seen.

In this project, we developed a model for H-induced piezoelectric effect in InP HEMTs that explains the gate-length dependence threshold voltage shift and provides design guidelines for minimizing H sensitivity. Our modeling approach involves: i) performing two-dimensional mechanical stress simulations in typical heterostructures, ii) computing the resulting piezoelectric charge, and iii) estimating its effect on V_T. This calculation framework provides results that are consistent with the experimental measurements and illuminate the key dependencies of ΔV_T on heterostructure and gate design.

We are recently studying state-of-the art InAlAs/InGaAs HEMTs specifically designed for ultra-high speed optical fiber communication systems. These devices have a WSiN/Ti/Pt/Au gate stack. We have found that the impact of hydrogen on the threshold voltage of these devices is one order of magnitude smaller than conventional Ti/Pt/Au-gate HEMTs. The figure shows the measured and calculated ΔV_T for these InP HEMTs with a WSiN/Pt/Au gate. The agreement is excellent. Our simulations showed that there are three main causes for the improvement of the H-sensitivity. First, the separation of the Ti-layer from the semiconductor by a thick WSiN layer significantly reduces the stress in the semiconductor heterostructure. Additionally, the thinner heterostructure and the presence of an InP etch-stop layer with a small piezoelectric constant underneath the gate both significantly contribute to a reduction in the threshold voltage shift that is caused by the mechanical stress.

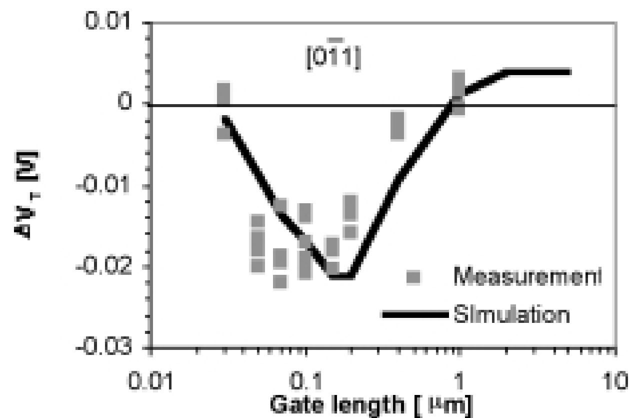

Fig 21: Measured and simulated ΔV_T for InP HEMTs with a WSiN-based gatestack and InP etch-stopper. Gate orientation is [01T].