Dynamic V_T Control with Optimized Planar Double-Gate SOI Structure

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Managing the standby power is becoming increasingly difficult as we are approaching the end of road map. In many applications, most circuits blocks are working in a burst mode and are active only for a portion of time. Leakage current of such blocks can be considerably lowered during idle periods by increasing the threshold voltage of transistors. This approach has been already used in bulk CMOS by using body effect as a means of V_T adjustment. Planar double-gate structure, which is considered as the most promising scalable MOSFET, is also attractive as a dynamic-V_T device. However, using the back gate for threshold voltage control instead of tying it to the top gate degrades the sub-threshold slope and DIBL of the transistor. The structure was optimized through the use of N^+-P^+ gates to push the carries more towards the top gate and by adjusting the length of the underlap between S/D doping and gate edge.

Figure 17 compares the total power consumption of dynamic V_T control scheme with conventional DG operation in a 10 nm device. It can be seen that when the circuit is active only for a fraction of time, V_T control offers more than an order of magnitude reduction in total power.

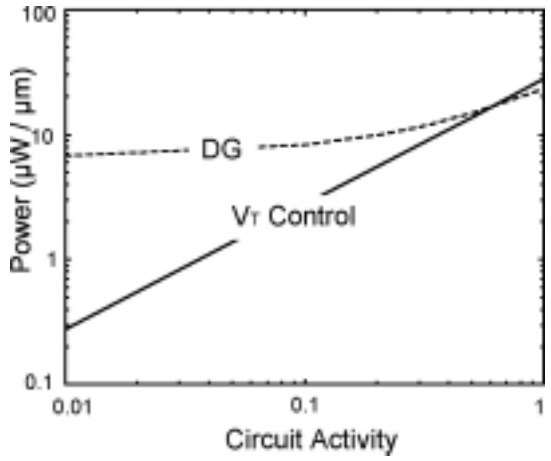

Fig. 17: Comparison of the power consumption in V_T control and DG modes of operation in 10 nm devices as a function of circuit activity.