Ultra-thin Strained Silicon on Insulator MOSFET

Personnel

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Fundamental limits to CMOS scaling are rapidly approaching as devices are scaled below the 50 nm range. Therefore, new methods and materials for CMOS fabrication must be investigated to allow continued device improvement. It is well known that SOI devices provide benefits of reduced parasitic capacitance allowing for high-speed operation while minimizing power dissipation. Ultra-thin body SOI devices have the added benefit of improved electrostatic integrity, and thus can be scaled to the shortest channel lengths. Recent work on surface-channel strained Silicon MOSFETs fabricated on relaxed $Si_{1-x}Ge_x$ show significant performance improvements. Most notably strain-induced transconductance leads to up to 60% enhancement for NMOSFETS over Silicon controls. In this work, a novel fabrication method for ultra-thin strained Silicon on insulator substrate is proposed. In addition, a potential device structure is investigated to achieve the enhanced transport of strained Silicon in a device structure that can scale to the limits of CMOS. The proposed structure combines the benefits of strained Silicon with the benefits of ultra-thin SOI.

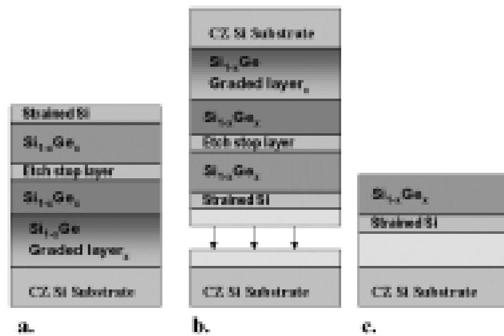

Fig. 14: Strained Silicon on Insulator via Bond and Etch-back: (a) As-grown epitaxial structure, (b) bonding, (c) selective grind and etch back

Our research is focused on both fabrication of strained Silicon on oxide as well as the fabrication and investigation of an ultra-thin body device. For the fabrication of thin strained Silicon layers on oxide two different approaches have been investigated. Both approaches involve the transfer of epitaxial layers to a handle wafer via oxide-oxide bonding. This allows the bonded interface to be well away from the device region. The first method involves a bond and etch-back structure to remove the backside of the wafer (Figure 14). Etch stop layers have been incorporated into the epitaxial structure for improved uniformity. The second method involves hydrogen-ion-implant induced delamination (Figure 15).

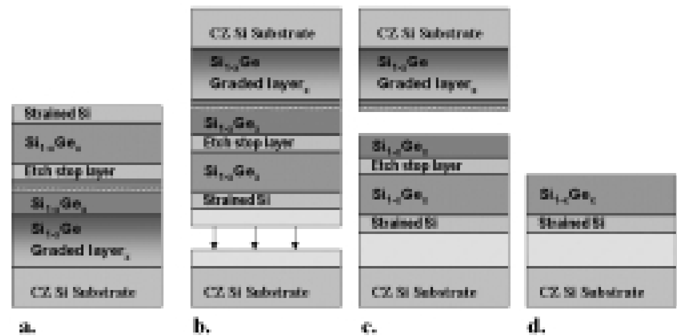

Fig. 15: Strained Silicon on Insulator via Hydrogen Ion Implant: (a) As-grown epitaxial structure with H+ implant, (b) bonding, (c) anneal for hydrogen induced delamination, (c) selective etch.

A cross-section of the proposed initial ultra-thin strained Silicon on insulator device is shown in Figure 16. Key features of this structure include raised source drain regions of thick relaxed $Si_{1-x}Ge_x$. Since the gate length between these regions is quite small it is possible that the strain in the Silicon will be maintained even though there is no $Si_{1-x}Ge_x$ layer directly holding the strain in the gate region. To test the ability of the source drain regions to maintain the strain in the gate region thin slots will be etched and TEM will be used to study the strain. Carrier transport in the device will

be tested in the single-gate, thin body, strained channel MOSFET (Figure 3) and compared to Silicon control MOSFET.

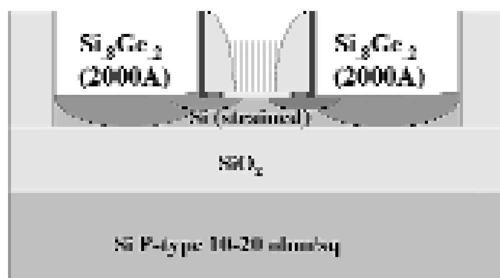

Fig. 16: Ultra-thin Body Strained Silicon on Insulator MOSFET Test Structure